UAV & Robotics Platform (URP)

User Guide

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1 Introduction

The UAV & Robotics Platform (URP) is a small form factor Xilinx Zynq Ultrascale+ ZU7EV based platform intended to be the processing heart of drones or other UAV. It houses the XCZU7EV-fbvb900-2-i SoC which is equipped with a quad core ARM Cortex A53 processor, a dual core ARM Cortex-R5 processor, a GPU with an ARM Mali 400MP and a big Ultrascale+ FPGA fabric including an H.265/H.264 video en/decoding unit.

Because of its targeting domain the URP has ECC enabled 72bit wide DDR4 memory connected to the PS and an onboard IMU consisting of several sensors: accelerometers, gyroscopes, GPS module, magnetic field sensor, temperature/humidity sensor and pressure sensor. Beside these onboard sensors the URP also has connectivity to connect 2 MIPI cameras, 4 motors and GPIO to connect other sensors.

Next to the above mentioned processing power, the URP provides connectivity to connect a Rincon Raptor extension board to enable more functionality, like a software defined radio (SDR), and more processing power with another Zynq Ultrascale+ (XCZU9EG) available on the Raptor board. It is also possible to stack multiple URP boards or to connect a Topic Miami SoM, increasing the processing power and connectivity for motors and/or other sensors. This also allows rapid adoption of new Xilinx silicon technologies in the form of Miami SOM compatible system-on-modules.

The URP comes with a Linux BSP that covers all board peripherals and a reference design (for CPU and FPGA) to kick-start prototyping with this platform.

The maximum power consumption of the whole board can be maximum 20W, depending on the utilization of the FPGA fabric and the complexity of the software applications running on the processing system. Suitable passive and active cooling precautions shall be put in place to support thermal conduction measures for the target application.

2 Installation

The URP can be delivered as a board or as a development kit. The bare board is intended for integration by the customer in his own application. The development kit is intended for evaluation and prototyping purposes.

2.1 URP Bare board

2.2 Development kit

The development kit delivers all the peripherals to start developing with the URP right away. This includes power supplies, debug extension board, the HMI interface board as well as a BLDC motor and power stage and 2 MIPI camera's. Also the antenna's for the WiFi/BT and GPS are included as well as the USB 3.0 adapter. The development kit is used as basis for the reference designs.

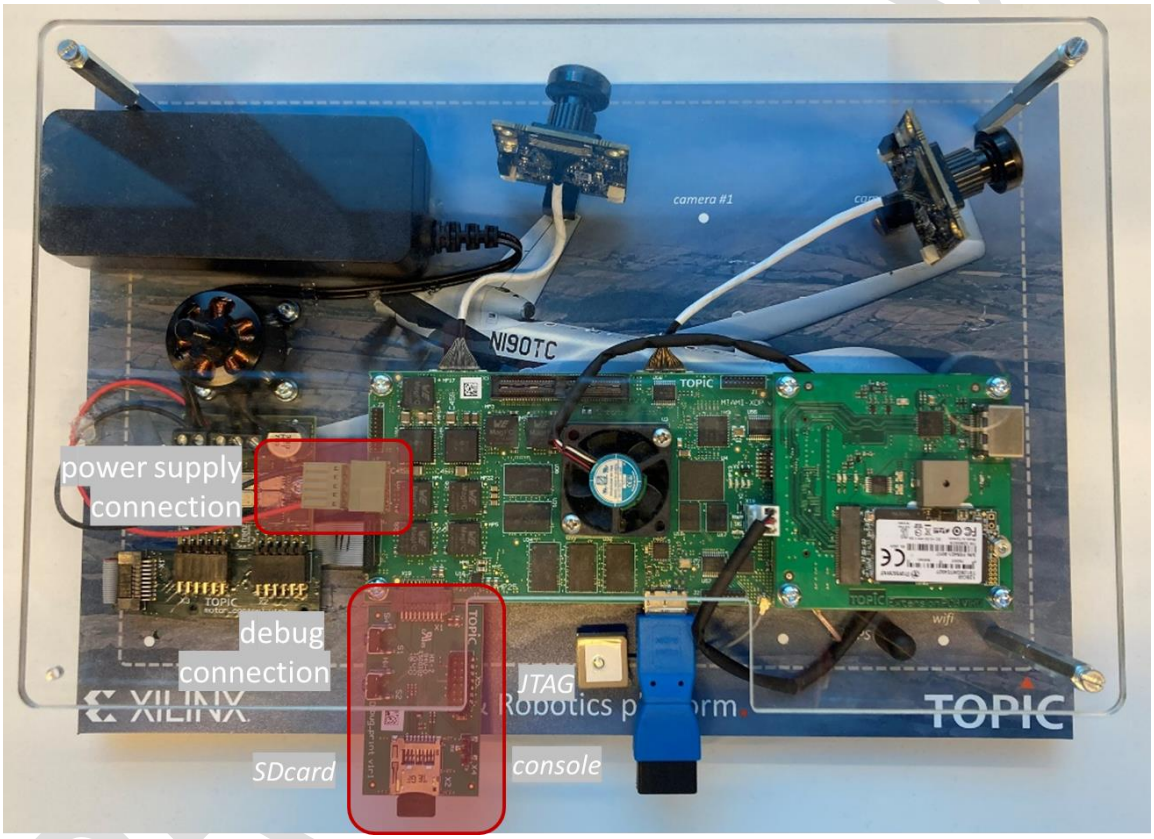
Warning: the URP is an ESD sensitive device. Although the board is designed to withstand ESD discharges on the interfaces, it still needs to be handled carefully with respect to ESD.

2.3 Getting started

The URP needs only a 12[Vdc] power supply or a 3S LiPo battery pack. The development kit comes with a 12[Vdc] mains adapter. When working with the bare board, a accessory pack is recommended, containing an adapter with the board compatible connector.

The board does not contain an on/off switch. When powered, the board is operational.

Because of the high board density and the intended use, the debug features are not integrated on the board, but made available using a debug extension board. This debug board is used to boot the URP from SDcard, connect to a JTAG debugger and connect with the default console interface.



Because of the rough environment where the board is applied in, the debug board should not be applied there. The application software shall be booted after deployment from the on-board eMMC NAND flash memory, the QSPI NOR flash memory. The recommended way of booting the device is use the NOR flash memory for the bootloader (Uboot) and the OS/root file system from the eMMC. Remind that the HDMI extension board allows the use of a large SSD. For logging large data sets, this memory is recommended for that use.

2.4 Software installation

The Miami URP comes with a Linux distribution, which can be downloaded from GitHub:

https://github.com/topic-embedded-products/topic-platform*

This is an easy starting point for developing your own applications. When accessing this website, you are guided through the steps to download, install and start using the software*. The Linux distribution contains:

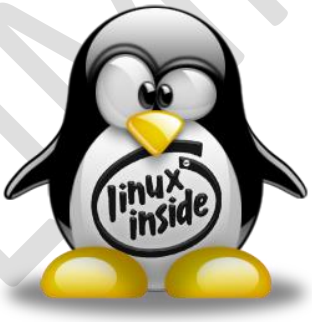
- Linux configuration and development tools
- Cross compiler for the Zynq MPSoC/Cortex-A53 processor
- BSP with drivers for all peripherals on URP
- Simple example program for getting started

Part of the distribution is a program to load the FPGA image from the file system in the NOR or SD-card flash memory. Therefore you are not required to use Xilinx Hardware Manager via the JTAG chain to download FPGA images or boot them from a storage device.

The Miami URP is not dependent on versions of Vivado tooling. However, example FPGA images are available for Vivado 2019.1 and higher.

For any help or support, please contact us at support@TopicEmbeddedProducts.com.

*) Topic-platform contains an README file which is generic for more boards. To build for the URP board use ‘URPzu7’ for the MACHINE environment variable.



3 URP features

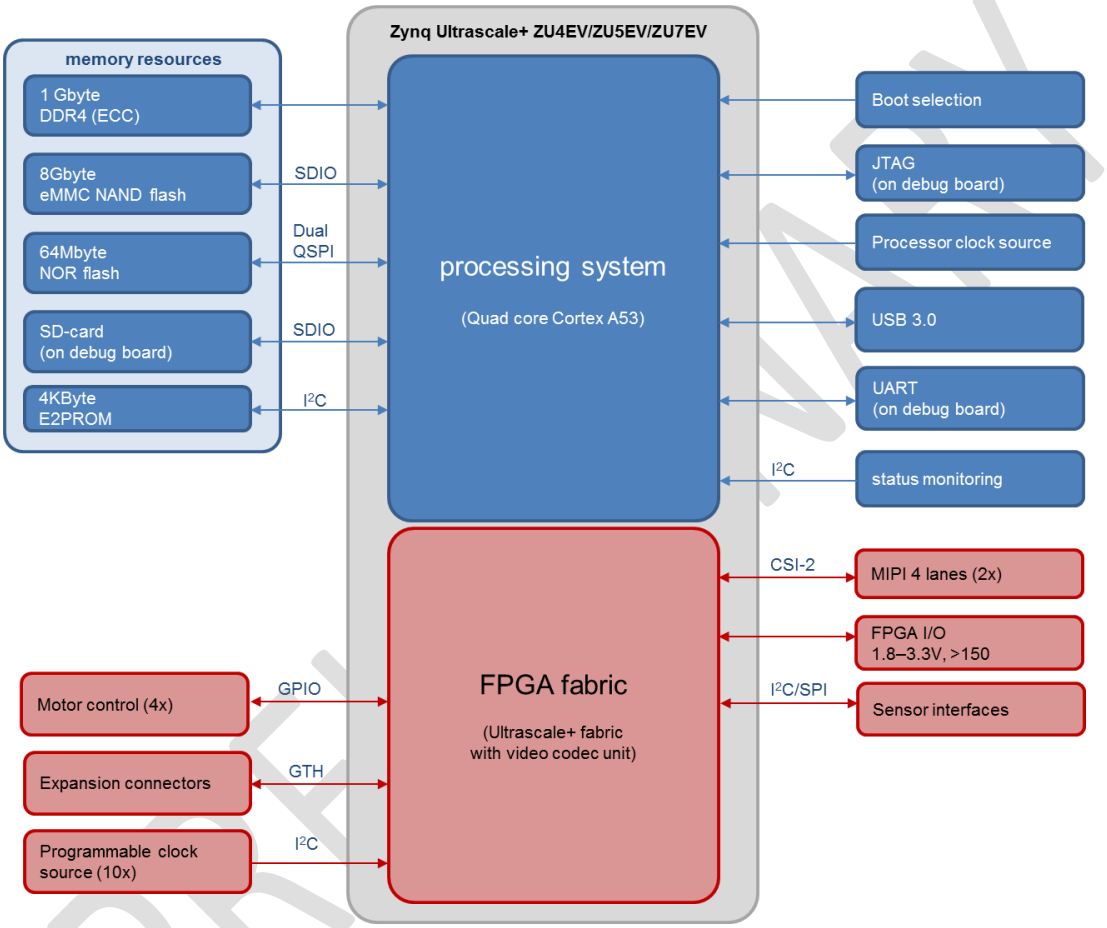
PROCESSOR SYSTEM	
Application Processor [1)]	XCZU7-EV-FBVB900
CPU Architecture	ARM Cortex-A53 (quad core)
CPU Performance	Up to 1.5GHz
Real Time Processor	ARM Cortex R5 (dual core)
Graphics Processor	ARM Mali™-400
Cache (Application processor)	L1: 32KB I / D per core, L2: 1MB, on chip memory 256KB
Cache (Real time processor)	L1: 32KB I / D per core, tightly coupled memory 128KB per core
Cache (Graphics processor)	64K
PROGRAMMABLE LOGIC	
Technology	Ultrascale+®
Logic cells	804K
LUTs	230K
Flip Flops	461K
Max distributed RAM	6.2Mb
BRAM	11Mb
UltraRAM	27Mb
DSP slices	1728
PS MGT transceivers	Channel 0 and 1: Routed to expansion connector. Channel 3: USB3.0
PL MGT transceivers (GTH)	Quad 0, 1, 2: Routed to expansion connectors. Quad 3: Unconnected.
Video Codec Unit	1
MEMORY	
SDRAM [1)]	4GB DDR4 with ECC (72 bit)
NOR [1)]	Dual Quad-SPI, 64MB
eMMC [1)]	8 GByte
Communication interfaces	
WiFi / Bluetooth	Murata LBEE5KL1DX
On board sensors	
Accelero/Gyro sensor	Bosch BMI088
Magneto sensor	Bosch BMM150
Environmental sensor	Bosch BME680
GPS	uBlox ZOE-M8B-0
Connectors	
Rincon Raptor board connection	Samtec QTH-060
Scalable connection (multiple URP)	Samtec QSH-060
Expansion IO (General purpose)	Samtec QSH-060
Motor interface (4x)	Wurth 62202021121
Power supply	
Input	12V adapter / 3S 11.1V Lipo battery
Output	
Software	
Bootloader / BSP	U-Boot
Boot options	JTAG, eMMC, SD-Card (external)
Operating System	Topic Linux 4.x distribution on GitHub
Dyplo® compatible platform	Yes
Mechanical and environmental	
Dimensions	135mm x 68mm
Temperature	

[1)] *Other configurations possible at higher volumes.*

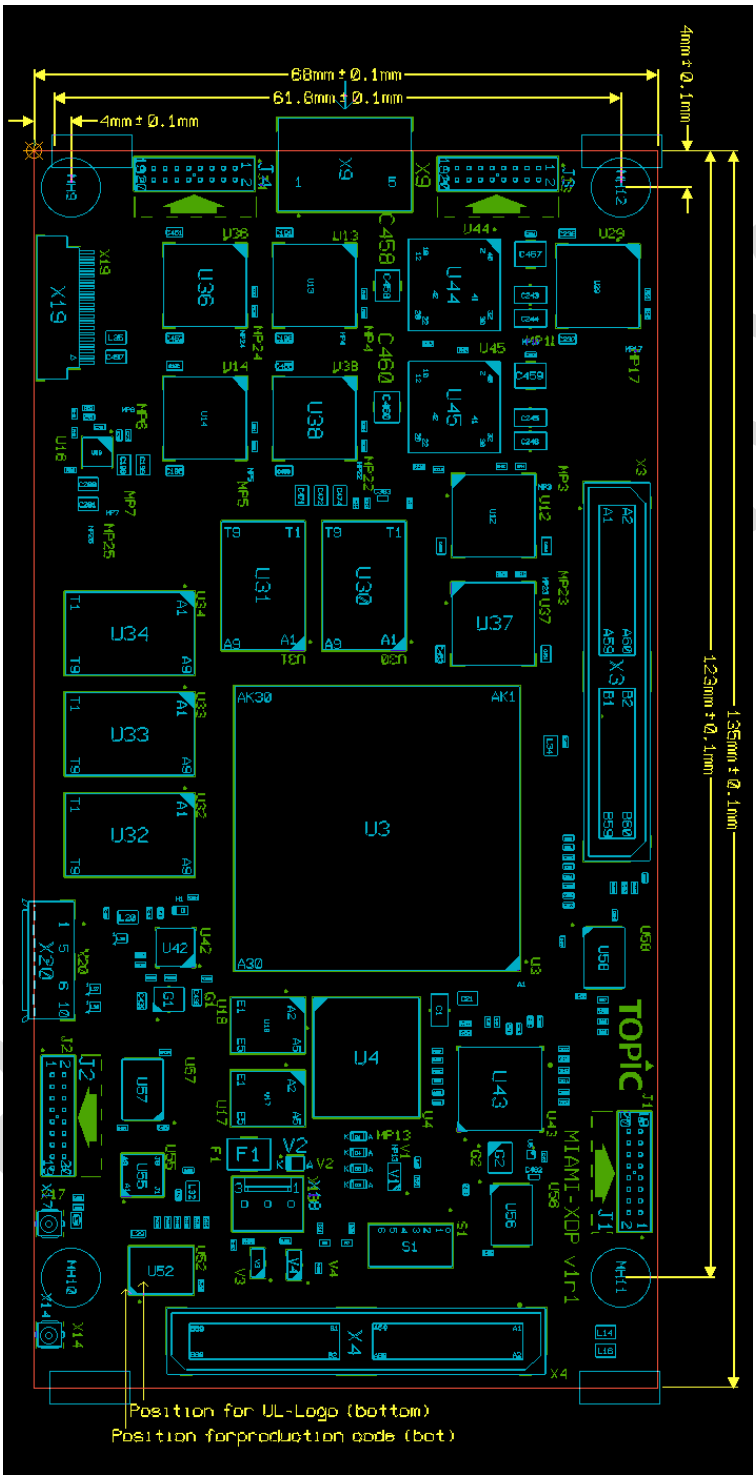
4 URP architecture

The Miami System-on-Module integrates all peripherals to bring up a full functional processing system. The SoM connects to the carrier board using two high performance connectors. The following paragraphs give an overview of peripherals and devices which determine the functionality of the board.

4.1 Block diagram



4.2 URP board layout



5 URP functionality

The functionality of the URP module can be divided in different function groups:

- Configuration and debug interfaces
- Memory resources
- Communication interfaces
- Miscellaneous functionality
- Power supplies and system integrity

In the following paragraphs the functions will be explained from a user perspective to help understand the context to use and program the functionality.

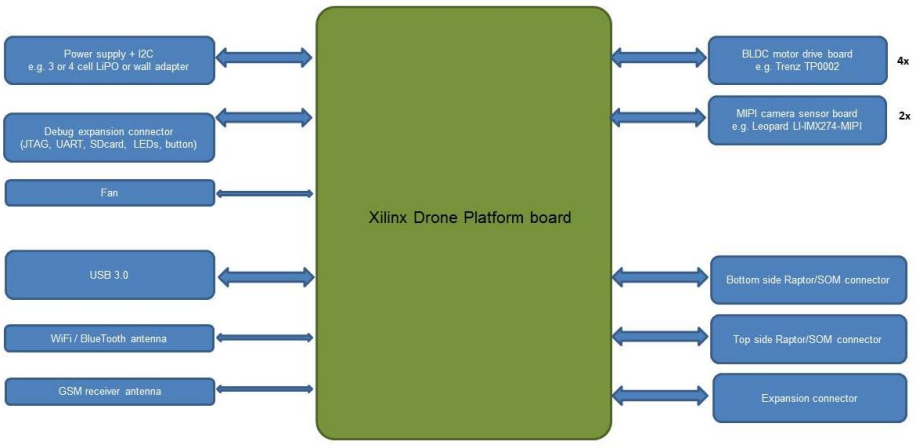


Figure 5.1 Connector interface overview URP board

Figure 5.1 illustrates the cabling interfaces of the URP board. The number of connectors is relatively high as the main purpose of the board is processing, where specific functions are left off the board as the applicable sensors and actuators (e.g. motors and cameras) require space and/or or specific physical location on the drone or UAV. As the URP is focusing on the core functionality of the drone (motor control, auto-pilot, sensors for basic flight control, communication), it is expected that more processing power is required for in-flight data processing. Therefore an infrastructure is in place to couple multiple URP boards, software defined radio boards and other, user defined boards. This can be accomplished using cabling connections as well as ridged connector connections.

Figure 5.2 gives a block diagram overview of all the functions on the URP board and their basic interconnect. In the paragraphs of this document the functionality and usage of these functions are explained.

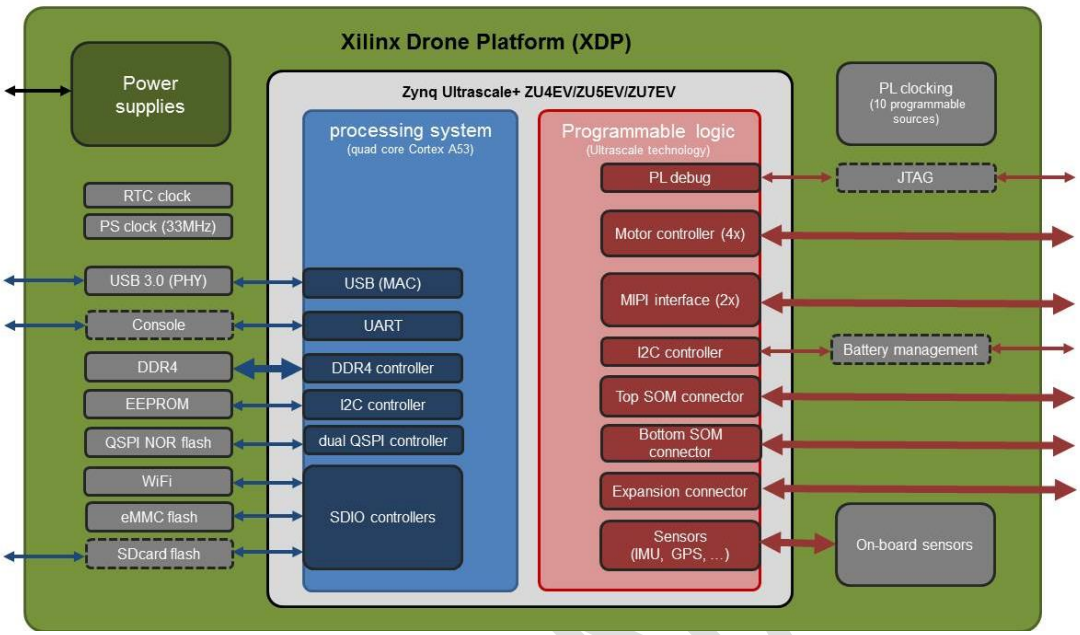


Figure 5.2 Block diagram overview of functions of the URP board

5.1 Configuration and debug interfaces

The configuration and debug interface of the URP consists of the following functionality:

- Configuration and boot switches
- Status LEDs
- JTAG interface *(via expansion board)*
- Hardware version ID
- UART console interface *(via expansion board)*
- Reset buttons *(via expansion board)*

5.1.1 Debug expansion header

The space on the URP board is limited. For this reason the debug interfaces, which are not needed as part of the operational functionality, are provided on a separate board. The signals to this debug board are provided via a 20 pins board-to-board connector. The following functionality and pin-out on the debug header are applicable:

Connector reference		(X19) Debug expansion header	
Connector type			
Pin	**Label**	**FPGA pin**	**Description**
1	+3V3	-	
2	GND	-	
3	JTAG_RST	-	
4	JTAG_TMS	L21	
5	JTAG_TDI	L20	
6	JTAG_TDO	M20	
7	JTAG_TCK	L19	
8	PS_SRST_B	P20	
9	JTAG_VREF	-	
10	GND	-	
11	CONSOLE_TXD	A18	
12	CONSOLE_RXD	B18	
13	uSD_DETECT	F23	
14	SD_CMD	J20	
15	SD_CLK	H21	
16	SD_DQ0	K20	
17	SD_DQ1	K21	
18	SD_DQ2	J21	
19	SD_DQ3	G21	
20	GND	-	

Figure 5.3 Pinout debug expansion header

5.1.2 Configuration and boot switches

The URP board implements a 6 position micro dipswitch. Three switches are used to select the boot mode configuration of the first stage bootloader. The behavior of the switches is specified by the Zynq Ultrascale+ silicon. The three other switches are connected to MIO pins of the processor. They are user configurable and can be used for application specific configuration settings. Using the Linux kernel configuration and bootloader of Topic, the switches are used to select from which memory the Linux kernel shall be booted.

Reference		(S1) Configuration and boot selection switches	
Switch	**Label**	**FPGA pin**	**Description**
1	PS_MODE0	R18	The dip switches control the state of the FPGA boot mode selection
2	PS_MODE1	R19	signals, located on the FPGA on pin T22 (PS-MODE0), R22 (PS_MODE1),
3	PS_MODE2	P21	T23 (PS-MODE2) and R23 (PS_MODE3). These are only used during
4	PS_USER_SW0	F21	Input to PS
5	PS_USER_SW1	D22	Input to PS
6	PL_USER_SW0	W8	Input to PL

Figure 5.4 Pinout configuration switches

The URP board first stage bootloader can be booted from the QSPI connected NOR flash, the SD-Card, the eMMC memory or via the JTAG chain. Further booting e.g. via u-boot, can be selected e.g. using the user defined switch settings.

5.1.3 Status LEDs

There are 4 status LEDs provided on the URP board. The LEDs are intended to have rapid insight in the state of the board. The following table explains the characteristic settings:

Reference		LED indicators	
LED	**Label**	**FPGA pin**	**Description**
D4	PS_DONE	N22	FPGA NOT configured indication (red)
D1	LED_USER1	AD15	FPGA alive blinking (Topic reference design) (green)
D5	LED_KERNEL_ALIVE	B20	CPU alive blinking (Topic Linux kernel) (green)
D3	POWER_GOOD	-	Status indication board power supplies all within range (green)

Figure 5.5 Assignment LEDs on the URP board

5.1.4 JTAG interfaces

The standard 14 pins boxed header for JTAG connectivity occupies too much space on the board. Therefore it is implemented on the debug expansion header interface. The JTAG chain of the board can be accessed via e.g. Diligent JTAG cables, of which one is part of the development kit. *Refer to appendix A for a detailed description on the debug expansion header.*

5.1.5 Hardware version ID

The FPGA I/O of the Zynq Zynq Ultrascale+ is not exhausted. Therefore, 4 pins are reserved to read back the board hardware status. This is a pull-down resistor network that also makes use of the internal pullup resistors. Using the network a total of 16 board revision IDs can be configured. This is a read-only configuration, assembled during production, starting with binary version 0x0h.

Reference		Board version ID	
Resistor	**Label**	**FPGA pin**	**Description**
R97	VERSION0	AA2	Board version ID number. Starting with version ID 0h0.
R98	VERSION1	AE4	
R99	VERSION2	AD4	
R100	VERSION3	AE5	

Figure 5.6 HW version ID resistors URP board

5.1.6 UART console interface

The primary software development interface is the console connection with the processing system. The URP board provides a fixed UART console connection directly on the MIO port of the processing system. The console interface is logically compatible with a standard FTDI TTL UART cable, which is part of the development kit. *Refer to appendix A for a detailed description on the debug expansion header.*

5.1.7 Reset buttons

The URP board can be reset in a number of ways. The following reset conditions are identified:

- Power-on reset. When applying power to the board, a defined power sequence scheme is executed. When all relevant supplies are powered, the reset is de-asserted after a few milliseconds.
- Board reset. This is a reset button connected to the debug expansion header. Asserting this button will reset the complete board, including FPGA pin “PS_POR_B”, “PS_INIT_B” or “PS_PROG_B”.
- FPGA initialization reset. This is a reset applied by the JTAG chain. It asserts the FPGA pin “PS_POR_B”, “PS_INIT_B” or “PS_PROG_B”.
- Software reset. This will reset only the processing system. It is asserted with a specific pin on the JTAG connector or by means of a switch on the debug expansion header. *Refer to appendix A for a detailed description on the debug expansion header.*

5.2 Memory resources

The URP board makes use of different memory resources with different usage:

- DDR4 SDRAM for fast volatile memory purposes
- NOR flash memory for fast and reliable booting
- eMMC flash memory for mass storage
- SDcard SDIO flash memory for mass storage especially during development
- I2C connect EEPROM for parameter storage

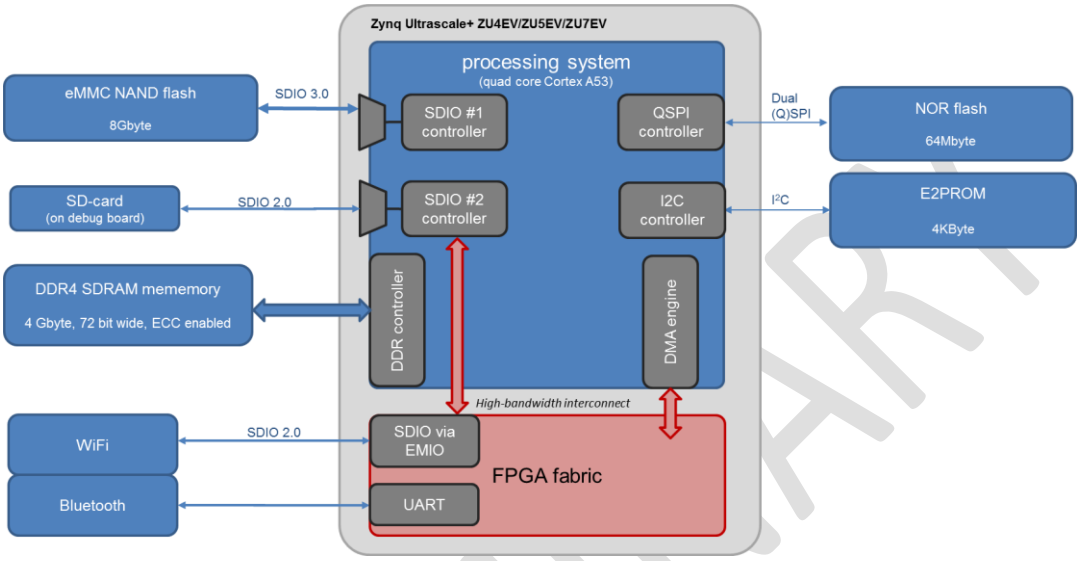


Figure 5.7 Block diagram overview of memory resources

5.2.1 DDR4 SDRAM memory (MT40A512M16GE-083E IT:B)

A DDR4 SDRAM memory solution is provided as the main background memory. The RAM memory has a 72-bit interface and can be clocked up to 2400 [MHz]. The DDR clock frequency is configured by the software configuration .The size of the DDR4 SDRAM memory is 4GB. The memory solution enables the use of ECC, making it suitable for high-altitude applications or where reliability of data content is required. Using the 72 bit wide memory interface, a theoretical memory data transfer rate of 18Gbyte/sec is possible. Effectively, 10Gbyte/sec is a practical number to calculate with.

The memory is shared between the processing system and the programmable logic. Due to the form factor of the URP platform as well as the power consumption, no dedicated memory was assigned to the programmable logic. For exploring the capabilities of the embedded video compression/decompression unit on the board, the memory bandwidth is sufficient. *Refer to implementation design rules for the VCU to the appropriate background material of Xilinx using the Document Navigator of Vivado*.

The solution is build using 5 16-bit wide DDR4 SDRAM memory chip (Micron MT40A256M16GE). The devices are connected to the dedicated DDR memory controller interface on the Zynq Ultrascale+.

5.2.2 Dual quad SPI NOR flash memory (MT25QU256)

The dual on-board QSPI NOR flash memories offers a reliable boot memory source with sufficient storage capacity to hold a moderate embedded Linux distribution. However, the primary goal is to hold the first stage bootloader as this is the fastest and most reliable memory source on the board. The URP board applies two Micron MT25QU256 devices, offering a total storage capacity of 64[MB].

The URP assigns the NOR flash to fixed processing system MIO pins. The following table describes which pins are being used by the QSPI controller.

Reference		Dual QSPI NOR flash memory	
Device reference		2x MT25QU256	
Pin	**Label**	**FPGA pin**	**Description**
QSPI1_DQ0	PS_MIO4	J17	
QSPI1_DQ1	PS_MIO1	A20	
QSPI1_DQ2	PS_MIO2	B19	
QSPI1_DQ3	PS_MIO3	D19	
QSPI1_CLK	PS_MIO0	H17	
QSPI1_CS	PS_MIO5	C19	
QSPI2_DQ0	PS_MIO8	E20	
QSPI2_DQ1	PS_MIO9	F20	
QSPI2_DQ2	PS_MIO10	F18	
QSPI2_DQ3	PS_MIO11	G18	
QSPI2_CLK	PS_MIO12	H18	
QSPI2_CS	PS_MIO7	E19	

Figure 5.8 Pin assignments dual QSPI NOR 64 MB flash

5.2.3 eMMC memory (Sandisk SDINBDG4-8G)

The URP board provides 8GByte of eMMC memory connected to the MIO SDIO interface as external storage device or as a boot source. The benefit of this flash memory is the mechanical stability on the board compared to SD card based flash memory as well as the very high data performance. The memory's interface is a SDIO 3.0 interface and is connected to fixed processing system MIO pins. The following table describes which pins are being used for the eMMC SDIO controller. *Refer to the datasheet of the SDINBDG4-8G regarding information how to use this device.*

Reference		eMMC NAND flash memory	
Device reference		SDINBDG4-8G	
Pin	**Label**	**FPGA pin**	**Description**
SDIO_eMMC_CLK	PS_MIO22	F17	
SDIO_eMMC_RESET	PS_MIO23	K19	
SDIO_eMMC_CMD	PS_MIO21	H19	
SDIO_eMMC_DQ0	PS_MIO13	G19	
SDIO_eMMC_DQ1	PS_MIO14	E18	
SDIO_eMMC_DQ2	PS_MIO15	J19	
SDIO_eMMC_DQ3	PS_MIO16	K17	
SDIO_eMMC_DQ4	PS_MIO17	C18	
SDIO_eMMC_DQ5	PS_MIO18	K18	
SDIO_eMMC_DQ6	PS_MIO19	K16	
SDIO_eMMC_DQ7	PS_MIO20	A19	

Figure 5.9 Pin assignments 8Gbyte eMMC NAND flash memory

5.2.4 SD-card memory interface

The URP board can boot from the SD-card interface on the debug expansion header. This allows the use of over 64Gbyte of NAND flash memory as mass storage. When applying SD-cards, be aware of quality differences. Cheaper SD-cards may result in corrupted file systems when not properly unmouted before powering down.

The SD-card interface is connected directly to the MIO pins of the PS part of the Zynq Ultrasacale+. As there are a total of three SDIO resources defined on the Zynq and only two simultaneously applied, the SD-card is connected to two pin locations on the processor. This gives the flexibility to switch between the combinations of Wifi/Bluetooth, eMMC memory and SD-card flash including selection of the primary boot source. For instance, the user defined switch positions can be used to detect the desired configuration.

Reference		Sdcard interface	
Device reference			
Pin	**Label**	**FPGA pin**	**Description**
uSD_CLK	PS_MIO51	H21	SDIO interface on the PS part of the Zynq Ultrascale+
uSD_CMD	PS_MIO50	J20	
uSD_DQ0	PS_MIO46	K20	
uSD_DQ1	PS_MIO47	K21	
uSD_DQ2	PS_MIO48	J21	
uSD_DQ3	PS_MIO49	G21	
uSD_DETECT	PS_MIO45	F23	

Figure 5.10 Pin assignments SD card interface

5.2.5 EEPROM memory (M24C32S-FCU)

The URP provides a 32Kbit I²C connected EEPROM device for storing parameters and other configuration and user settings. This device is connected to the URP system I²C bus, accessible via the following MIO pins of the processor system. *Refer to the datasheet of the M24C32S-FCU regarding information how to use this device. Be aware that 16 highest address words of the 512 available words are reserved by the system for the serial number and administrative parameters. Do not overwrite this data.*

Reference		I2C EEPROM parameter storage (U6)	
Device reference		M24C32S-FCU, I2C address 0x51	
Pin	**Label**	**FPGA pin**	**Description**
SCL_1V8	PS_MIO74	E29	
SDA_1V8	PS_MIO75	D29	

Figure 5.11 Pin assignments EEPROM memory

5.3 Sensor and actuator interfaces

The URP board implements a number of sensors and actuators required to make a drone platform perform as a drone platform. These peripherals are:

- 4 brushless DC motor controller actuator interfaces
- 2 MIPI high-resolution camera sensor interfaces
- 3D accelerometer sensor
- 3D gyroscope sensor
- 3D magnetic field sensor
- GPS localization sensor
- Temperature sensor
- Humidity sensor
- Pressure sensor

Apart from these interfaces, a drone can make use of more sensors, such as radar, lidar and ultrasound for example. A dedicated expansion header is provided to support customized extension of the URP board.

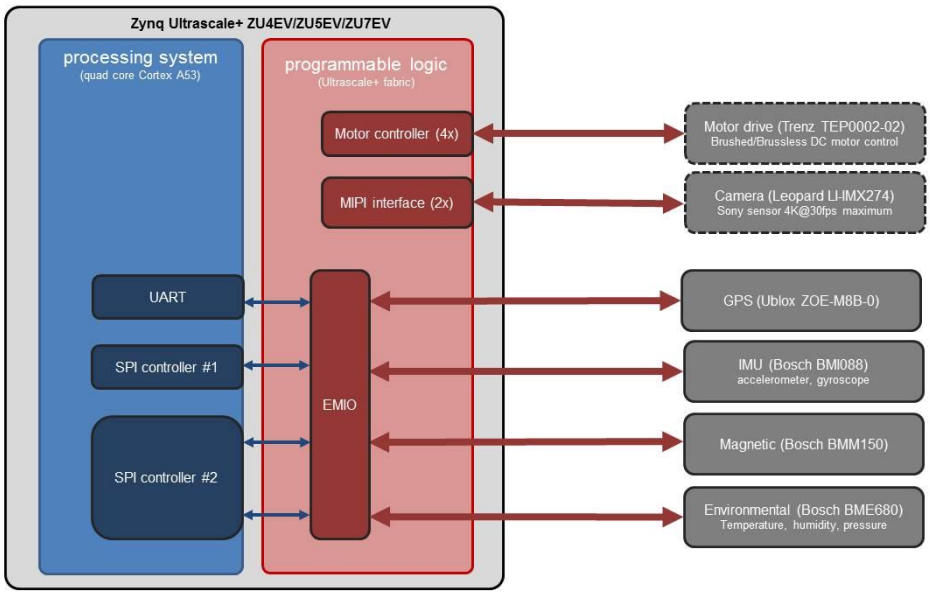


Figure 5.12 Block diagram description sensor interface

5.3.1 4 brushless DC motor controller actuator interfaces

The URP board implements the control centrally of 4 brushless DC motors. The FPGA fabric allows very accurate control loops to perform the commutation of the motors. Apart from commutation the stator/rotor position needs to be determined. As motor drives and interfaces vary, the URP foresees in generic motor control signals and readback

An example of an available driver board for brushless DC motors is the Trenz-Electronic TEP0002 board. The board accepts 3V3 logic signals via 2 PMOD connectors. When driving 4 motors, 4 of these boards are required. Interfacing 8 PMOD interfaces is not an option. Therefore it is needed to have an interface board that connects 14 3V3 signals via a small form factor connector from the URP board to a dual PMOD adapter board. The signals from/to the motor control PCB are buffered and level converted to the right logic level and drive.

The SPI clock speed for reading the back EMF signal levels back are limited to 40MHz. Typical control of the H-bridges is putting the high side drive permanently and switch the lower side of another half bridge to induce a sine wave. Assuming a rotor rotation speed of maximum 20.000 RPM < 350 RPS and 4 pole pairs per revolution, a harmonic signal of 1500 Hz must be created using PWM. Assuming 10 stable PWM periods per sample and 10 bits PWM resolution, the PWM clock frequency is still less then 20MHz.

Connector reference		(J1-4) Motor interface header				
Connector type		WURTH 62202021121				
Pin	Motor	FPGA pin (M0)	FPGA pin (M1)	FPGA pin (M2)	FPGA pin (M3)	Description
1	+3V3	-	-	-	-	
2	GND	-	-	-	-	
3	PWM_CH0	A14	A17	E13	D15	
4	EN_CH0	A13	C16	F12	J14	
5	PWM_CH1	B14	C17	E12	D16	
6	EN_CH1	B12	A16	F13	K15	
7	PWM_CH2	C14	D17	D14	E17	
8	EN_CH2	A12	B16	G14	G15	
9	GND	-	-	-	-	
10	SENSOR_FAULT	AA8	AD9	G13	J15	
11	GND	-	-	-	-	
12	ADC_CH	AA7	AC9	H12	G16	
13	ADC_SCK	Y7	Y10	D12	E15	
14	ADC_CS	AC8	AD7	H13	H16	
15	ADC0_DO	Y8	AA10	C13	F15	
16	ADC1_DO	AC7	AB8	H14	J16	
17	ADC2_DO	AD6	AE7	C12	F16	
18	ADC3_DO	AC6	AB6	E14	K14	
19	GND	-	-	-	-	
20	+3V3	-	-	-	-	

Figure 5.13 Connector pinout motor control interface 4x

5.3.2 2 MIPI high-resolution camera sensor interfaces

The URP provides 2 MIPI interfaces in the form of support for a Leopard LI-IMX274-MIPI connector. Via the 30 pins I-PEX connector all signals required to drive the Sony IMX274LQC image sensor are provided, offering a maximum resolution of 4K@30fps. This is a limitation of the applied sensor. The FPGA and related IP blocks are capable of supporting sensors with capabilities of e.g. 4K@60fps. The connector defines additional signals for controlling e.g. flash light and lens motors to facilitate autofocus. The interface is logically driven by 1V8 logic and power using a 3V3 source.

The clock to the MIPI board is driven by an FPGA pin. This gives the flexibility to drive the MIPI camera sensor with a flexible clock frequency.

The I2C bus is used to configure the image sensor. The Linux driver configuring the camera is depending on the applied sensor. For the IMX274LQC the driver provided by Leopard, will be part of the Linux BSP that comes with the URP board.

To interface with a MIPI camera, Xilinx is offering the MIPI CSI-2 Controller Subsystems (part numbers EF-DI-MIPI-CSI-RX-SITE and EF-DI-MIPI-CSI2-TX-SITE), providing both receiving and transmitting capabilities. The physical interface on the URP board allows the usage of both, but it is designed and tested to support camera inputs. Using the IP block in the FPGA will result in an AXI4-Stream compatible video pixel stream to be used as needed, e.g. for stereo vision.

Reference		MIPI camera connector 1 AND 2			
Device reference		Leopard LI-IMX274-MIPI (Sony IMX274LQC image sensor)			
Pin	**Label**	**FPGA pin MIPI#0**	**FPGA pin MIPI#1**	**Level/technology**	**Description**
1	MIPI_D3P	AB10	AB1	LVDS	MIPI CSI-2 or sub -LVDS interface signals. Data is configured via the CAM_SCL/CAM_SDA port. The connector is compatible with the Leopard LI-IMX274-MIPI camera. These signals are directly connected to the Sony IMX274LQC image sensor.
2	MIPI_D3N	AB9	AC1	LVDS	
3	MIPI_D1P	AB11	AC3	LVDS	
4	MIPI_D1N	AC11	AC2	LVDS	
5	GND	-	-	GND	
6	MIPI_CP	AC12	AD2	LVDS	
7	MIPI_CN	AD12	AE2	LVDS	
8	MIPI_D0P	AA12	AD1	LVDS	
9	MIPI_D0N	AA11	AE1	LVDS	
10	MIPI_D2P	AD11	AA3	LVDS	
11	MIPI_D2N	AD10	AB3	LVDS	
12	TEST4	-	-	-	Not connected
13	CAM_SCL	AE14	AD14	1V8 CMOS	I2C clock, e.g. IMX274LQC sensor
14	CAM_SDA	AE13	AA14	1V8 CMOS	I2C data, e.g. IMX274LQC sensor
15	CAM_RST	AA13	AB14	1V8 CMOS	Reset signal for IMX274LQC sensor
16	CLK	AC14	AB15	1V8 CMOS	1V8 level clock for IMX274LQC sensor
17	FLASH_EN	AB13	AA15	1V8 CMOS	To flash control board (for Leopard board)
18	TEST3	AA6	AE3	1V8 CMOS*	To lens control board (for Leopard board)
19	TEST2	AA5	Y1	1V8 CMOS*	To lens control board (for Leopard board)
20	TX1_GPIO2	-	-	-	Not connected
21	TEST1	AB4	W9	1V8 CMOS*	To lens control board (for Leopard board)
22	TX1_GPIO1	AC4	AA1	1V8 CMOS*	To lens control board (for Leopard board)
23	V_1.2V	-	-	-	Not connected
24	V_1.2V	-	-	-	Not connected
25	V_1.8V	-	-	-	Not connected
26	V_2.8VA	-	-	-	Not connected
27	V_5.0V	-	-	-	Not connected
28	V_3.3V	-	-	3V3 supply	Supply for MIPI camera
29	V_3.3V	-	-	3V3 supply	
30	V_3.3V	-	-	3V3 supply	

*) IOSTANDARD on MIPI connector. On the board these pins are level-translated to 1V2 CMOS

Figure 5.14 Connector pinout MIPI interface 2x

5.3.3 3D accelerometer sensor/3D gyroscope sensor (BMI088)

For operating a drone, it is required to have enough accurate sensors available to compensate for movements, both intended and unintended. The BMI088 of Bosch Sensortech is especially developed for drone applications. It integrates both a 3D accelerometer and gyroscope with 16 bit accuracy and a measurement bandwidth of over 500Hz. At a maximum acquisition rate of 2KHz, reading 6 values of 16 bit each, the required bandwidth is 200kbit/second. For this reason, the interface with the FPGA is chosen to be SPI to anticipate higher throughput rates.

Reference		I2C Accelerometer/Gyroscope sensor	
Device reference		BMI088, SPI operated	
Pin	**Label**	**FPGA pin**	**Description**
CSB1	IO_L18N_T2U_N11_AD2N_64	AE19	Chip select accelerometer
CSB2	IO_L19P_T3L_N0_DBC_AD9P_64	AG16	Chip select gyroscope
SD01	IO_L17N_T2U_N9_AD10N_64	AC18	Data output accelerometer
SD02	IO_L17N_T2U_N9_AD10N_64	AC18	Data output gyroscope
SCK	IO_L19N_T3L_N1_DBC_AD9N_64	AH16	SPI clock
SDI	IO_L18P_T2U_N10_AD2P_64	AD19	SPI data input
A_INT0	IO_L21P_T3L_N4_AD8P_64	AH17	Accelerometer interrupt 0
A_INT1	IO_L20P_T3L_N2_AD1P_64	AJ16	Accelerometer interrupt 1
G_INT0	IO_L22P_T3U_N6_DBC_AD0P_64	AK17	Gyroscope interrupt 0
G_INT1	IO_L21N_T3L_N5_AD8N_64	AJ17	Gyroscope interrupt 1

Figure 5.15 Accelerometer/gyroscope sensor connectivity

5.3.4 3D magnetic field sensor (BMM150)

For auto piloting, it is required to have an orientation notion. Compass information can be obtained by measuring the earth magnetic field as well as using the GPS module. A problem with GPS based compasses is that you have to move around to make it work. A geo-magnetic field sensor can assist in this context. Be aware that the field is very weak and metal objects will negatively influence accurate measurements. The location on the board is chosen carefully. The BMM150 sensor of Bosch Sensortech qualified very well for this functionality in terms of size, accuracy and applicability.

Reference		I2C Magnetic field sensor	
Device reference		BMM150, SPI operated	
Pin	**Label**	**FPGA pin**	**Description**
CSB	IO_17P_T2U_N8_AD10P_64	AC17	Chip select
SD0	IO_L24P_T3U_N10_64	AE18	Data output
SCK	IO_L23P_T3U_N8_64	AG18	SPI clock
SDI	IO_L24N_T3U_N11_64	AF18	SPI data input
INT	IO_L22N_T3U_N7_DBC_AD0N_64	AK18	Magneto Interupt
DRDY	IO_L20N_T3L_N3_AD1N_64	AK16	Data Ready

Figure 5.16 Magnetic field sensor connectivity

5.3.5 Temperature, humidity and pressure sensor

When flying around with a drone at different altitudes, apart from direction you may want to know the height you fly, the temperature and humidity. An auto-pilot can increase operational accuracy based on these aspects. Also GPS enhancements are possible. The Bosch Sensortech BME680 integrates these functions in a single device.

Reference		I2C Temperature, humidity and pressure sensor	
Device reference		BME680, SPI operated	
Pin	**Label**	**FPGA pin**	**Description**
CSB	IO_L23N_T3U_N9_64	AH18	Chip select
SD0	IO_L24P_T3U_N10_64	AE18	Data output
SCK	IO_L23P_T3U_N8_64	AG18	SPI clock
SDI	IO_L24N_T3U_N11_64	AF18	SPI data input

Figure 5.18 Temperature, humidity and pressure sensor connectivity

5.3.6 GPS localization sensor

Autonomous flying or moving requires an accurate notion of location. GPS is a must in this case. Depending on the required accuracy, additional measures are required to increase the accuracy. Examples are Galileo, GLONASS, BeiDou. For the URP, the Ublox ZOE-M8B-0 is selected. The module has a battery backup to decrease the first-fix time after a power-down period. This device incorporates already an LNA, allowing the use of a passive antenna.

Reference		GPS localization sensor	
Device reference		ZOE-M8B	
Pin	**Label**	**FPGA pin**	**Description**
SDA/SPI CS_N	IO_T2U_N12_65	AH4	
SCL/SPI CLK	IO_T1U_N12_65	AG9	
PIO11	IO_L24P_T3U_N10_PERSTN1_I2C_S	AF3	
PIO15	IO_L22P_T3U_N6_DBC_AD0P_65	AG4	
PIO14	IO_L22N_T3U_N7_DBC_AD0N_65	AG3	
PIO13/EXTINT	IO_T0U_N12_VRP_65	AE10	
RXD/SPI MOSI	IO_L23P_T3U_N8_I2C_SCLK_65	AG1	
TXD/SPI MISO	IO_L23N_T3U_N9_65	AH1	
RESET_N	IO_T3U_N12_65	AF1	
D_SEL	IO_L24N_T3U_N11_PERSTN0_65	AF2	

Figure 5.17 GPS sensor connectivity

5.4 Communication interfaces

The communication interfaces on a drone are limited to wireless connectivity and generic expansion interfaces. The following connectivity is implemented:

- USB 3.0
- WiFi/Bluetooth

A long range radio connection has to be established by using the expansion connector equipped with a radio module or using the Raptor software defined radio.

5.4.1 USB 3.0

The USB 3.0 interface makes use of the dedicated USB 2.0 OTG MAC of the Zynq Ultrascale+ in combination with one pair of GTR transceivers of the PS. The Zynq's interface is connected to a USB PHY, the USB3343-CP from SMSC. This PHY uses a 26MHz X-tal to create the required clocks for the PHY. The pin mapping is described in the table below.

Reference		USB 3.0	
Connector		X20	
Device reference		U42	
Pin	**Label**	**FPGA pin**	**Description**
22	USB_RESET	D25	USB PHY Reset
12	USB_DQ7	A29	USB PHY Databus bit 7
11	USB_DQ6	B28	USB PHY Databus bit 6
10	USB_DQ5	B29	USB PHY Databus bit 5
8	USB_DQ4	C25	USB PHY Databus bit 4
7	USB_DQ3	A27	USB PHY Databus bit 3
6	USB_DQ2	A23	USB PHY Databus bit 2
5	USB_DQ1	A26	USB PHY Databus bit 1
4	USB_DQ0	A25	USB PHY Databus bit 0
24	USB_STP	A28	USB PHY, stops data stream
3	USB_NXT	B26	USB PHY, current byte has been accepted
1	USB_DIR	B25	USB PHY, databus direction
2	USB_CLK	A24	USB PHY Clock output to MAC
-	USB_RXD_GTX_P	H27	USB GTR RX_P
-	USB_RXD_GTX_N	H28	USB GTR RX_N
-	USB_TXD_GTX_P	J25	USB GTR TX_P
-	USB_TXD_GTX_N	J26	USB GTR TX_N

Apart from the above signals for the PHY, the OTG functionality is controlled via the I2C bus. The bus voltage (5V) can be enabled by making USB_OTG_EN_N low and in case there is an over current situation, this is indicated via USB_OTG_OC_N going low (see chapter **Error! Reference source not found.**). Once there is 5V present on Vbus, a green LED right behind the USB connector will light up.

5.4.2 Wifi/Bluetooth

The Miami URP features a combined WLAN and Bluetooth wireless module. This module, the LBEE5KL1DX module from Murata, features an external antenna connected via the UFL connector.

Reference		Bluetooth / Wifi	
Device reference		U52	
Pin	**Label**	**FPGA pin**	**Description**
28	IO_L6N_T0U_N11_AD6N_64	AE15	Wifi Enable
27	IO_L16P_T2U_N6_QBC_AD3P_64	AA16	Wifi wake
24	IO_L16N_T2U_N7_QBC_AD3N_64	AB16	SDIO Data 0
26	IO_T1U_N12_64	AF13	SDIO Data 1
23	IO_T2U_N12_64	AC19	SDIO Data 2
5	IO_T0U_N12_VRP_64	AC13	SDIO Data 3
22	IO_T3U_N12_64	AG19	SDIO Command
20	IO_L7P_T1L_N0_QBC_AD13P_64	AG13	SDIO Clock
14	IO_L15N_T2L_N5_AD11N_65	AK6	Bluetooth enable
29	IO_L7N_T1L_N1_QBC_AD13N_64	AH13	Bluetooth wake
3	IO_L8N_T1L_N3_AD5N_64	AK12	UART TX from device
2	IO_L9P_T1L_N4_AD12P_64	AJ14	UART RX to device
5	IO_L8P_T1L_N2_AD5P_64	AK13	UART RTS from device
4	IO_L9N_T1L_N5_AD12N_64	AK14	UART CTS to device

The Zynq Ultrascale+ contains 2 embedded SDIO controllers. Both controllers can be used for booting the processor system. In this case it is bound to be connected to a particular set of MIO pins. When it is not required to boot from an SDIO connected SD-card image/eMMC memory, both SDIO controllers can be accessed via the MIO processor pins or via the FPGA fabric. Be aware that the use of SDIO interface via FPGA fabric requires specific design constraints for proper operation. IP blocks covering this functionality are available via our webshop. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the usage of the SDIO controller refer to Xilinx document UG1085 (Zynq UltraScale+ MPSoC technical reference guide) chapter 26.*

5.5 Miscellaneous resources

There are a number of resources on the board that are required for basic system operation. These are:

- Clocking source processing system
- Clocking sources programmable logic and transceivers
- Crystal for real-time clock

5.5.1 Clocking source processing system

The URP applies a 33.333 [MHz] clock for the processor system. This clock drives the processing system PLL from which all of the required clocks are derived. From this clock also an internal FPGA clock can be derived.

The second clock (200[MHz]) is available for the programmable logic and the third is a user programmable clock. The 200MHz clock and the user configurable clock are differential paired. Based on the PS_CLOCK, the processing system generates the clocks to drive the CPU cores, DDR memory and the bus clock. This clock is also available for the user in the FPGA fabric. The 200MHz clock is especially applicable for clocking the FPGA fabric. The third clock can be programmed through I2C between 100 KHz and 250 MHz.

Clock signal	FPGA pin	FPGA pin label	Description
PS_CLOCK_33MHZ	U24	PS_REF_CLK	33.333 MHz, 20 ppm
CLOCK_FPGA_0_P	AH7	IO_L12P_T1U_N10_GC_65	Programmable: 100 kHz to 250 MHz P, 20 ppm
CLOCK_FPGA_0_N	AJ7	IO_L12N_T1U_N11_GC_65	Programmable: 100 kHz to 250 MHz P, 20 ppm
CLOCK_FPGA_1_P	AH6	IO_L13P_T2L_N0_GC_QBC_65	Programmable: 100 kHz to 250 MHz P, 20 ppm
CLOCK_FPGA_1_N	AJ6	IO_L13N_T2L_N1_GC_QBC_65	Programmable: 100 kHz to 250 MHz N, 20 ppm

5.5.2 I2C connected support peripherals

The following table gives an overview of the involved pins on the Zynq Ultrascale+. The PS I^2C bus is especially intended for user controlled chains on the carrier boards. However, the I^2C controller is also accessible via the EMIO ports via the programmable logic pins. This allows the user to use the involved pins on the MIO for other purposes.

I2C bus signal name	FPGA pin	FPGA pin label
SCL_1V8	E29	PS_MIO74_502
SDA_1V8	D29	PS_MIO75_502

The SYS I^2C has multiple connected peripherals to control and maintain consistent operation of the modules. The devices are available for the user, but care must be taken as certain configurations may harm reliable operation. The following table lists the peripherals integrated as well as the functionality they provide on the board.

I2C peripheral	I2C address	Description
M24C32S-FCU	0b1010000x = 0x51	General purpose EEPROM memory. Refer to the datasheet of the CAT24C04 for information how to access this device.
SI5341D	0b1110100x= 0x74	Programmable I2C XO. Refer to the datasheet of the Si5341 for information how to access this device.

5.5.3 Real Time Clock

The Zynq Ultrascale+ device incorporates a Real Time Clock that maintains the real time, even when the device is off. When de device is off, the RTC is switched to the battery power supply (Vbat). The RTC uses a 32.768 KHz 20 ppm crystal.

Refer to Xilinx document UG1085 (Zynq UltraScale+ MPSoC technical reference guide) chapter 7 for more details on the Real Time Clock.

5.6 Interface connectors

The URP board is a stand-alone board, demonstrating the capabilities of an embedded heterogeneous processing system in a UAV context. Although the versatility is high, the capabilities have a limit. Therefore the platform must be expandable with different other processing boards. The expansion solutions identified are:

- Rincon Raptor software-defined radio add-on board
- Second Xilinx Drone Platform board
- Miami System-on-Module or other SOM expansion
- Custom expansion board

Figure 5.17 gives an overview of the connections between the different boards. All boards are using the same Samtec 120 pins QSH-060 mezzanine connector. This allows stacking of boards using direct board-to-board connections and wired board connection for maximum flexibility with preservation of signal integrity.

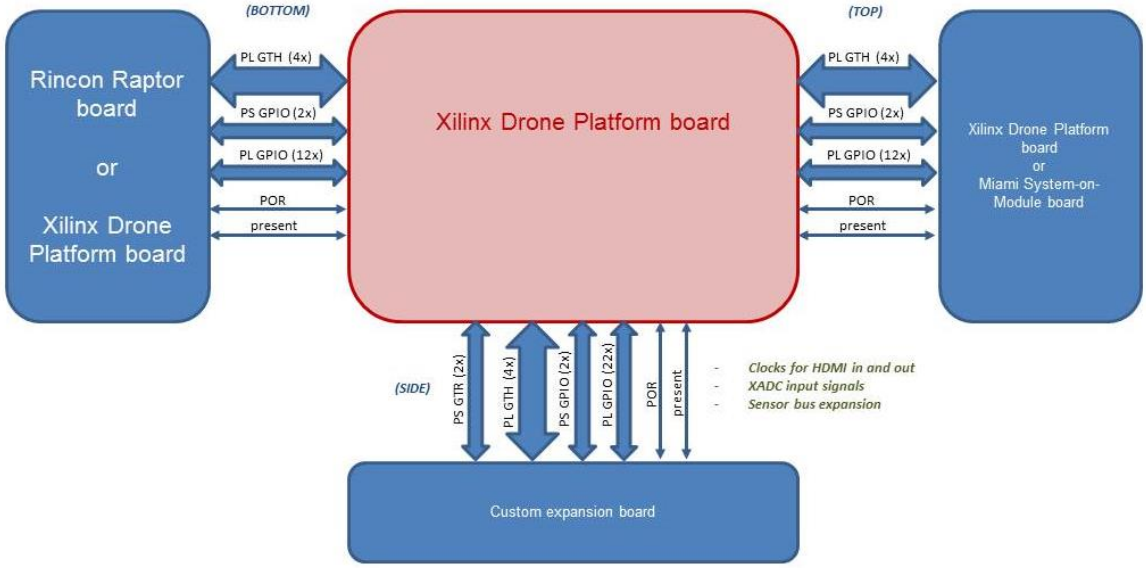


Figure 5.17: Board expansion specification

The boards all share the same pinning to reduce the complexity of the interconnect and enforcing a form of standardization. As the Raptor board is already available, the pinning of that board is taken as reference. The following connectivity is foreseen:

- 4x PL GTH transceiver link shared with all three boards. This gives a maximum 65Gbit/sec link between the individual boards. The transceivers are utilized in groups around quads on the FPGA. This allows binding to a single high-speed connection. When assuming that 4K@60fsp with 32 bit color is a state-of-the-art video standard, the resulting bit rate of such a stream is around 16Gbit/sec. This means that every link can host multiple feeds in both directions.
- 2x PS GPIO signals. This allows direct, uncomplicated signal exchange at processor level between the processors.
- 12 / 22x PL GPIO signals. This allows any type of low-latency connectivity between the FPGA logic on all boards. Using LVDS connectivity more high-speed connections are also possible.
- The connector to the custom expansion board is also equipped with signals connected to the PS-GTR transceivers. This to setup gigabit links directly to the processor, for example, SATA, PCI-Express or DisplayPort.

As an example of the connectivity capabilities of the board, the block diagram of the Ricon's Raptor software defined radio board is given in figure 5.18.

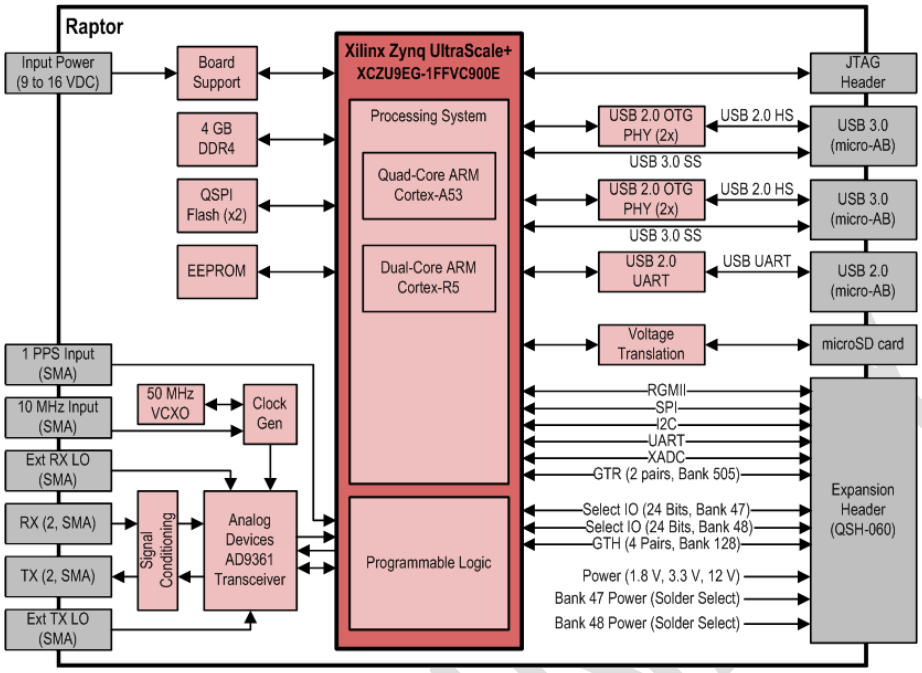


Figure 5.18: Rincon's Raptor software defined radio add-on board

The pin-out of the 3 connectors is given in table 5.x. Care must be taken when powering the expansion boards from the URP board.

Connector reference		(Jx) Ricon Raptor, stacking, expansion, Miami header				
Connector type						
Pin	Label	FPGA pin (Bottom)	FPGA pin (Top)	FPGA pin (Exp)	Logic level	Description
2	PSGTR_RX0_p	L29	J29	H27	GTR	Communication link with processor system connected transceivers. Allows high-speed data communication between the processor systems. Only one pair is used due to routing restrictions. 6Gb/s/lane max.
4	PSGTR_RX0_n	L30	J30	H28	GTR	
6	PSGTR_TX0_p	M27	K27	J25	GTR	
8	PSGTR_TX0_n	M28	K28	J26	GTR	
14	PSGTR_RX1_p	-	-	-	-	Not connected. Not enough resources on PL transceivers.
16	PSGTR_RX1_n	-	-	-	-	
20	PSGTR_TX1_p	-	-	-	-	
22	PSGTR_TX1_n	-	-	-	-	
26	PS_SPI1_MOSI	xxx	xxx	xxx		Allows data exchange at GPIO, SPI or UART level between the processor systems
28	PS_SPI1_MISO	xxx	xxx	xxx		
30	PS_SPI1_CS1_n	xxx	xxx	xxx		
32	PSG_SPI1_CLK					
36	PS_UART1_TX	-	-	-	-	Not connected. Not enough resources on PL transceivers.
38	PS_UART1_RX	-	-	-	-	
40	VCC_I2C1_SDA	-	-	-	-	
42	VCC_I2C1_SCL	-	-	-	-	
44	VCC_1V8	-	-	-	-	Not connected, supply from Raptor board
46	PS_MDC	-	-	-	-	Not connected, no need for Ethernet PHY connection
48	PS_MDIO	-	-	-	-	
50	PS_RGMII_TXD0	-	-	-	-	
52	PS_RGMII_TXD1	-	-	-	-	
54	PS_RGMII_TXD2	-	-	-	-	
56	PS_RGMII_TXD3	-	-	-	-	
58	PS_RGMII_TX_CTL	-	-	-	-	
60	PS_RGMII_TXC	-	-	-	-	
49	PS_RGMII_RXD0	-	-	-	-	
51	PS_RGMII_RXD1	-	-	-	-	
53	PS_RGMII_RXD2	-	-	-	-	
55	PS_RGMII_RXD3	-	-	-	-	
57	PS_RGMII_RX_CTL	-	-	-	-	
59	PS_RGMII_RXC	-	-	-	-	
43	PLGTH_RX0_n	D2	N4	V2	GTH	Communication link between the Programmable Logic parts. By utilizing a complete quad, the maximum performance on data exchange is possible. A typical Auroralink will perform with a bandwidth of over 5Gbyte/sec over such a link. An uncompressed 4K@60fps video stream needs roughly 2 Gbyte/sec.
45	PLGTH_RX0_p	D1	N3	V1	GTH	
37	PLGTH_TX0_n	D6	P6	W4	GTH	
39	PLGTH_TX0_p	D5	P5	W3	GTH	
31	PLGTH_RX1_n	C2	M2	U4	GTH	
33	PLGTH_RX1_p	C3	M1	U3	GTH	
25	PLGTH_TX1_n	C8	M6	V6	GTH	
27	PLGTH_TX1_p	C7	M5	V5	GTH	
19	PLGTH_RX2_n	B2	K2	T2	GTH	
21	PLGTH_RX2_p	B1	K1	T1	GTH	
13	PLGTH_TX2_n	B6	L4	T6	GTH	
15	PLGTH_TX2_p	B5	L3	T5	GTH	
7	PLGTH_RX3_n	A4	J4	P2	GTH	
9	PLGTH_RX3_p	A3	J3	P1	GTH	
1	PLGTH_TX3_n	A8	K6	R4	GTH	
3	PLGTH_TX3_p	A7	K5	R3	GTH	
61	PL47_IO0	xxx	xxx	xxx	1V8 CMOS	This can be used for low-latency connectivity between boards. Data pumping should be performed via the GTH links.
63	PL47_IO1	xxx	xxx	xxx	1V8 CMOS	
65	PL47_IO2	xxx	xxx	xxx	1V8 CMOS	
67	PL47_IO3	xxx	xxx	xxx	1V8 CMOS	
69	PL47_IO4	xxx	xxx	xxx	1V8 CMOS	
71	PL47_IO5	xxx	xxx	xxx	1V8 CMOS	
73	PL47_IO6	xxx	xxx	xxx	1V8 CMOS	
75	PL47_IO7	xxx	xxx	xxx	1V8 CMOS	

79	PL47_IO8	-	-	-	-	Not connected. No functionality expected, other then communication.
81	PL47_IO9	-	-	-	-	
83	PL47_IO10	-	-	-	-	
85	PL47_IO11	-	-	-	-	
87	PL47_IO12	-	-	-	-	
89	PL47_IO13	-	-	-	-	
91	PL47_IO14	-	-	-	-	
93	PL47_IO15	-	-	-	-	
97	PL47_IO16	-	-	-	-	
99	PL47_IO17	-	-	-	-	
101	PL47_IO18	-	-	-	-	
103	PL47_IO19	-	-	-	-	
105	PL47_IO20	-	-	-	-	
107	PL47_IO21	-	-	-	-	
109	PL47_IO22	-	-	-	-	
111	PL47_IO23	-	-	-	-	
77	VCC_PL47	-	-	-	-	Not connected, supply from Raptor board. Bank voltage level is a soldering option on the Raptor board. Must be set to 1V8.
95	VCC_PL47	-	-	-	-	
62	PL48_IO0	-	-	-	-	Not connected. No functionality expected, other then communication.
64	PL48_IO1	-	-	-	-	
66	PL48_IO2	-	-	-	-	
68	PL48_IO3	-	-	-	-	
70	PL48_IO4	-	-	-	-	
72	PL48_IO5	-	-	-	-	
74	PL48_IO6	-	-	-	-	
76	PL48_IO7	-	-	-	-	
80	PL48_IO8	-	-	-	-	
82	PL48_IO9	-	-	-	-	
84	PL48_IO10	-	-	-	-	
86	PL48_IO11	-	-	-	-	
88	PL48_IO12	-	-	-	-	
90	PL48_IO13	-	-	-	-	
92	PL48_IO14	-	-	-	-	
94	PL48_IO15	-	-	-	-	
98	PL48_IO16	xxx	xxx	xxx	1V8 CMOS	This can be used for low-latency connectivity between boards. Data pumping should be performed via the GTH links.
100	PL48_IO17	xxx	xxx	xxx	1V8 CMOS	
102	PL48_IO18	xxx	xxx	xxx	1V8 CMOS	
104	PL48_IO19	xxx	xxx	xxx	1V8 CMOS	
106	PL48_IO20	xxx	xxx	xxx	1V8 CMOS	
108	PL48_IO21	xxx	xxx	xxx	1V8 CMOS	
110	PL48_IO22	xxx	xxx	xxx	1V8 CMOS	
112	PL48_IO23	xxx	xxx	xxx	1V8 CMOS	
78	VCC_PL48	-	-	-	-	Not connected, supply from Raptor board. Bank voltage level is a soldering option on the Raptor board. Must be set to 1V8.
96	VCC_PL48	-	-	-	-	
113	VCC_3V3	-	-	-	-	Not connected, supply from Raptor board
115	VCC_3V3	-	-	-	-	Not connected, supply from Raptor board
114	VCC_9V_to_16V	-	-	-	-	Not connected, supply from Raptor board
117	SYSMON_V_p	-	-	-	-	Not connected, used for ADC on Raptor
119	SYSMON_V_n	-	-	-	-	Not connected, used for ADC on Raptor
118	PS_POR_n	???	???	???	???	Reset to the Raptor board to enforce a power-on-reset
120	EXP_PRSNT_n	???	???	???	???	Signals the presence of the expansion board

6 Power supplies

6.1 Battery pack and charger

A 3S2P LiIon battery pack can be connected to connector X70 on the FLORIDA (see **Error! Reference source not found.**). The battery charger is functioning autonomously and will work regardless of the position of the on/off switch. It is preset to a charge current of 1.5A and a green LED (next to the power LED) will indicate that charging is in progress. If the MIAMI is up and running, the charge progress can also be monitored via the I2C bus (see chapter I2C).

A gas gauge, the LTC2943CDD from Linear Technology, is being used to track the battery packs state of charge. This gas gauge is connected to the general I2C bus (see chapter I2C).

7 Characteristics

7.1 Electrical specifications

Supply voltage	9 - 17 [Vdc]
Current consumption	15 [W] maximum

7.2 Environment specifications

Extended operating temperature	-0 … +70[°C]
Storage temperature	-40 … +125[°C]
Relative humidity	0 … 95%, non-condensing

7.3 Mechanical specifications

Weight	approximately 50 [gram]
Board	glass epoxy Megtron6, UL-listed, 16 layers, 1.6 [mm]
Dimensions	135 [mm] x 68 [mm] x 10.0 [mm] (length x width x height)

7.4 Regulatory conformation

CE (EMC, EMI)	Report available on request
Temperature and humidity	Report available on request
RoHS	All applied components, printed circuit board material, production of the printed circuit board as well as the assembly of the boards are conducted in compliance with the RoHS legislation. Report available on request.

Appendix A: Debug expansion board

A micro SD Card interface is available on the debug print, allowing the MIAMI to boot from. A normal micro SD memory card can be used in this slot. The external interface is directly connected the MIO pins of the PS.

X2 pin	Signal	X1 pin	Description
1	SDIO_uSD_DQ2	18	SDIO Data 2
2	SDIO_uSD_DQ3	19	SDIO Data 2
3	SDIO_uSD_CMD	14	SDIO CMD
4	+3V3	-	-
5	SDIO_uSD_CLK	15	SDIO CLK
6	GND	-	-
7	SDIO_uSD_DQ0	16	SDIO Data 0
8	SDIO_uSD_DQ1	17	SDIO Data 1
9	GND	-	-
10	SDIO Detect	13	SDIO detect signal
SH1-4	Shield	-	Shield

A card detect signal is routed directly from the uSD connector to the SOM interface. This signal, SDIO_DETECT is connected to pin X23-56 and is pulled low whenever a card is inserted.

UART

There is an UART connection to the Miami URP, this UART is running on 1.8V. To use this UART for debugging purposes you could use an UART to USB converter (e.g. TTL-232RG-VREG1V8-WE FROM FTDI) on X4.

X4 pin	Signal	X1 pin	Description
1	GND	-	Ground
2	UART_RXD	11	RXD from header
3	UART_TXD	10	TXD to header

JTAG

There is a JTAG connection to the Miami URP, this is running on 1.8V. To use this JTAG for debugging purposes you can use a standard Xilinx JTAG to USB T converter (e.g. HW-USB-II-G) on X5.

X4 pin	Signal	X1 pin	Description
1	GND	-	Ground
2	JTAG V_REF	3	V REF
3	GND	-	Ground
4	JTAG_TMS	4	TMS
5	GND	-	Ground
6	JTAG_TCK	7	TCK
7	GND	-	Ground
8	JTAG_TDO	6	TDO
9	GND	-	Ground
10	JTAG_TDI	5	TDI
11	GND	-	Ground
12	JTAG_RESET	3	Reset
13	GND	-	Ground
14	SW_RESET_N	9	Reset

Appendix B: Extension Board

On the extension print are some LED’s, a buzzer, a HDMI output, an M.2 connector and the necessary circuits around it. It plugs directly into the extension connector on the Miami URP and has two mounting holes that are lined out for securing the board.

The HDMI output is based on the SN65DP159 chipset from Texas Instruments and the Xilinx HDMI IP Core. The AC coupled GTX HDMI output is converted by the SN65DP159 to the necessary DC TMDS standard. The chipset can handle 4K 60fps at a maximum.

The M.2 connector makes use of a two lane PCIe solution directly connected to the GTR transceivers of the MPSoC processor. It can handle up to speeds of 6Gb/s.It has a M key connector and can house an 2242 size M.2 SSD (e.g. Toshiba RC100 NVMe SSD).

Appendix C: Motor interface board

The motor control interface board is a board that converts the motor connector pinout to the necessary pinout for the PMOD Motor drivers from Trenz electronic