SOM MIAMI+ XC7Z045

Product Guide

V1R2 / 18/9/17

TOPIC
EMBEDDED PRODUCTS

Materiaalweg 4, 5681 RJ BEST, the Netherlands
P.O. Box 440, 5680 AK BEST, the Netherlands
t: +31 (0)499 336969 | f: +31 (0)499 336970
w: www.TopicEmbeddedProducts.com | e: info@TopicEmbeddedProducts.com

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Topic Embedded Products’ products. To the maximum extent permitted by applicable law: (1) Materials are made available “AS IS” and with all faults, Topic Embedded Products hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Topic Embedded Products shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Topic Embedded Products had been advised of the possibility of the same. Topic Embedded Products assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. IP cores may be subject to warranty and support terms contained in a license issued to you by Topic Embedded Products. Topic Embedded Products’ products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Topic Embedded Products’ products in Critical Applications.

© Copyright 2013-2017 Topic Embedded Products B.V. Topic Embedded Products, the Topic Embedded Products logo and other designated brands included herein are trademarks of Topic Embedded Products in the Netherlands and other countries. All other trademarks are the property of their respective owners.

Table of Contents

Notice of Disclaimer 2
Table of Contents 3
1 Introduction 5
2 Installation 6
2.1 Software installation 6
3 Miami+ SoM features 7
4 Miami+ SoM architecture 8
4.1 Miami+ SoM board layout 8
4.2 Block diagram 9
4.3 Mechanical description 10
5 Miami+ SoM board functionality 11
5.1 Configuration and debug interfaces 11
5.1.1 Status LEDs 11
5.1.2 Boot mode selection switches 12
5.1.3 JTAG interfaces 12
5.1.4 Console interfaces 13
5.2 Memory resources 14
5.2.1 DDR3 SDRAM memory (MT41K256M16) 14
5.2.2 Serial Dual QSPI NOR flash memory (N25Q256) 16
5.2.3 SD-card memory interface 16
5.2.4 EEPROM memory (CAT24C04) 16
5.2.5 Memory vault (ATSHA204A) 17
5.3 Communication interfaces 18
5.3.1 Gigabit Ethernet 18
5.3.2 USB 2.0 OTG 18
5.3.3 SDIO 18
5.3.4 SATA 19
5.3.5 PCI-Express 19
5.4 Miscellaneous resources 21
5.4.1 Clocking resources 21
5.4.2 Fan controller 21
5.4.3 I2C connected support peripherals 22
5.5 Power supplies 23
5.5.1 Battery backup supply 23
5.5.2 I/O reference supplies 23
5.5.3 Analogue supply 23
5.5.4 Power distribution 26
6 Connector pin assignments 27
6.1 X1: Carrier board connector pinning 28
6.2 X2: Carrier board connector pinning 29
6.3 X3: Carrier board connector pinning 30
7 Electrical characteristics 32
7.1 Electrical specifications 32

7.2 Environment specifications 32
7.3 Mechanical specifications 32
7.4 Regulatory conformation 32

1 Introduction

The MIAMI+ XC7045 processor module is a 85x68.5mm sized CPU board based on the Xilinx Zynq XC7Z045 processor. This Zynq processor includes a dual-core ARM Cortex A9 processor integrated with FPGA fabric, adding programmable logic and high-performance computing capabilities to the processor platform. The processor is based on Kintex FPGA technology, adding a logic density, higher clock rates and increased DSP performance up to 2622 GMAC fixed-point operations per second.

The processor cores run up to 1GHz and include a variety of functions required for multimedia, medical or industrial applications. These include encryption, encoding, accelerators, display interface, camera interfacing, LVDS interfaces, audio interfaces and general purpose inputs and outputs.

When placing a production order of 50 units or more, the modules can be ordered with different sizes of flash memory, DDR-SDRAM and several configuration options. The SoM provides support for several standard interfaces, such as Ethernet, USB 2.0, SDIO, PCI-Express and SATA2 or SATA3.

All interfaces are accessible through the three high-performance Samtec connectors.

Maximum power consumption of the whole board is around 30W. Passive or active cooling precautions must be put in place to support thermal conduction measures suitable for the target application. Otherwise the Miami+ will overheat.

2 Installation

The Miami+ System-on-Modules are delivered with a pre-installed Linux distribution, executed from the NOR flash memory. Powering the board by mounting the Miami on a carrier board will automatically boot the Miami+ board from the NOR flash and gives you a command prompt on the terminal (UART) port.

2.1 Software installation

The Miami+ SoM comes with a Linux distribution, which can be downloaded from GitHub:

https://github.com/topic-embedded-products/topic-platform

This is an easy starting point for developing your own applications. When accessing this website, you are guided through the steps to download, install and start using the software. The Linux distribution contains:

- Linux configuration and development tools
- Cross compiler for the Zynq/Cortex-A9 processor
- BSP with drivers for all peripherals on the Miami SoMs (including the PCAP to program the FPGA)
- Simple example program for getting started

The Miami+ SoMs are not dependent on versions of Vivado tooling.

For any help or support, please contact us at support@TopicEmbeddedProducts.com.

3 Miami+ SoM features

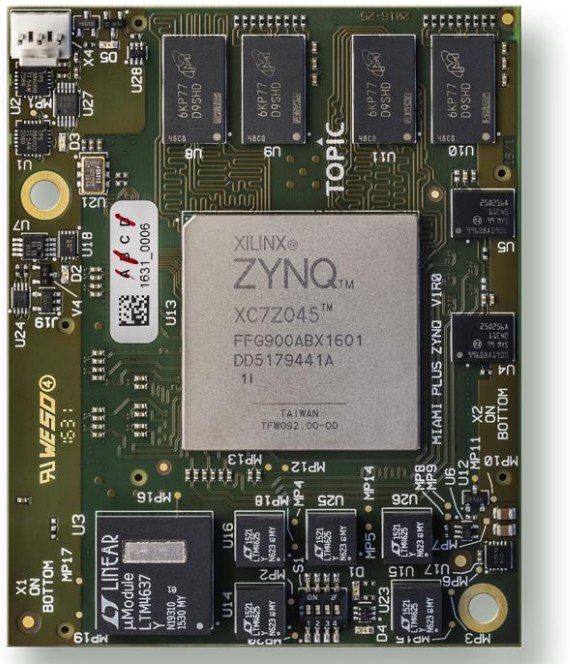
	MIAMI+ XC7035	MIAMI+ XC7045	MIAMI+ XC7100
PROCESSOR SYSTEM			
Xilinx SoC [1)]	XC7Z035-FFG900-2	XC7Z045-FFG900-2	XC7Z100-FFG900-2
CPU Architecture	ARM Cortex-A9 (dual core)		
CPU Performance	Up to 1 GHz		
Co-Processor	2x ARM NEON™		
MEMORY			
Cache	L1: 32KB instruction/core, 32KB data/core, L2: 512KB		
SDRAM [1)]	DDR3/DDR3L @ 533MHz, 1024 MB (connected to CPU)		
SDRAM [1)]	DDR3/DDR3L @ 533MHz, 1024 MB (connected to FPGA)		
NOR [1)]	Dual QSPI, 64MB		
EEPROM	4 Kb for secure (SHA-256) storage 4 Kb normal storage		
FPGA			
Technology	Kintex®-7		
Logic cells	275K	350K	444K
LUTs	171.900	218.600	277.400
Flip Flops	343.800	437.200	554.800
RAM (36Kb BRAM)	2000 KB (500)	2180 KB (545)	3020 KB (755)
DSP slices	900	900	2020
GTX transceivers	16x (10.3125 Gb/s each)		
2x120 and 1x180 pins available on SOM connector for programmable interfaces			
LAN	10/100/1000Mbps Ethernet, additional RMII interface		
Analog	Up to 8 channels differential, 12 bits		
Serial	UART, I2C, SPI, I2S, user defined		
Video	LVDS, SDI, TFT, VGA, LCD		
USB	USB OTG 2.0		
Debug	Debug UART, console		
Miscellaneous	GPIO/SD/SDIO 2.0/MMC 3.31 compliant controllers		
GTX transceivers	16x (10.3125 Gb/s each)		
Dedicated interfaces on SOM connector			
Network	1000Mbps Ethernet		
USB	USB OTG 2.0		
SATA	SATA-3		
PCI-Express	GEN2 – 8 lanes		
JTAG	JTAG chain for carrier board programming		
Power supply			
Input	15V via connector On-board voltage regulation		
Output	Programmable I/O standards and voltages		
Control	Current measurement for PL and PS		
Software			
Bootloader / BSP	U-Boot		
Boot options	JTAG, NOR, (external) SD-Card		
Operating System	Topic Linux 4.x distribution on GitHub		
Dyplo® compatible platform	Yes		
Mechanical and environmental			
Dimensions			
Connectors	2x 120 pins & 1x 180 pins Samtec high performance mezzanine carrier board connectors		
Temperature	Industrial grade		

[1)] *Other configurations possible at higher volumes.*

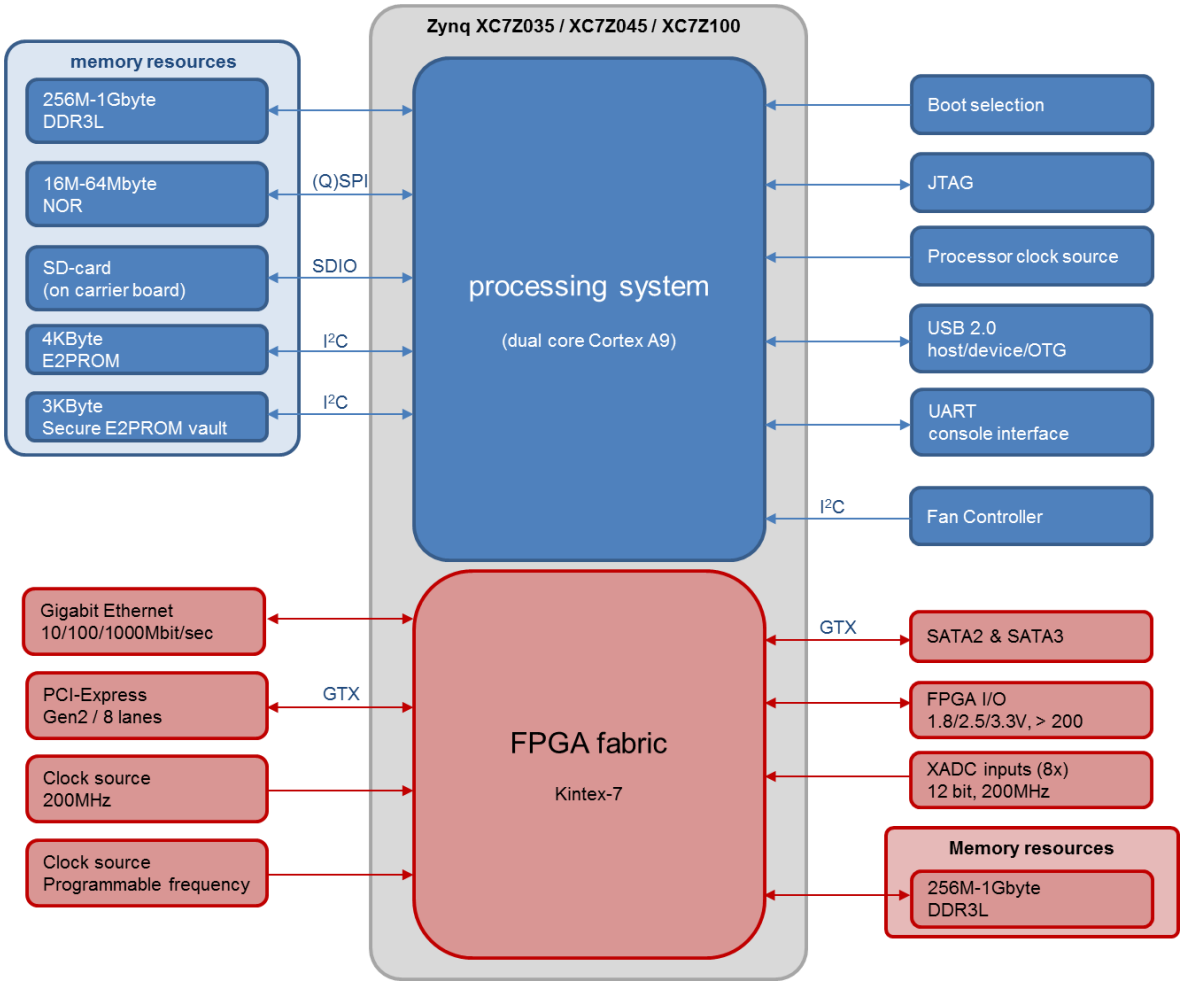
4 Miami+ SoM architecture

The Miami+ System-on-Module integrates all peripherals to bring up a full functional processing system. The system connects to the carrier board using three high performance connectors. The following paragraphs give an overview of peripherals and devices which determine the functionality of the board.

4.1 Miami+ SoM board layout



4.2 Block diagram

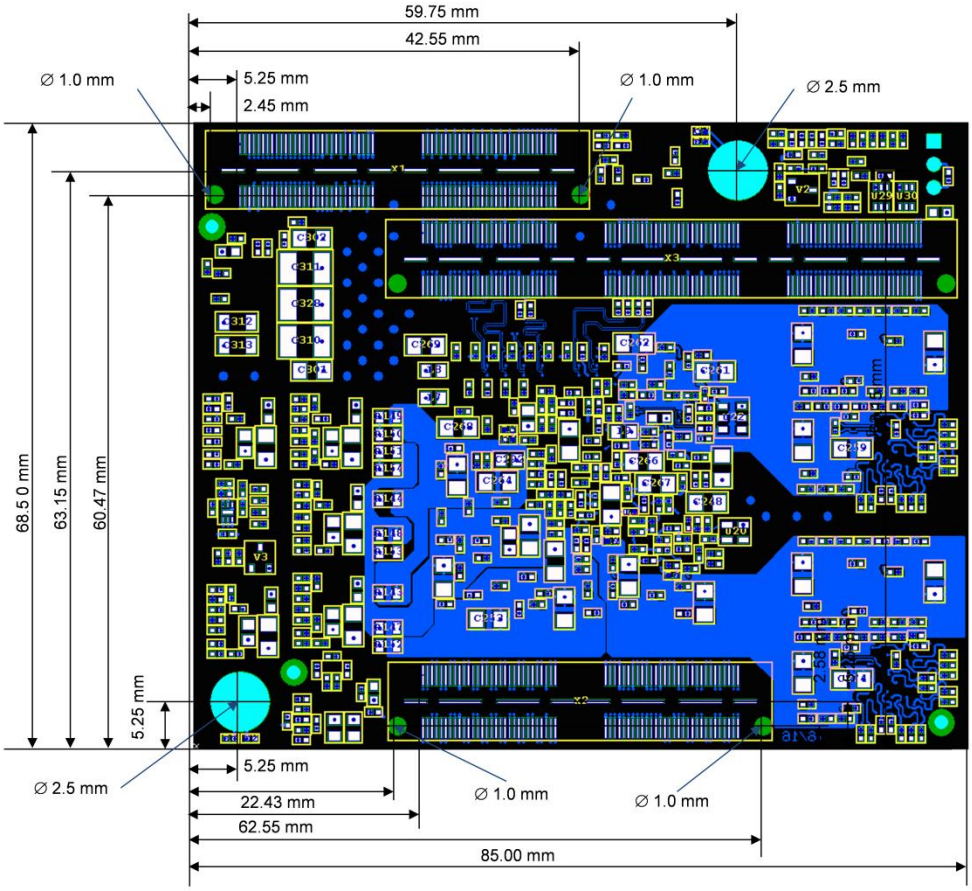


4.3 Mechanical description

The Miami should be fitted on a carrier board using three mating connectors:

Part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm (2x)
	Samtec, QTH-090-01-L-D-A, High Speed ground plane socket, 180 pins (3x60), stacking height 5mm

The exact relative placement details of the connectors, the guide holes for the connectors and the fixation standoff holes are described in the following figure. The exact measurement details can be downloaded from the support website as a DXF object to match the Miami SoM exactly on your carrier board layout placement plan.



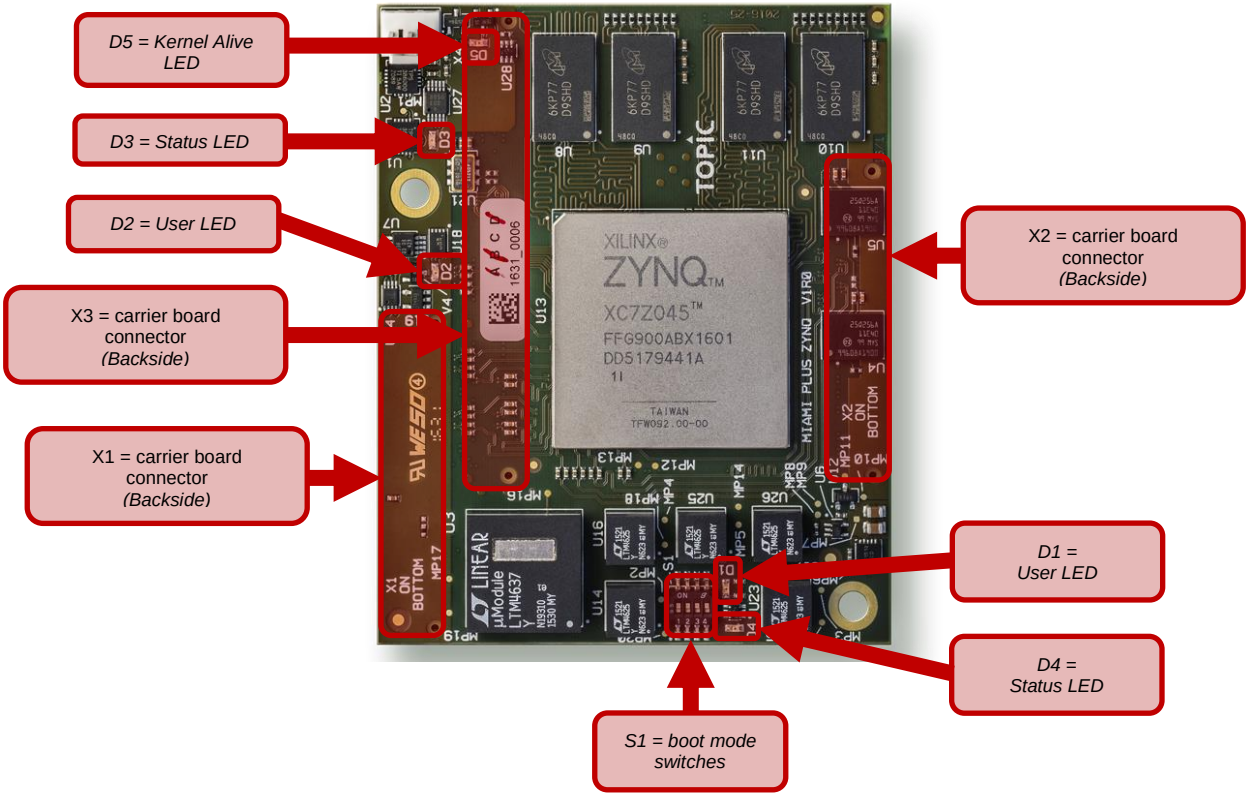
5 Miami+ SoM board functionality

The functionality of the SoM module can be divided in different function groups:

- Configuration and debug interfaces
- Memory resources
- Communication interfaces
- Miscellaneous functionality
- Power supplies and system integrity

In the following paragraphs the functions will be explained from a user perspective to help understand the context to use and program the functionality.

5.1 Configuration and debug interfaces



5.1.1 Status LEDs

There are 4 status LEDs provided on the Miami boards. These are indicating the operational status of the board from a system and user perspective.

LED reference	FPGA pin	Description
D1	AA17 (IO-25-10)	FPGA user LED. By default this LED will be off. However, the LED is available for the user to give it a different function.
D2	n.a.	User LED. By default this LED will be off. However, the LED is available for the user to give it a different function. The LED is connected to the GPIO expander, channel 4.
D3	n.a.	Power-good LED. When active, the primary power supplies on the board are up and within operational limits. When the Miami board is powered by 3.3[V] this must be the case.
D4	n.a.	FPGA image not ready. When active, the FPGA part of the Zynq is not loaded yet. When programmed with a valid bit stream, the LED will be off.
D5	B24 (PS_MIO7_500)	CPU alive LED. This LED is controlled by the processor system. By default a heartbeat signal is applied to the LED to indicate proper operation of the software. However, the LED is available for the user to give it a different function.

5.1.2 Boot mode selection switches

The first stage boot loader of the processor is able to boot the initial boot code from a selectable source: JTAG, NOR memory of from SD-card. This boot mode strapping is configurable using a 4 positions dipswitch S1 or via a configurable resistor bank. The last option is available as customization option.

Switch S1 settings *(sw1 to sw4)*	Boot mode	Comment
1010	JTAG in cascade mode	The dip switches control the state of the FPGA boot mode selection signals, located on the FPGA on pin F23(PS_MIO2_500), C23 (PS_MIO3_500), E23 (PS_MIO4_500) and C24 (PS-MIO5-500). These are only used during power-up state. Otherwise the functionality is shared with the quad SPI and memory controller.
0110	Dual QSPI NOR flash	
0101	SD-Card flash	

Another boot mode option is the signaling of the supply voltage on the MIO banks 500 and 501 of the processing system. Both banks are configured as 1.8 [V] banks, which is fixed in the Miami context. Another boot mode option is the bypassing of the PLL. This is a customization option, not a dynamic configuration item on the Miami.

Refer to Xilinx document UG585 (Zynq technical reference guide) chapter 6 for more details on booting strategies.

5.1.3 JTAG interfaces

The Zynq processor of Xilinx has one JTAG port connected to the dedicated JTAG pins on the Zynq. It is using 3.3[V] signal levels. The applicable pull-up resistors are integrated on the Miami board. Using the JTAG port you can:

- Program the FPGA fabric
- Use the ChipScope logic analyzer to debug the programmed FPGA logic
- Boundary scan for production verification
- Debug the processor software using the ARM CoreSight Debug Access Port (DAP)
- Debug the FPGA logic using the ILA (Integrated Logic Analyzer) from Xilinx

PL_JTAG signals	Connector pin	FPGA pin	Description
TDI	X1.113	P10 (TDI_0)	Dedicated package pin
TDO	X1.119	Y10 (TDO_0)	Dedicated package pin
TCK	X1.117	Y12 (TCK_0)	Dedicated package pin
TMS	X1.115	V10 (TMS_0)	Dedicated package pin

The JTAG port can be accessed from the carrier board using the SOM connector X1. This will allow the simultaneous connection of a FPGA and processor debugger, connect a console via USB to the processor and power the Miami via a mains adapter.

In addition to the standard JTAG signals, an additional reset signal is added. This is implemented to comply with Xilinx and ARM debug recommendations.

JTAG signal name	Connector pin	FPGA pin	Description
PS_JTAG_RSTN	X1.111	n.a.	Available for the software debugger to enforce a soft reset to the processor system.

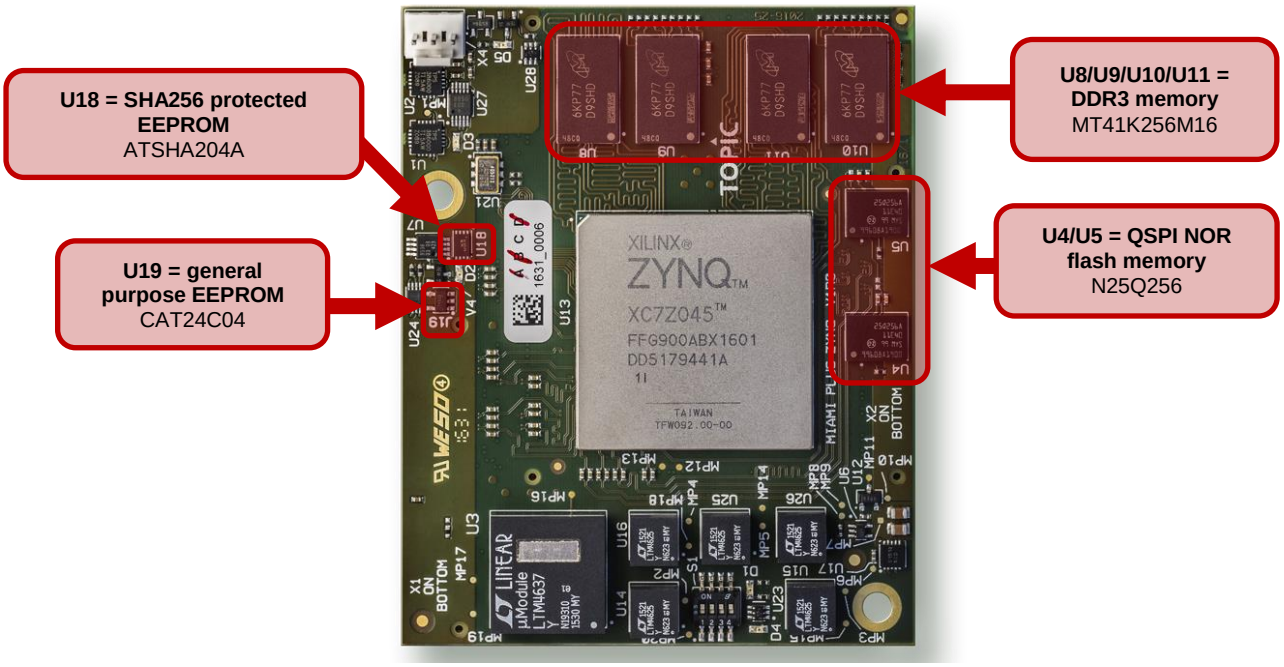
5.1.4 Console interfaces

A primary software development interface is the console connection with the processing system. The Miami provides a fixed console connection directly on the MIO port of the processing system.

Console signals	Connector pin	FPGA pin	Description
UART_RXD	X1.63	B22 (PS_MIO14_500)	Serial data from processor to other device. Can be used for other functionality if needed.
UART_TXD	X1.61	C22 (PS_MIO15_500)	Serial data from other device to processor. Can be used for other functionality if needed.

The console signals are available on the both the carrier board connector X1. The signals are provided 1.8[V] CMOS logic levels compatible. Make sure that you implement provisions when allowing simultaneous access to the console signals using the debug expansion header in combination with a carrier board.

5.2 Memory resources



5.2.1 DDR3 SDRAM memory (MT41K256M16)

The Miami+ has two low-power DDR3 SDRAM memory solutions. The first solution is for the PS part of the Zynq and the second one is for the PL part of the Zynq. Both RAM memory solutions have a 32-bit interface and can be clocked up to 533 [MHz]. The DDR clock frequency is configured by the software configuration using PLL1 clock output 2, which the standard DDR clock output. The SDRAM memory size can be ordered[1] in sizes of 256[MB], 512[MB] and 1[GB] (default).

Both solutions are build using two 16-bit wide DDR3 memory chips (Micron MT41K256M16). The devices are connected to the dedicated DDR memory controller interface on the Zynq. They can be supplied by a 1.5[V] (default) or a 1.35[V] supply. The supply level is a hard-configuration option[2] of the module.

FPGA Pinning of DDR3 module connected to PL

Signal	FPGA pin	FPGA pin label
CLOCK_200M_N	G9	IO_L13N_T2_MRCC_34
CLOCK_200M_P	H9	IO_L13P_T2_MRCC_34
CLOCK_FPGA_N	D8	IO_L12N_T1_MRCC_34
CLOCK_FPGA_P	D9	IO_L12P_T1_MRCC_34
PL_DDR3_A0	A10	IO_L1N_T0_34
PL_DDR3_A1	A8	IO_L3P_T0_DQS_PUDC_B_3
PL_DDR3_A10	C7	IO_L4P_T0_34
PL_DDR3_A11	B9	IO_L2P_T0_34
PL_DDR3_A12	B7	IO_L4N_T0_34
PL_DDR3_A13	E11	IO_L8P_T1_34
PL_DDR3_A14	B6	IO_L5N_T0_34
PL_DDR3_A2	B10	IO_L1P_T0_34
PL_DDR3_A3	J11	IO_L7P_T1_34
PL_DDR3_A4	F7	IO_L16N_T2_34
PL_DDR3_A5	H7	IO_L18P_T2_34
PL_DDR3_A6	G7	IO_L18N_T2_34
PL_DDR3_A7	L7	IO_L19P_T3_34
PL_DDR3_A8	A7	IO_L3N_T0_DQS_34

[1] *Minimum order volume = 50 pieces*
[2] *Minimum order volume = 50 pieces*

PL_DDR3_A9	A9	IO_L2N_T0_34
PL_DDR3_BA0	H12	IO_L9P_T1_DQS_34
PL_DDR3_BA1	D6	IO_L17N_T2_34
PL_DDR3_BA2	C6	IO_L5P_T0_34
PL_DDR3_CAS_B	E7	IO_L17P_T2_34
PL_DDR3_CKE	E10	IO_L10P_T1_34
PL_DDR3_CKN	F10	IO_L11N_T1_SRCC_34
PL_DDR3_CKP	G10	IO_L11P_T1_SRCC_34
PL_DDR3_CS_B	H11	IO_L7N_T1_34
PL_DDR3_DM0	J4	IO_L1P_T0_33
PL_DDR3_DM1	G2	IO_L7P_T1_33
PL_DDR3_DM2	D4	IO_L16P_T2_33
PL_DDR3_DM3	C4	IO_L19P_T3_33
PL_DDR3_DQ0	K1	IO_L2N_T0_33
PL_DDR3_DQ1	L1	IO_L2P_T0_33
PL_DDR3_DQ10	H3	IO_L11N_T1_SRCC_33
PL_DDR3_DQ11	G5	IO_L12P_T1_MRCC_33
PL_DDR3_DQ12	G1	IO_L10N_T1_33
PL_DDR3_DQ13	G6	IO_L8N_T1_33
PL_DDR3_DQ14	H2	IO_L10P_T1_33
PL_DDR3_DQ15	F2	IO_L7N_T1_33
PL_DDR3_DQ16	F4	IO_L14P_T2_SRCC_33
PL_DDR3_DQ17	F3	IO_L14N_T2_SRCC_33
PL_DDR3_DQ18	F5	IO_L13P_T2_MRCC_33
PL_DDR3_DQ19	E2	IO_L17N_T2_33
PL_DDR3_DQ2	K6	IO_L6P_T0_33
PL_DDR3_DQ20	D3	IO_L16N_T2_33
PL_DDR3_DQ21	E1	IO_L18P_T2_33
PL_DDR3_DQ22	E5	IO_L13N_T2_MRCC_33
PL_DDR3_DQ23	E3	IO_L17P_T2_33
PL_DDR3_DQ24	C2	IO_L22P_T3_33
PL_DDR3_DQ25	B2	IO_L23P_T3_33
PL_DDR3_DQ26	C1	IO_L22N_T3_33
PL_DDR3_DQ27	B5	IO_L20P_T3_33
PL_DDR3_DQ28	A2	IO_L24N_T3_33
PL_DDR3_DQ29	B4	IO_L20N_T3_33
PL_DDR3_DQ3	L2	IO_L4N_T0_33
PL_DDR3_DQ30	B1	IO_L23N_T3_33
PL_DDR3_DQ31	A3	IO_L24P_T3_33
PL_DDR3_DQ4	J5	IO_L5N_T0_33
PL_DDR3_DQ5	K5	IO_L5P_T0_33
PL_DDR3_DQ6	J3	IO_L1N_T0_33
PL_DDR3_DQ7	L3	IO_L4P_T0_33
PL_DDR3_DQ8	H4	IO_L11P_T1_SRCC_33
PL_DDR3_DQ9	H6	IO_L8P_T1_33
PL_DDR3_DQS_N0	K2	IO_L3N_T0_DQS_33
PL_DDR3_DQS_N1	H1	IO_L9N_T1_DQS_33
PL_DDR3_DQS_N2	D5	IO_L15N_T2_DQS_33
PL_DDR3_DQS_N3	A4	IO_L21N_T3_DQS_33
PL_DDR3_DQS_P0	K3	IO_L3P_T0_DQS_33
PL_DDR3_DQS_P1	J1	IO_L9P_T1_DQS_33
PL_DDR3_DQS_P2	E6	IO_L15P_T2_DQS_33
PL_DDR3_DQS_P3	A5	IO_L21P_T3_DQS_33
PL_DDR3_ODT	G11	IO_L9N_T1_DQS_34
PL_DDR3_RAS_B	C9	IO_L6P_T0_34
PL_DDR3_RESET_B	D11	IO_L8N_T1_34
PL_DDR3_WE_B	F8	IO_L16P_T2_34

5.2.2 Serial Dual QSPI NOR flash memory (N25Q256)

The on-board Dual quad SPI NOR flash memory offers a reliable boot memory source with sufficient storage capacity to hold a moderate embedded Linux distribution. The Miami applies two Micron N25Q256 devices, offering 64[MB]. This is a configuration option[3], which allows customization of the memory capacity to 128[MB].

The Miami assigns the NOR flash to fixed processing system MIO pins. Therefore, these pins are not available for user functionality. The following table describes which pins are being used by the dual quad SPI controller and not to be used by the user.

SPI NOR flash signal name	FPGA pin	FPGA pin label
SFLASH_DQ0_MODE3	F23	PS_MIO2_500
SFLASH_DQ1_MODE2	E23	PS_MIO4_500
SFLASH_DQ2_MODE1	C23	PS_MIO3_500
SFLASH_DQ3_MODE0	C24	PS_MIO5_500
SFLASH_SCK0_MODE4	D24	PS_MIO6_500
SFLASH_CS0_N	D23	PS_MIO1_500
SFLASH_DQ4	E22	PS_MIO10_500
SFLASH_DQ5	A23	PS_MIO11_500
SFLASH_DQ6	E21	PS_MIO12_500
SFLASH_DQ7	F22	PS_MIO13_500
SFLASH_SCK1	A24	PS_MIO9_500
SFLASH_CS1_N	F24	PS_MIO0_500

5.2.3 SD-card memory interface

Optionally, the Miami+ SoM can be booted from an SD-card, mounted on the carrier board, if implemented. The pin location on the connector is fixed when it is required for booting. If not required, the SDIO interface may be routed via the programmable logic and connected to any valid I/O pad. Under these conditions, the MIO signals on the processing system can be used for other purposes.

The SDIO interface is operated at 1.8[V]. This may require the use of a level converter on the carrier board to properly interface with the SDIO controller. The following table addresses the involved signals for proper carrier board implementation and software control.

SoM signal name	Signal	SoM pin	FPGA pin	FPGA pin label
IO_S_VCC4_6	uSD_CLK	X1.48	B20	PS_MIO40_501
IO_S_VCC4_10	uSD_CMD	X1.54	J18	PS_MIO41_501
IO_S_VCC4_12	uSD_DQ0	X1.58	D20	PS_MIO42_501
IO_S_VCC4_8	uSD_DQ1	X1.50	E18	PS_MIO43_501
IO_S_VCC4_4	uSD_DQ2	X1.46	E20	PS_MIO44_501
IO_S_VCC4_9	uSD_DQ3	X1.52	H18	PS_MIO45_501
IO_S_VCC4_11	DETECT	X1.56	A18	PS_MIO47_501

5.2.4 EEPROM memory (CAT24C04)

The SoM provides a 4Kbit I^2C connected CAT24C04 EEPROM device for storing parameters and other configuration and user settings. This device is connected to the Miami system I^2C bus, accessible via the following MIO pins of the processor system. *Refer to the datasheet of the CAT24C04 regarding information how to use this device. Be aware that 16 highest address words of the 512 available words are reserved by the system for the serial number and administrative parameters. Do not overwrite this data.*

I2C bus signal name	FPGA pin	FPGA pin label
SCL_1V8	C19	PS_MIO48_501
SDA_1V8	D18	PS_MIO49_501

I^2C address E^2PROM memory	0xA0

[3] *Minimum order volume = 50 pieces*

5.2.5 Memory vault (ATSHA204A)

An additional memory resource on the Miami+ SoM is a SHA256 protected memory vault to securely store data. The total amount of memory is limited to 3Kbit, but is secured using a HASH-based protection protocol. This device, the ATSHA204A of Atmel, is also connected to the Miami system I^2C bus, accessible via the following MIO pins of the processor system. *Refer to the datasheet of the ATSHA204 regarding information how to use this device.*

I2C bus signal name	FPGA pin	FPGA pin label
SCL_1V8	C19	PS_MIO48_501
SDA_1V8	D18	PS_MIO49_501

I^2C address memory vault	0xC8

5.3 Communication interfaces

5.3.1 Gigabit Ethernet

The Zynq processor contains 2 gigabit Ethernet controllers. These controllers are to be connected via the EMIO interface with the programmable logic and then routed to the I/O pads. Be aware that the use of common RMII Gigabit PHY devices requires an IP block in the FPGA converting the provided MII. This is because RMII via the EMIO is not supported by the Zynq. IP blocks covering this functionality are available via our web shop. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the high-end performance capabilities of the Gigabit Ethernet Controller (GEM) refer to Xilinx document UG585 (Zynq technical reference guide) chapter 16.*

5.3.2 USB 2.0 OTG

The Miami+ SoM supports one of the two integrated USB OTG controllers. These are only accessible via the MIO connected I/O pads, not the programmable logic. When the second USB controller is required, other MIO peripherals must be moved to other pin locations or functionally dropped. When USB is required, the USB control signals to the carrier board have to be connected using the designated signals on the connector and the corresponding signals on the Zynq device as described in the following table.

SoM signal name	Signal	SoM pin	FPGA pin	FPGA pin label
IO_S_VCC4_24	USB_CLK	X1.83	H17	PS_MIO36_501
IO_S_VCC4_26	USB_DIR	X1.87	H22	PS_MIO29_501
IO_S_VCC4_23	USB_STP	X1.81	L18	PS_MIO30_501
IO_S_VCC4_25	USB_NXT	X1.85	H21	PS_MIO31_501
IO_S_VCC4_27	USB_DQ0	X1.89	K17	PS_MIO32_501
IO_S_VCC4_22	USB_DQ1	X1.79	G22	PS_MIO33_501
IO_S_VCC4_20	USB_DQ2	X1.75	K18	PS_MIO34_501
IO_S_VCC4_16	USB_DQ3	X1.67	G21	PS_MIO35_501
IO_S_VCC4_19	USB_DQ4	X1.73	L27	PS_MIO28_501
IO_S_VCC4_17	USB_DQ5	X1.69	B21	PS_MIO37_501
IO_S_VCC4_21	USB_DQ6	X1.77	A20	PS_MIO38_501
IO_S_VCC4_18	USB_DQ7	X1.71	F18	PS_MIO39_501
USB_RESET	USB_RESET	X1.91	n.a.	Connected to the processor system using the PCA9536 I^2C I/O expander on address 0x82 on the Miami system I^2C bus. The signal can be accessed by addressing I/O pin IO[0].

5.3.3 SDIO

The Zynq processor contains 2 embedded SDIO controllers. The first controller can be used for booting the processor system. In this case it is bound to be connected to a particular set of MIO pins. When it is not required to boot from an SDIO connected SD-card image, both SDIO controllers can be accessed via the MIO processor pins or via the FPGA fabric. Be aware that the use of SDIO interface via FPGA fabric requires specific design constraints for proper operation. IP blocks covering this functionality are available via our webshop. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the usage of the SDIO controller refer to Xilinx document UG585 (Zynq technical reference guide) chapter 13.*

5.3.4 SATA

SATA-2 and SATA-3 compatible storage devices can be connected using the GTX transceivers on the Miami+ SoM. A total of 16 differential transceiver pairs are available on the carrier board connector, offering the ability to implement up to 16 SATA-3 devices. The GTX transceivers can support up to 10.3125[Gbit/sec]. To make use of SATA on the Miami, an additional IP block must be purchased, e.g. via the Topic Embedded Products webshop, interfacing the transceivers with the processing system by means of a SATA media access controller (MAC) in FPGA fabric and a software driver for the applicable operating system e.g. Linux.

The SATA interface can be connected to any of the transceiver pairs. Keep in mind that you are required to provide a differential clock source for driving one or both of the GTX transceivers dedicated clock sources through the carrier board connector. It is not possible to provide a clock directly from within the FPGA fabric.

The table on the next page gives an overview of the signals involved with the SATA interface.

5.3.5 PCI-Express

The Miami+ SoM integrated Zynq device incorporates a PCI-Express endpoint, supporting the Gen1 and Gen2 standard. Up to 8 lanes are supported. For using the PCI-Express integrated end-point or root-complex you require to acquire an additional IP block, e.g. via the Topic Embedded Products webshop, and additional software.

The PCI-Express interface has to be connected to the transceiver pairs according to the implementation requirements specified by Xilinx. *For more details refer to Xilinx data sheet DS821, user guide UG477. Keep in mind that you are required to provide one or more differential clock sources for driving the GTX transceivers dedicated clock sources through the carrier board connector. It is NOT possible to provide a clock directly from within the FPGA fabric!*

For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the usage of the PCI-Express end-point or root-complex refer to Xilinx document UG585 (Zynq technical reference guide) chapter 31.

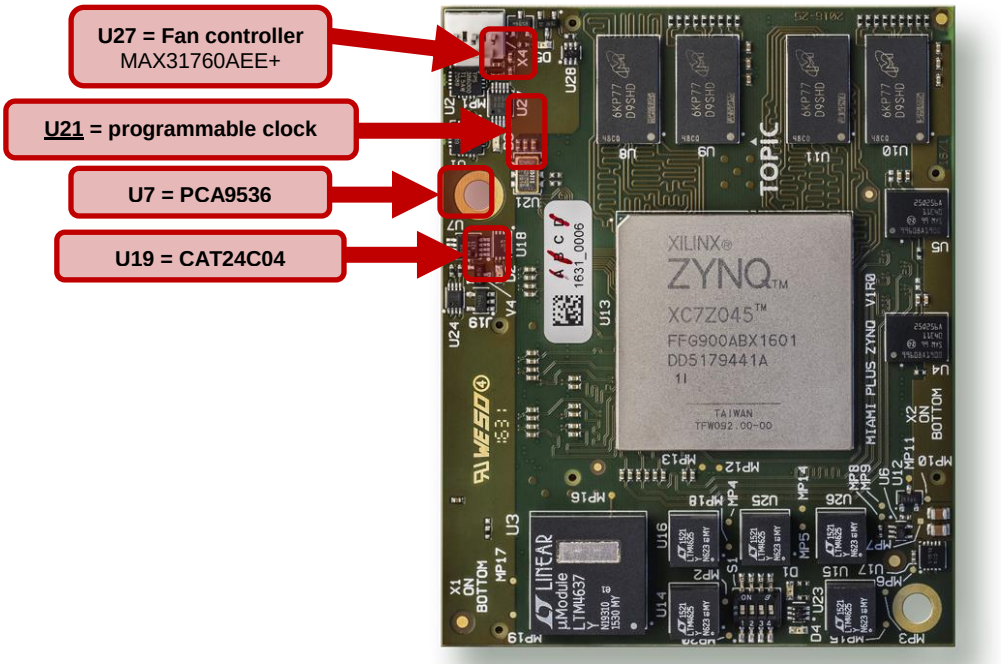
The table on the next page gives an overview of the signals involved with the PCI-Express interface. Be aware that these GTX transceivers are shared with SATA functionality. When implementing SATA and PCI-Express simultaneously, be aware that the total number of available PCI-Express lanes is reduced.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
MGT_D_REF_CLK_0_P	X2.87	AD10	MGTREFCLK0P_109
MGT_D_REF_CLK_0_N	X2.89	AD9	MGTREFCLK0N_109
MGT_D_REF_CLK_1_P	X2.64	AF10	MGTREFCLK1P_109
MGT_D_REF_CLK_1_N	X2.66	AF9	MGTREFCLK1N_109
MGT_D_REF_CLK_2_P	X3.27	AA8	MGTREFCLK0P_110
MGT_D_REF_CLK_2_N	X3.29	AA7	MGTREFCLK0N_110
MGT_D_REF_CLK_3_P	X3.52	U8	MGTREFCLK0P_111
MGT_D_REF_CLK_3_N	X3.54	U7	MGTREFCLK0N_111
MGT_D_REF_CLK_4_P	X3.81	N8	MGTREFCLK0P_112
MGT_D_REF_CLK_4_N	X3.83	N7	MGTREFCLK0N_112
MGT_D_TX_0_P	X2.75	AK10	MGTXTXP0_109
MGT_D_TX_0_N	X2.77	AK9	MGTXTXN0_109
MGT_D_TX_1_P	X2.63	AK6	MGTXTXP1_109
MGT_D_TX_1_N	X2.65	AK5	MGTXTXN1_109
MGT_D_TX_2_P	X2.81	AJ4	MGTXTXP2_109
MGT_D_TX_2_N	X2.83	AJ3	MGTXTXN2_109
MGT_D_TX_3_P	X2.69	AK2	MGTXTXP3_109
MGT_D_TX_3_N	X2.71	AK1	MGTXTXN3_109
MGT_D_TX_4_P	X3.15	AH2	MGTXTXP0_110
MGT_D_TX_4_N	X3.17	AH1	MGTXTXN0_110
MGT_D_TX_5_P	X3.16	AF2	MGTXTXP1_110

MGT_D_TX_5_N	X3.18	AF1	MGTXTXN1_110
MGT_D_TX_6_P	X3.21	AE4	MGTXTXP2_110
MGT_D_TX_6_N	X3.23	AE3	MGTXTXN2_110
MGT_D_TX_7_P	X3.22	AD2	MGTXTXP3_110
MGT_D_TX_7_N	X3.24	AD1	MGTXTXN3_110
MGT_D_TX_8_P	X3.40	AB2	MGTXTXP0_111
MGT_D_TX_8_N	X3.42	AB1	MGTXTXN0_111
MGT_D_TX_9_P	X3.45	Y2	MGTXTXP1_111
MGT_D_TX_9_N	X3.47	Y1	MGTXTXN1_111
MGT_D_TX_10_P	X3.46	W4	MGTXTXP2_111
MGT_D_TX_10_N	X3.48	W3	MGTXTXN2_111
MGT_D_TX_11_P	X3.51	V2	MGTXTXP3_111
MGT_D_TX_11_N	X3.53	V1	MGTXTXN3_111
MGT_D_TX_12_P	X3.69	T2	MGTXTXP0_112
MGT_D_TX_12_N	X3.71	T1	MGTXTXN0_112
MGT_D_TX_13_P	X3.70	R4	MGTXTXP1_112
MGT_D_TX_13_N	X3.72	R3	MGTXTXN1_112
MGT_D_TX_14_P	X3.75	P2	MGTXTXP2_112
MGT_D_TX_14_N	X3.77	P1	MGTXTXN2_112
MGT_D_TX_15_P	X3.76	N4	MGTXTXP3_112
MGT_D_TX_15_N	X3.78	N3	MGTXTXN3_112
MGT_D_RX_0_P	X2.76	AH10	MGTXRXP0_109
MGT_D_RX_0_N	X2.78	AH9	MGTXRXN0_109
MGT_D_RX_1_P	X2.82	AJ8	MGTXRXP1_109
MGT_D_RX_1_N	X2.84	AJ7	MGTXRXN1_109
MGT_D_RX_2_P	X2.88	AG8	MGTXRXP2_109
MGT_D_RX_2_N	X2.90	AG7	MGTXRXN2_109
MGT_D_RX_3_P	X2.70	AE8	MGTXRXP3_109
MGT_D_RX_3_N	X2.72	AE7	MGTXRXN3_109
MGT_D_RX_4_P	X3.3	AH6	MGTXTXP0_110
MGT_D_RX_4_N	X3.5	AH5	MGTXTXN0_110
MGT_D_RX_5_P	X3.4	AG4	MGTXTXP1_110
MGT_D_RX_5_N	X3.6	AG3	MGTXTXN1_110
MGT_D_RX_6_P	X3.9	AF6	MGTXTXP2_110
MGT_D_RX_6_N	X3.11	AF5	MGTXTXN2_110
MGT_D_RX_7_P	X3.10	AD6	MGTXTXP3_110
MGT_D_RX_7_N	X3.12	AD5	MGTXTXN3_110
MGT_D_RX_8_P	X3.28	AC4	MGTXTXP0_111
MGT_D_RX_8_N	X3.30	AC3	MGTXTXN0_111
MGT_D_RX_9_P	X3.33	AB6	MGTXTXP1_111
MGT_D_RX_9_N	X3.35	AB5	MGTXTXN1_111
MGT_D_RX_10_P	X3.34	Y6	MGTXTXP2_111
MGT_D_RX_10_N	X3.36	Y5	MGTXTXN2_111
MGT_D_RX_11_P	X3.39	AA4	MGTXTXP3_111
MGT_D_RX_11_N	X3.41	AA3	MGTXTXN3_111
MGT_D_RX_12_P	X3.57	V6	MGTXTXP0_112
MGT_D_RX_12_N	X3.59	V5	MGTXTXN0_112
MGT_D_RX_13_P	X3.58	U4	MGTXTXP1_112
MGT_D_RX_13_N	X3.60	U3	MGTXTXN1_112
MGT_D_RX_14_P	X3.63	T6	MGTXTXP2_112
MGT_D_RX_14_N	X3.65	T5	MGTXTXN2_112
MGT_D_RX_15_P	X3.64	P6	MGTXTXP3_112
MGT_D_RX_15_N	X3.66	P5	MGTXTXN3_112

Important: *for AC coupling reasons, the transmitter lines are coupled with a 100[nF] bypass capacitor. You have to take care that the carrier board implements the bypass capacitor on the transmitter side of the return signal. The signals are routed differentially with a controlled impedance of 100[Ohm].*

5.4 Miscellaneous resources



5.4.1 Clocking resources

The Miami+ SoM integrates three clock sources: the first (33.333[MHz]) is intended for the processor system, the second (200[MHz]) is available for the programmable logic and the third is a user programmable clock. The 200MHz clock and the user configurable clock are differential paired. Based on the PS_CLOCK, the processing system generates the clocks to drive the CPU cores, DDR memory and the bus clock. This clock is also available for the user in the FPGA fabric. The 200MHz clock is especially applicable for clocking the FPGA fabric. The third clock can be programmed between 100 KHz and 250 MHz, through the I2C bus.

Clock signal name	FPGA pin	Description	FPGA pin label
PS_CLOCK_33MHz	A22	33.333 MHz, 20 ppm	PS_CLK_500
CLOCK_200M_P	H9	200 MHz P, 20 ppm	IO_L13P_T2_MRCC_34
CLOCK_200M_N	G9	200 MHz N, 20 ppm	IO_L13N_T2_MRCC_34
CLOCK_FPGA_P	D9	100 kHz to 250 MHz P, 20 ppm	IO_L12P_T1_MRCC_34
CLOCK_FPGA_N	D8	100 kHz to 250 MHz N, 20 ppm	IO_L12N_T1_MRCC_34

5.4.2 Fan controller

The Miami+ SoM has the possibility to connect an external fan to provide extra cooling to the chip. This fan is controlled by a MAX31760AEE+ chip. This chip is controllable through the I2C bus which can be used to for example control the speed of the Fan. The fan can be powered by a 12V (default) or a 5V supply. The supply level is a hard-configuration option of the Miami SoM[4]. *Refer to the datasheet of the MAX31760AEE+ regarding information how to use this device.*

Fan out connector X4		
Signal	**Connector pin**	**Description**
GND	X4.1	GND reference for Fan
VCC	X4.2	Supply input for Fan
TACHO	X4.3	Tacho readback from Fan

[4] *Minimum order volume = 50 pieces*

5.4.3 I2C connected support peripherals

The Miami+ SoM implements one I^2C chain via the MIO pads directly with the processing system. The following table gives an overview of the involved pins on the Zynq and the carrier board pins. The I^2C bus implements peripherals on the Miami+ SoM. The use of the I^2C bus is NOT recommended on the carrier board.

I2C bus signal name	SoM pin	FPGA pin	FPGA pin label
SCL_1V8	X1.51	C19	PS_MIO48_500
SDA_1V8	X1.53	D18	PS_MIO49_500

The I^2C bus has multiple connected peripherals to control and maintain consistent operation of the modules. The devices are available for the user, but care must be taken as certain configurations may harm reliable operation. The following table lists the peripherals integrated as well as the functionality they provide on the board.

I2C peripheral	I2C address	Description
ATSHA204	0b1100100x	SHA encryption protected memory vault. Refer to the datasheets of the ATSHA204 for information how to access this device.
CAT24C04	0b1010000x	General purpose EEPROM memory. Refer to the datasheet of the CAT24C04 for information how to access this device.
Si514	0b01010101	Programmable I2C XO. Refer to the datasheet of the Si514 for information how to use this device.
MAX31760AEE+	0b10101110	Fan controller. Refer to the datasheet of the MAX31760AEE+ for information how to use this device.

5.5 Power supplies

For powering the Miami+ SoM a single 15.0[V] power supply is sufficient. The maximum current of the module is depending on:

- Operational frequency of the processor
- Load, execution profile and clock speed of the FPGA logic
- Type of I/O interfaces in use (especially the GTX transceivers consume much energy)

Power profile	
Nominal power supply	12 [V] +/- 5% / 15 [V] +/- 5%
Maximum current allowed	4.0 [A]

The Miami+ SoM must be powered from the carrier boards using the Samtec socket connectors. (X3.177-X3.180)

5.5.1 Battery backup supply

The FPGA facilitates a battery-backup supply pin for holding specific functions active during power-down of the device. By supplying this pin, the functionality behind this is guaranteed. *Refer to Xilinx user guide UG585 for more information on this functionality.*

5.5.2 I/O reference supplies

The used processor I/O banks (bank 500, 501, 10, 11, 12 and 35) are powered with different supply voltages and interface with signals present on the carrier board connector. To facilitate proper level conversion or limited logic supply loading, the supply of each I/O bank is made available. It is recommended not to exceed 100mA loading per supply pin presented on the connector.

5.5.3 Analogue supply

The analogue supply is provided as reference for the FPGA integrated XADC. It is not intended for supplying devices with relative high loads. Care must be taken to load this supply with as little as possible noise as it will influence the accuracy of the AD converter result.

The power supply connections are provided on the following carrier board and debug expansion connectors:

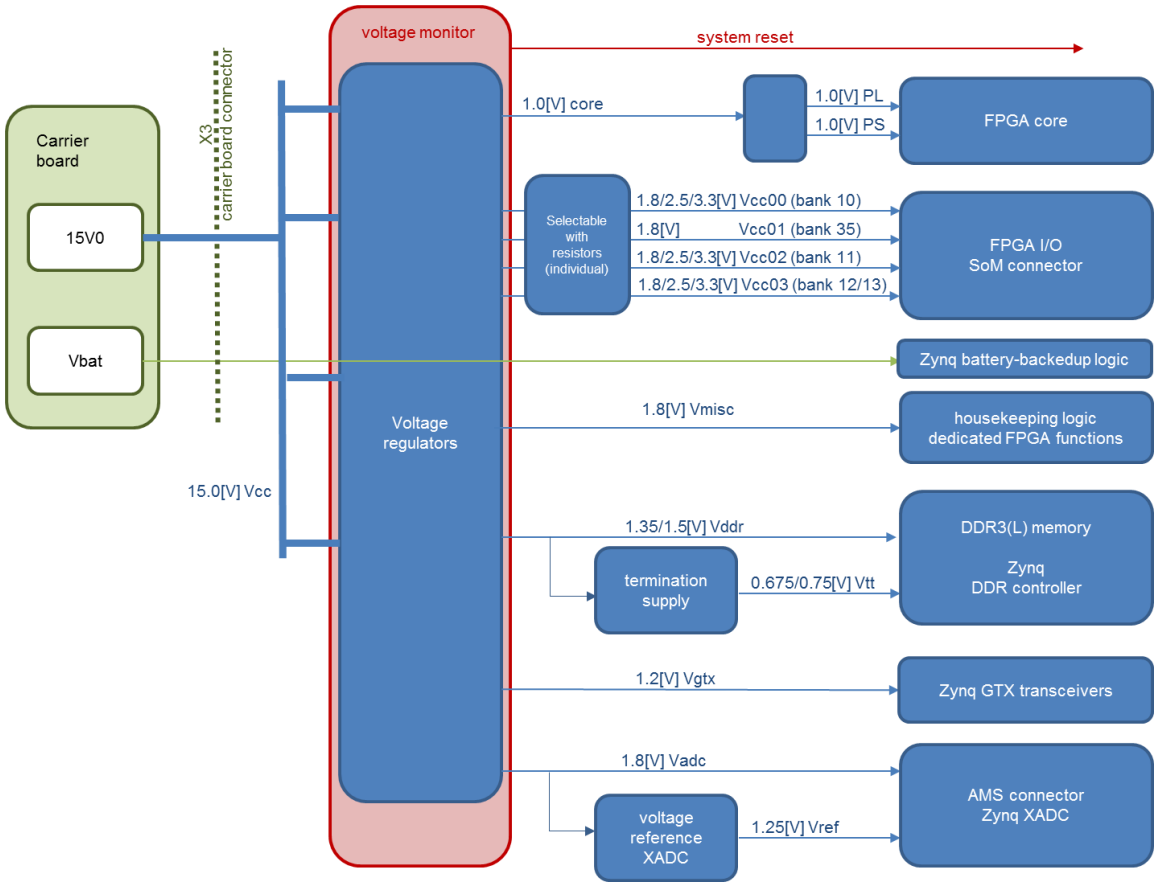
Carrier board connector X1			
Signal name	**Connector pin**	**Direction**	**Description**
Vbat	X1.6	In	Battery backed-up supply from carrier board
GND	X1.8	Ref	Supply ground reference
GND	X1.37	Ref	Supply ground reference
GND	X1.55	Ref	Supply ground reference
+1V8	X1.57	Out	Logic supply for logic level matching PS I/O bank 500 and 501 (recommended max .100[mA])
+1V8	X1.59	Out	Logic supply for logic level matching PS I/O bank 500 and 501 (recommended max. 100[mA])
+1.25A	X1.84	Out	Analogue power supply for on-board XADC
GND_XADC	X1.86	Ref	Ground reference for on-board XADC
GND	X1.93	Ref	Supply ground reference
+VCCO0	X1.95	Out	3.3V logic supply for logic level matching FPGA I/O bank 10 (recommended max.100[mA])[1)]
+VCCO1	X1.97	Out	1.8V logic supply for logic level matching FPGA I/O bank 35 (recommended max.100[mA])[1)]
+VCCO2	X1.99	Out	1.8V logic supply for logic level matching FPGA I/O bank 11 (recommended max.100[mA])[1)]
GND_XADC	X1.101	Ref	Ground reference for on-board XADC
GND	X1 ground strip	Ref	Supply ground reference

[1)] *Other configurations possible at higher volumes.*

Carrier board connector X2			
Signal name	**Connector pin**	**Direction**	**Description**
GND	X2.17	Ref	Supply ground reference
GND	X2.18	Ref	Supply ground reference
GND	X2.55	Ref	Supply ground reference
GND	X2.56	Ref	Supply ground reference
GND	X2.61	Ref	Supply ground reference for GTX transceivers
GND	X2.62	Ref	Supply ground reference for GTX transceivers
GND	X2.67	Ref	Supply ground reference for GTX transceivers
GND	X2.68	Ref	Supply ground reference for GTX transceivers
GND	X2.73	Ref	Supply ground reference for GTX transceivers
GND	X2.74	Ref	Supply ground reference for GTX transceivers
GND	X2.79	Ref	Supply ground reference for GTX transceivers
GND	X2.80	Ref	Supply ground reference for GTX transceivers
GND	X2.85	Ref	Supply ground reference for GTX transceivers
GND	X2.86	Ref	Supply ground reference for GTX transceivers
GND	X2.91	Ref	Supply ground reference for GTX transceivers
GND	X2.92	Ref	Supply ground reference for GTX transceivers
GND	X2 ground strip	Ref	Supply ground reference

Carrier board connector X3			
Signal name	**Connector pin**	**Direction**	**Description**
GND	X3.1	Ref	Supply ground reference for GTX transceivers
GND	X3.2	Ref	Supply ground reference for GTX transceivers
GND	X3.7	Ref	Supply ground reference for GTX transceivers
GND	X3.8	Ref	Supply ground reference for GTX transceivers
GND	X3.13	Ref	Supply ground reference for GTX transceivers
GND	X3.14	Ref	Supply ground reference for GTX transceivers
GND	X3.19	Ref	Supply ground reference for GTX transceivers
GND	X3.20	Ref	Supply ground reference for GTX transceivers
GND	X3.25	Ref	Supply ground reference for GTX transceivers
GND	X3.26	Ref	Supply ground reference for GTX transceivers
GND	X3.31	Ref	Supply ground reference for GTX transceivers
GND	X3.32	Ref	Supply ground reference for GTX transceivers
GND	X3.37	Ref	Supply ground reference for GTX transceivers
GND	X3.38	Ref	Supply ground reference for GTX transceivers
GND	X3.43	Ref	Supply ground reference for GTX transceivers
GND	X3.44	Ref	Supply ground reference for GTX transceivers
GND	X3.49	Ref	Supply ground reference for GTX transceivers
GND	X3.50	Ref	Supply ground reference for GTX transceivers
GND	X3.55	Ref	Supply ground reference for GTX transceivers
GND	X3.56	Ref	Supply ground reference for GTX transceivers
GND	X3.61	Ref	Supply ground reference for GTX transceivers
GND	X3.62	Ref	Supply ground reference for GTX transceivers
GND	X3.67	Ref	Supply ground reference for GTX transceivers
GND	X3.68	Ref	Supply ground reference for GTX transceivers
GND	X3.73	Ref	Supply ground reference for GTX transceivers
GND	X3.74	Ref	Supply ground reference for GTX transceivers
GND	X3.79	Ref	Supply ground reference for GTX transceivers
GND	X3.80	Ref	Supply ground reference for GTX transceivers
GND	X3.85	Ref	Supply ground reference for GTX transceivers
GND	X3.86	Ref	Supply ground reference for GTX transceivers
GND	X3.91	Ref	Supply ground reference for GTX transceivers
GND	X3.92	Ref	Supply ground reference for GTX transceivers
GND	X3.97	Ref	Supply ground reference for GTX transceivers
GND	X3.98	Ref	Supply ground reference for GTX transceivers
GND	X3.103	Ref	Supply ground reference for GTX transceivers
GND	X3.104	Ref	Supply ground reference for GTX transceivers
GND	X3.109	Ref	Supply ground reference for GTX transceivers
GND	X3.110	Ref	Supply ground reference for GTX transceivers
+VCC3	X3.125	Out	1.8V logic supply for logic level matching FPGA I/O bank 12 (recommended max.100[mA])[1)]
GND	X3.126	Ref	Supply ground reference
GND	X3.151	Ref	Supply ground reference
GND	X3.152	Ref	Supply ground reference
+15V	X3.177	In	Supply input from carrier board (max. 1[A] per pin)
+15V	X3.178	In	Supply input from carrier board (max. 1[A] per pin)
+15V	X3.179	In	Supply input from carrier board (max. 1[A] per pin)
+15V	X3.180	In	Supply input from carrier board (max. 1[A] per pin)
GND	X3 ground strip	Ref	Supply ground reference

5.5.4 Power distribution

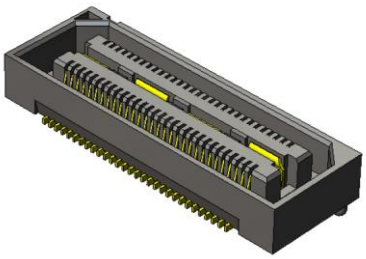


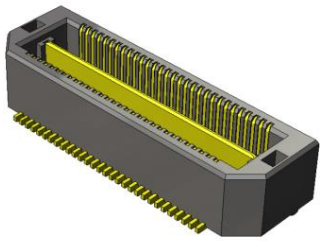
6 Connector pin assignments

The Miami+ XC7045 uses three Samtec high-speed connectors to interface with its carrier board.

6.1 X1: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm



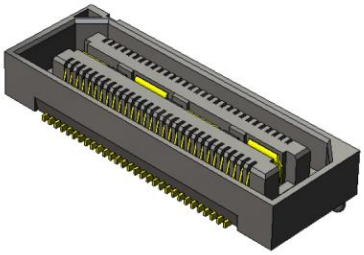


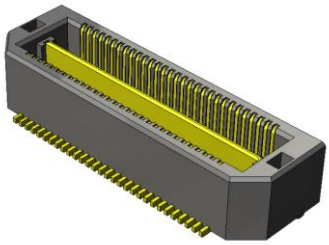
Pin	Signal	FPGA pin	Dir.	I/O level	Type		Type	I/O level	Dir.	FPGA pin	Signal	Pin
1	reserved	-	In	+3V3	PWR		PWR	+3V3	In	-	reserved	2
3	reserved	-	In	+3V3	PWR		PWR	+3V3	In	-	reserved	4
5	IO_D_VCC1_21_N	C13	I/O	+VCCO1	B35		PWR		In	-	Vbat	6
7	IO_D_VCC1_21_P	C14	I/O	+VCCO1	B35		PWR	0V	Ref	-	GND	8
9	IO_D_VCC1_22_N	A14	I/O	+VCCO1	B35		n.a.	+3V3	In	-	SOM_RST_N	10
11	IO_D_VCC1_22_P	B14	I/O	+VCCO1	B35		B35	+VCCO1	I/O	L15	IO_D_AD_VCC1_0_P	12
13	IO_D_CC_VCC1_23_N	E15	I/O	+VCCO1	B35		B35	+VCCO1	I/O	L14	IO_D_AD_VCC1_0_N	14
15	IO_D_CC_VCC1_23_P	E16	I/O	+VCCO1	B35		B35	+VCCO1	I/O	J14	IO_D_VCC1_16_P	16
17	IO_D_AD_VCC1_11_N	A17	I/O	+VCCO1	B35		B35	+VCCO1	I/O	H14	IO_D_VCC1_16_N	18
19	IO_D_AD_VCC1_11_P	B17	I/O	+VCCO1	B35		B35	+VCCO1	I/O	D15	IO_D_AD_CC_VCC1_1_P	20
21	IO_D_AD_VCC1_12_N	B12	I/O	+VCCO1	B35		B35	+VCCO1	I/O	D14	IO_D_AD_CC_VCC1_1_N	22
23	IO_D_AD_VCC1_12_P	C12	I/O	+VCCO1	B35		B35	+VCCO1	I/O	D13	IO_D_CC_VCC1_17_N	24
25	IO_D_AD_VCC1_13_N	A15	I/O	+VCCO1	B35		B35	+VCCO1	I/O	E13	IO_D_CC_VCC1_17_P	26
27	IO_D_AD_VCC1_13_P	B15	I/O	+VCCO1	B35		B35	+VCCO1	I/O	F14	IO_D_CC_VCC1_18_N	28
29	IO_D_AD_VCC1_14_N	B11	I/O	+VCCO1	B35		B35	+VCCO1	I/O	F15	IO_D_CC_VCC1_18_P	30
31	IO_D_AD_VCC1_14_P	C11	I/O	+VCCO1	B35		B35	+VCCO1	I/O	H13	IO_D_AD_VCC1_2_N	32
33	IO_D_AD_VCC1_15_P	A13	I/O	+VCCO1	B35		B35	+VCCO1	I/O	J13	IO_D_AD_VCC1_2_P	34
35	IO_D_AD_VCC1_15_N	A12	I/O	+VCCO1	B35		B35	+VCCO1	I/O	K13	IO_D_AD_VCC1_3_N	36
37	GND	-	Ref	0V	PWR		B35	+VCCO1	I/O	L13	IO_D_AD_VCC1_3_P	38
39	reserved	-	I/O	+1V8	B501		B35	+VCCO1	I/O	J15	IO_D_AD_VCC1_4_N	40
41	IO_S_VCC4_1	D19	I/O	+1V8	B501		B35	+VCCO1	I/O	K15	IO_D_AD_VCC1_4_P	42
43	reserved	-	I/O	+1V8	B501		B501	+1V8		-	V_PRESENT	44
45	IO_S_VCC4_3	C18	I/O	+1V8	B501		B501	+1V8		E20	IO_S_VCC4_4	46
47	IO_S_VCC4_5	A19	I/O	+1V8	B501		B501	+1V8		B20	IO_S_VCC4_6	48
49	IO_S_VCC4_7	F19	I/O	+1V8	B501		B501	+1V8		E18	IO_S_VCC4_8	50
51	SCL_1V8	C19	I/O	+1V8	B9		B501	+1V8		H18	IO_S_VCC4_9	52
53	SDA_1V8	D18	I/O	+1V8	B9		B501	+1V8		J18	IO_S_VCC4_10	54
55	GND	-	Ref	0V	PWR		B501	+1V8		A18	IO_S_VCC4_11	56
57	+1V8	-	Out	+1V8	PWR		B501	+1V8		D20	IO_S_VCC4_12	58
59	+1V8	-	Out	+1V8	PWR		B501	+1V8		F20	IO_S_VCC4_13	60
61	IO_S_VCC4_14	C22	Out	+1V8	B500		B11	+VCCO2	I/O	W21	IO_D_VCC2_18_P	62
63	IO_S_VCC4_15	B22	In	+1V8	B500		B11	+VCCO2	I/O	Y21	IO_D_VCC2_18_N	64
65	SW_RST_N	-	In	+3V3	n.a.		B11	+VCCO2	I/O	Y22	IO_D_VCC2_19_P	66
67	IO_S_VCC4_16	G21	I/O	+1V8	B501		B11	+VCCO2	I/O	Y23	IO_D_VCC2_19_N	68
69	IO_S_VCC4_17	B21	I/O	+1V8	B501		B11	+VCCO2	I/O	AA24	IO_D_VCC2_20_P	70
71	IO_S_VCC4_18	F18	I/O	+1V8	B501		B11	+VCCO2	I/O	AB24	IO_D_VCC2_20_N	72
73	IO_S_VCC4_19	L17	I/O	+1V8	B501		B11	+VCCO2	I/O	AA22	IO_D_VCC2_21_P	74
75	IO_S_VCC4_20	K18	I/O	+1V8	B501		B11	+VCCO2	I/O	AA23	IO_D_VCC2_21_N	76
77	IO_S_VCC4_21	A20	I/O	+1V8	B501		B11	+VCCO2	I/O	AC22	IO_D_VCC2_22_P	78
79	IO_S_VCC4_22	G22	I/O	+1V8	B501		B11	+VCCO2	I/O	AC23	IO_D_VCC2_22_N	80
81	IO_S_VCC4_23	L18	I/O	+1V8	B501		B11	+VCCO2	I/O	AF20	IO_S_CC_VCC2_0	82
83	IO_S_VCC4_24	H17	I/O	+1V8	B501		PWR	+1V25A	Out	-	+1V25A	84
85	IO_S_VCC4_25	H21	I/O	+1V8	B501		PWR	0V	Ref	-	GND_XADC	86
87	IO_S_VCC4_26	H22	I/O	+1V8	B501		B10	+VCCO0	I/O	AA13	IO_S_VCC0_0	88
89	IO_S_VCC4_27	K17	I/O	+1V8	B501		B10	+VCCO0	I/O	AE18	IO_D_VCC0_16_P	90
91	USB_RESET	-	In	+3V3	n.a.		B10	+VCCO0	I/O	AE17	IO_D_VCC0_16_N	92
93	GND	-	Ref	0V	PWR		B10	+VCCO0	I/O	AD16	IO_D_VCC0_17_P	94
95	+VCCO0	-	Out	+VCCO0	PWR		B10	+VCCO0	I/O	AD15	IO_D_VCC0_17_N	96
97	+VCCO1	-	Out	+VCCO1	PWR		B10	+VCCO0	I/O	AC14	IO_D_VCC0_18_P	98
99	+VCCO2	-	Out	+VCCO2	PWR		B10	+VCCO0	I/O	AC13	IO_D_VCC0_18_N	100
101	GND_XADC	-	Ref	0V	PWR		B10	+VCCO0	I/O	AA15	IO_D_VCC0_19_P	102
103	XADC_VP	R15	In	+1V25A	B0		B10	+VCCO0	I/O	AA14	IO_D_VCC0_19_N	104
105	XADC_VN	T14	In	+1V25A	B0		B10	+VCCO0	I/O	AC12	IO_D_VCC0_20_N	106
107	XADC_DXP	U15	In	+1V25A	B0		B10	+VCCO0	I/O	AB12	IO_D_VCC0_20_P	108
109	XADC_DXN	U14	In	+1V25A	B0		B10	+VCCO0	I/O	AB15	IO_D_VCC0_21_P	110
111	PL_JTAG_RSTN	-	In	+3V3	B0		B10	+VCCO0	I/O	AB14	IO_D_VCC0_21_N	112
113	PL_JTAG_TDI	P10	In	+3V3	B0		B10	+VCCO0	I/O	AC16	IO_D_VCC0_22_N	114
115	PL_JTAG_TMS	V10	In	+3V3	B0		B10	+VCCO0	I/O	AC17	IO_D_VCC0_22_P	116
117	PL_JTAG_TCK	Y12	In	+3V3	B0		B10	+VCCO0	I/O	AB16	IO_D_VCC0_23_N	118
119	PL_JTAG_TDO	Y10	Out	+3V3	B0		B10	+VCCO0	I/O	AB17	IO_D_VCC0_23_P	120

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

6.2 X2: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm



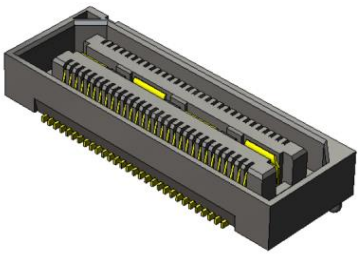


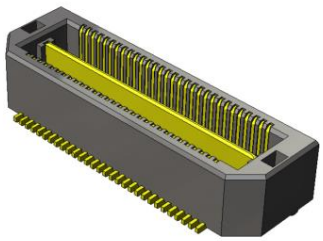
Pin	Signal	FPGA pin	Dir.	I/O level	Type		Type	I/O level	Dir.	FGPA pin	Signal	Pin
1	IO_D_AD_VCC1_5_N	G16	I/O	+VCCO1	B35		B35	+VCCO1	I/O	G15	IO_D_AD_VCC1_6_P	2
3	IO_D_AD_VCC1_5_P	G17	I/O	+VCCO1	B35		B35	+VCCO1	I/O	G14	IO_D_AD_VCC1_6_N	4
5	IO_D_AD_VCC1_7_P	G12	I/O	+VCCO1	B35		B35	+VCCO1	I/O	J16	IO_D_VCC1_19_P	6
7	IO_D_AD_VCC1_7_N	F12	I/O	+VCCO1	B35		B35	+VCCO1	I/O	H16	IO_D_VCC1_19_N	8
9	IO_D_AD_VCC1_8_N	E12	I/O	+VCCO1	B35		B35	+VCCO1	I/O	F17	IO_D_AD_VCC1_9_P	10
11	IO_D_AD_VCC1_8_P	F13	I/O	+VCCO1	B35		B35	+VCCO1	I/O	E17	IO_D_AD_VCC1_9_N	12
13	IO_D_VCC1_20_P	D16	I/O	+VCCO1	B35		B35	+VCCO1	I/O	B16	IO_D_AD_VCC1_10_N	14
15	IO_D_VCC1_20_N	C16	I/O	+VCCO1	B35		B35	+VCCO1	I/O	C17	IO_D_AD_VCC1_10_P	16
17	GND	-	Ref	0V	PWR		PWR	0V	Ref	-	GND	18
19	IO_D_VCC2_0_P	AJ25	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AK22	IO_D_VCC2_1_P	20
21	IO_D_VCC2_0_N	AK25	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AK23	IO_D_VCC2_1_N	22
23	IO_D_VCC2_2_P	AJ21	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AJ23	IO_D_VCC2_3_P	24
25	IO_D_VCC2_2_N	AK21	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AJ24	IO_D_VCC2_3_N	26
27	IO_D_CC_VCC2_4_P	AD23	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AH23	IO_D_VCC2_5_P	28
29	IO_D_CC_VCC2_4_N	AE23	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AH24	IO_D_VCC2_5_N	30
31	IO_D_VCC2_6_P	AG22	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AC24	IO_D_VCC2_7_P	32
33	IO_D_VCC2_6_N	AH22	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AD24	IO_D_VCC2_7_N	34
35	IO_D_VCC2_8_P	AG24	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AF23	IO_D_VCC2_9_P	36
37	IO_D_VCC2_8_N	AG25	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AF24	IO_D_VCC2_9_N	38
39	IO_D_VCC2_10_P	AD21	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AJ20	IO_D_VCC2_11_P	40
41	IO_D_VCC2_10_N	AE21	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AK20	IO_D_VCC2_11_N	42
43	IO_D_VCC2_12_P	AK17	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AE22	IO_D_CC_VCC2_13_P	44
45	IO_D_VCC2_12_N	AK18	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AF22	IO_D_CC_VCC2_13_N	46
47	IO_D_VCC2_14_P	AH19	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AF19	IO_D_VCC2_15_P	48
49	IO_D_VCC2_14_N	AJ19	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AG19	IO_D_VCC2_15_N	50
51	IO_D_VCC2_16_P	AB21	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AG21	IO_D_CC_VCC2_17_P	52
53	IO_D_VCC2_16_N	AB22	I/O	+VCCO2	B11		B11	+VCCO2	I/O	AH21	IO_D_CC_VCC2_17_N	54
55	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	56
57	IO_D_VCC0_0_P	AK13	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AH18	IO_D_VCC0_1_P	58
59	IO_D_VCC0_0_N	AK12	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AJ18	IO_D_VCC0_1_N	60
61	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	62
63	GTP_TX_1_P	AK6	Out	+1V2	B109		B109	+1V2	In	AF10	GTP_REF_CLK_1_P	64
65	GTP_TX_1_N	AK5	Out	+1V2	B109		B109	+1V2	In	AF9	GTP_REF_CLK_1_N	66
67	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	68
69	GTP_TX_3_P	AK2	Out	+1V2	B109		B109	+1V2	In	AE8	GTP_RX_3_P	70
71	GTP_TX_3_N	AK1	Out	+1V2	B109		B109	+1V2	In	AE7	GTP_RX_3_N	72
73	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	74
75	GTP_TX_0_P	AK10	Out	+1V2	B109		B109	+1V2	In	AH10	GTP_RX_0_P	76
77	GTP_TX_0_N	AK9	Out	+1V2	B109		B109	+1V2	In	AH9	GTP_RX_0_N	78
79	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	80
81	GTP_TX_2_P	AJ4	Out	+1V2	B109		B109	+1V2	In	AJ8	GTP_RX_1_P	82
83	GTP_TX_2_N	AJ3	Out	+1V2	B109		B109	+1V2	In	AJ7	GTP_RX_1_N	84
85	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	86
87	GTP_REF_CLK_0_P	AD10	In	+1V2	B109		B109	+1V2	In	AG8	GTP_RX_2_P	88
89	GTP_REF_CLK_0_N	AD9	In	+1V2	B109		B109	+1V2	In	AG7	GTP_RX_2_N	90
91	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	92
93	IO_D_VCC0_2_P	AJ14	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AJ16	IO_D_VCC0_3_P	94
95	IO_D_VCC0_2_N	AJ13	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AK16	IO_D_VCC0_3_N	96
97	IO_D_CC_VCC0_4_P	AE13	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AJ15	IO_D_VCC0_5_P	98
99	IO_D_CC_VCC0_4_N	AF13	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AK15	IO_D_VCC0_5_N	100
101	IO_D_CC_VCC0_6_P	AF14	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AH17	IO_D_VCC0_7_P	102
103	IO_D_CC_VCC0_6_N	AG14	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AH16	IO_D_VCC0_7_N	104
105	IO_D_VCC0_8_P	AE12	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AH14	IO_D_VCC0_9_P	106
107	IO_D_VCC0_8_N	AF12	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AH13	IO_D_VCC0_9_N	108
109	IO_D_CC_VCC0_10_P	AG17	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AD14	IO_D_VCC0_11_P	110
111	IO_D_CC_VCC0_10_N	AG16	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AD13	IO_D_VCC0_11_N	112
113	IO_D_VCC0_12_P	AG12	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AF18	IO_D_VCC0_13_P	114
115	IO_D_VCC0_12_N	AH12	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AF17	IO_D_VCC0_13_N	116
117	IO_D_CC_VCC0_14_P	AF15	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AE16	IO_D_VCC0_15_P	118
119	IO_D_CC_VCC0_14_N	AG15	I/O	+VCCO0	B10		B10	+VCCO0	I/O	AE15	IO_D_VCC0_15_N	120

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

6.3 X3: Carrier board connector pinning

Part type	Samtec, QSH-090-01-L-D-A, High Speed ground plane socket, 180 pins (3x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-090-01-L-D-A, High Speed ground plane socket, 180 pins (3x60), stacking height 5mm





Pin	Signal	FPGA pin	Dir.	I/O level	Type		Type	I/O level	Dir.	FGPA pin	Signal	Pin
1	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	2
3	MGT_RX_4_P	AH6	In	+1V2	B110		B110	+1V2	In	AG4	MGT_RX_5_P	4
5	MGT_RX_4_N	AH5	In	+1V2	B110		B110	+1V2	In	AG3	MGT_RX_5_N	6
7	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	8
9	MGT_RX_6_P	AF6	In	+1V2	B110		B110	+1V2	In	AD6	MGT_RX_7_P	10
11	MGT_RX_6_N	AF5	In	+1V2	B110		B110	+1V2	In	AD5	MGT_RX_7_N	12
13	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	14
15	MGT_TX_4_P	AH2	Out	+1V2	B110		B110	+1V2	Out	AF2	MGT_TX_5_P	16
17	MGT_TX_4_N	AH1	Out	+1V2	B110		B110	+1V2	Out	AF1	MGT_TX_5_N	18
19	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	20
21	MGT_TX_6_P	AE4	Out	+1V2	B110		B110	+1V2	Out	AD2	MGT_TX_7_P	22
23	MGT_TX_6_N	AE3	Out	+1V2	B110		B110	+1V2	Out	AD1	MGT_TX_7_N	24
25	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	26
27	MGT_D_REFCLK_2_P	AA8	In	+1V2	B110		B111	+1V2	In	AC4	MGT_RX_8_P	28
29	MGT_D_REFCLK_2_N	AA7	In	+1V2	B110		B111	+1V2	In	AC3	MGT_RX_8_N	30
31	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	32
33	MGT_RX_9_P	AB6	In	+1V2	B111		B111	+1V2	In	Y6	MGT_RX_10_P	34
35	MGT_RX_9_N	AB5	In	+1V2	B111		B111	+1V2	In	Y5	MGT_RX_10_N	36
37	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	38
39	MGT_RX_11_P	AA4	In	+1V2	B111		B111	+1V2	Out	AB2	MGT_TX_8_P	40
41	MGT_RX_11_N	AA3	In	+1V2	B111		B111	+1V2	Out	AB1	MGT_TX_8_N	42
43	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	44
45	MGT_TX_9_P	Y2	Out	+1V2	B111		B111	+1V2	Out	W4	MGT_TX_10_P	46
47	MGT_TX_9_N	Y1	Out	+1V2	B111		B111	+1V2	Out	W3	MGT_TX_10_N	48
49	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	50
51	MGT_TX_11_P	V2	Out	+1V2	B111		B111	+1V2	In	U8	MGT_D_REFCLK_3_P	52
53	MGT_TX_11_N	V1	Out	+1V2	B111		B111	+1V2	In	U7	MGT_D_REFCLK_3_N	54
55	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	56
57	MGT_RX_12_P	V6	In	+1V2	B112		B112	+1V2	In	U4	MGT_RX_13_P	58
59	MGT_RX_12_N	V5	In	+1V2	B112		B112	+1V2	In	U3	MGT_RX_13_N	60
61	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	62
63	MGT_RX_14_P	T6	In	+1V2	B112		B112	+1V2	In	P6	MGT_RX_15_P	64
65	MGT_RX_14_N	T5	In	+1V2	B112		B112	+1V2	In	P5	MGT_RX_15_N	66
67	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	68
69	MGT_TX_12_P	T2	Out	+1V2	B112		B112	+1V2	Out	R4	MGT_TX_13_P	70
71	MGT_TX_12_N	T1	Out	+1V2	B112		B112	+1V2	Out	R3	MGT_TX_13_N	72
73	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	74
75	MGT_TX_14_P	P2	Out	+1V2	B112		B112	+1V2	Out	N4	MGT_TX_15_P	76
77	MGT_TX_14_N	P1	Out	+1V2	B112		B112	+1V2	Out	N3	MGT_TX_15_N	78
79	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	80
81	MGT_D_REFCLK_4_P	N8	Out	+1V2	B112		-	-	-	-	reserved	82
83	MGT_D_REFCLK_4_N	N7	Out	+1V2	B112		-	-	-	-	reserved	84
85	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	86
87	reserved	-	-	-	-		-	-	-	-	reserved	88
89	reserved	-	-	-	-		-	-	-	-	reserved	90
91	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	92
93	reserved	-	-	-	-		-	-	-	-	reserved	94
95	reserved	-	-	-	-		-	-	-	-	reserved	96
97	GND	-	Ref	V0	PWR		PWR	V0	-	-	GND	98
99	reserved	-	-	-	-		-	-	-	-	reserved	100
101	reserved	-	-	-	-		-	-	-	-	reserved	102
103	GND	-	Ref	V0	PWR		PWR	V0	-	-	GND	104
105	reserved	-	-	-	-		-	-	-	-	reserved	106
107	reserved	-	-	-	-		-	-	-	-	reserved	108
109	GND	-	Ref	V0	PWR		PWR	V0	-	-	GND	110
111	IO_S_VCC4_28	L19	I/O	+1V8	B501		B501	+1V8	I/O	K21	IO_S_VCC4_29	112
113	IO_S_VCC4_30	K20	I/O	+1V8	B501		B501	+1V8	I/O	J20	IO_S_VCC4_31	114
115	IO_S_VCC4_32	M20	I/O	+1V8	B501		B501	+1V8	I/O	L20	IO_S_VCC4_33	116
117	IO_S_VCC4_34	J21	I/O	+1V8	B501		B501	+1V8	I/O	M19	IO_S_VCC4_35	118
119	IO_S_VCC4_36	G19	I/O	+1V8	B501		B501	+1V8	I/O	M17	IO_S_VCC4_37	120
121	IO_S_VCC4_38	J19	I/O	+1V8	B501		B501	+1V8	I/O	G20	IO_S_VCC4_39	122
123	Reserved	-	-	+1V2	-		-	-	-	-	Reserved	124
125	+VCC3	-	Out	+VCC3	PWR		PWR	V0	Ref	-	GND	126

Pin	Signal	FPGA pin	Dir.	I/O level	Type		Type	I/O level	Dir.	FGPA pin	Signal	Pin
127	IO_D_CC_VCC3_0_P	AB27	I/O	+VCC3	B12		B12	+VCC3	I/O	AC28	IO_D_CC_VCC3_1_P	128
129	IO_D_CC_VCC3_0_N	AC27	I/O	+VCC3	B12		B12	+VCC3	I/O	AD28	IO_D_CC_VCC3_1_N	130
131	IO_D_CC_VCC3_2_P	AE28	I/O	+VCC3	B12		B12	+VCC3	I/O	AE27	IO_D_CC_VCC3_3_P	132
133	IO_D_CC_VCC3_2_N	AF28	I/O	+VCC3	B12		B12	+VCC3	I/O	AF27	IO_D_CC_VCC3_3_N	134
135	IO_D_VCC3_4_P	AF29	I/O	+VCC3	B12		B12	+VCC3	I/O	AF30	IO_D_VCC3_5_P	136
137	IO_D_VCC3_4_N	AG29	I/O	+VCC3	B12		B12	+VCC3	I/O	AG30	IO_D_VCC3_5_N	138
139	IO_D_VCC3_6_P	AG26	I/O	+VCC3	B12		B12	+VCC3	I/O	AE25	IO_D_VCC3_7_P	140
141	IO_D_VCC3_6_N	AG27	I/O	+VCC3	B12		B12	+VCC3	I/O	AF25	IO_D_VCC3_7_N	142
143	IO_D_VCC3_8_P	AH28	I/O	+VCC3	B12		B12	+VCC3	I/O	AJ30	IO_D_VCC3_9_P	144
145	IO_D_VCC3_8_N	AH29	I/O	+VCC3	B12		B12	+VCC3	I/O	AK30	IO_D_VCC3_9_N	146
147	IO_D_VCC3_10_P	AJ28	I/O	+VCC3	B12		B12	+VCC3	I/O	AK27	IO_D_VCC3_11_P	148
149	IO_D_VCC3_10_N	AJ29	I/O	+VCC3	B12		B12	+VCC3	I/O	AK28	IO_D_VCC3_11_N	150
151	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	152
153	IO_D_CC_VCC3_12_P	U25	I/O	+VCCO0	B13		B13	+VCC3	I/O	U26	IO_D_CC_VCC3_13_P	154
155	IO_D_CC_VCC3_12_N	V26	I/O	+VCCO0	B13		B13	+VCC3	I/O	U27	IO_D_CC_VCC3_13_N	156
157	IO_D_CC_VCC3_14_P	R25	I/O	+VCCO0	B13		B13	+VCC3	I/O	R27	IO_D_CC_VCC3_15_P	158
159	IO_D_CC_VCC3_14_N	R26	I/O	+VCCO0	B13		B13	+VCC3	I/O	T27	IO_D_CC_VCC3_15_N	160
161	IO_D_VCC3_16_P	N26	I/O	+VCCO0	B13		B13	+VCC3	I/O	P25	IO_D_VCC3_17_P	162
163	IO_D_VCC3_16_N	N27	I/O	+VCCO0	B13		B13	+VCC3	I/O	P26	IO_D_VCC3_17_N	164
165	IO_D_VCC3_18_P	T24	I/O	+VCCO0	B13		B13	+VCC3	I/O	P23	IO_D_VCC3_19_P	166
167	IO_D_VCC3_18_N	T25	I/O	+VCCO0	B13		B13	+VCC3	I/O	P24	IO_D_VCC3_19_N	168
169	IO_D_VCC3_20_P	P21	I/O	+VCCO0	B13		B13	+VCC3	I/O	T22	IO_D_VCC3_21_P	170
171	IO_D_VCC3_20_N	R21	I/O	+VCCO0	B13		B13	+VCC3	I/O	T23	IO_D_VCC3_21_N	172
173	IO_D_VCC3_22_P	R22	I/O	+VCCO0	B13		B13	+VCC3	I/O	U22	IO_D_VCC3_23_P	174
175	IO_D_VCC3_22_N	R23	I/O	+VCCO0	B13		B13	+VCC3	I/O	V22	IO_D_VCC3_23_N	176
177	+15V	-	In	+15V	PWR		PWR	+15V	In	-	+15V	178
179	+15V	-	In	+15V	PWR		PWR	+15V	In	-	+15V	180

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

7 Electrical characteristics

7.1 Electrical specifications

Supply voltage	15.0 [V], +/- 5%
Current consumption	2.0 [A] typically

7.2 Environment specifications

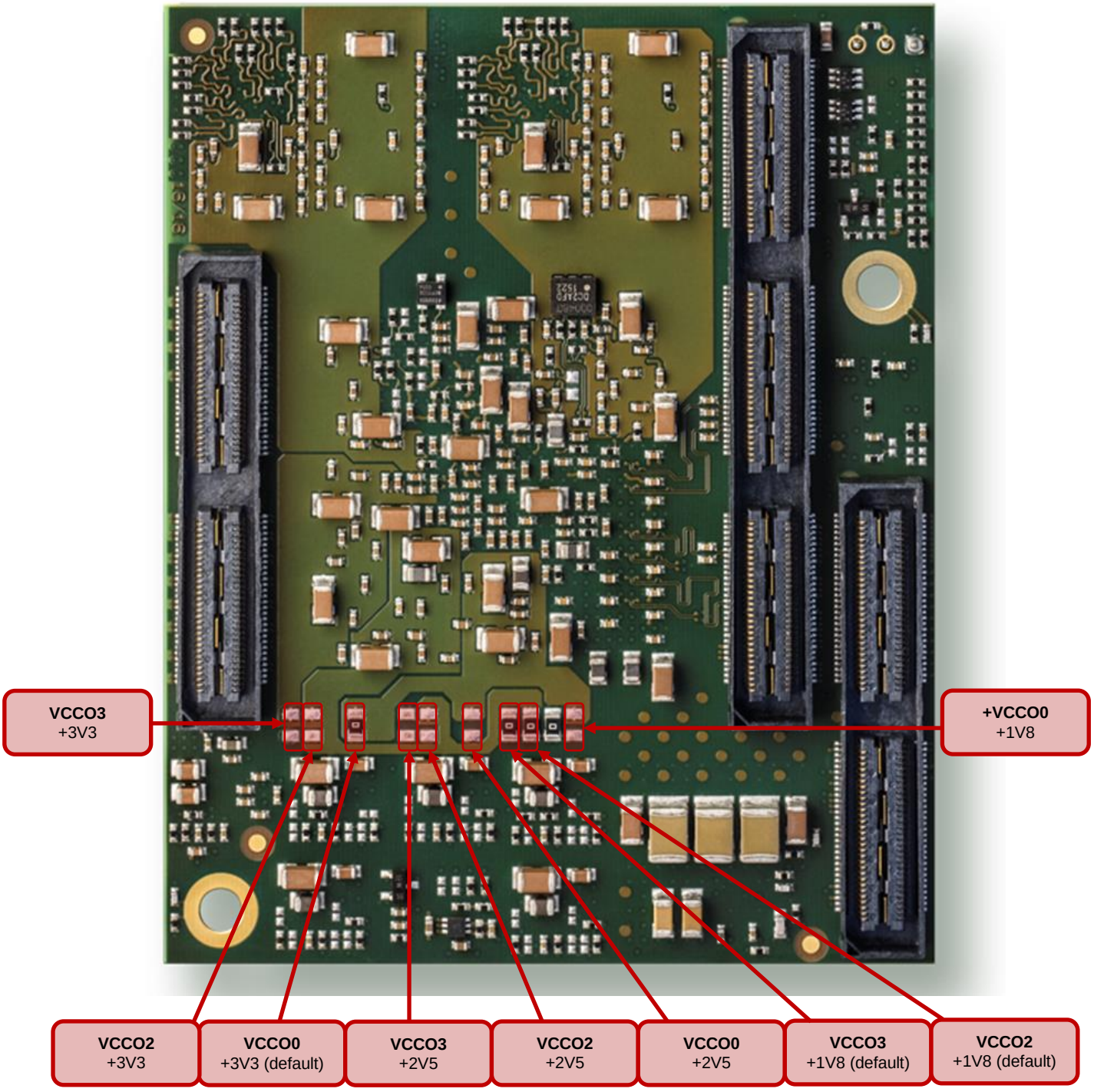
Extended operating temperature	-40 … +85[°C]
Storage temperature	-40 … +125[°C]
Relative humidity	0 … 95%, non-condensing

7.3 Mechanical specifications

Weight	approximately 20 [gram]
Board	glass epoxy FR-4, UL-listed, 12 layers, 1.6 [mm]
Dimensions	85[mm] x 68.5 [mm] x 10.0 [mm] (length x width x height)

7.4 Regulatory conformation

CE (EMC, EMI)	Report available on request
Temperature and humidity	Report available on request
RoHS	All applied components, printed circuit board material, production of the printed circuit board as well as the assembly of the boards are conducted in compliance with the RoHS legislation.


VCCO3
+3V3
+VCCO0
+1V8
VCCO2
+3V3
VCCO0
+3V3 (default)
VCCO3
+2V5
VCCO2
+2V5
VCCO0
+2V5
VCCO3
+1V8 (default)
VCCO2
+1V8 (default)