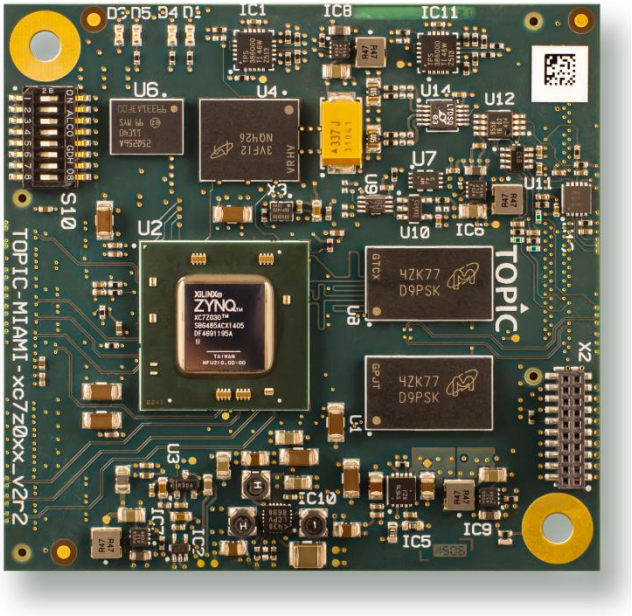
Miami Zynq SOM 7012S/7015/7030

Product Guide

V2R2 / 2021-04-08 / Rev. B



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1 Introduction

The Miami Zynq System-on-Module (SOM) processor module is a 68.4x65.0mm sized CPU board based on the Xilinx Zynq XC7Z012S, XC7Z015 or XC7Z030 processors. All Zynq devices include a single or dual-core ARM Cortex A9 processor integrated with FPGA fabric, adding programmable logic and high-performance computing capabilities to the processor platform. The XC7Z012S and XC7Z015 processor are based on Artix FPGA technology, providing flexible I/O technology and DSP capabilities with over 200GMAC fixed-point operations per second. The XC7Z030 high-performance processor is based on Kintex FPGA technology, adding a logic density, higher clock rates and increased DSP performance up to 600GMAC fixed-point operations per second.

The processor cores run up to 800MHz (depending on the speed grade) and include a variety of functions required for multimedia, medical or industrial applications. These include encryption, encoding, accelerators, display interface, camera interfacing, LVDS interfaces, audio interfaces and general purpose inputs and outputs.

When placing a production order of 50 units or more, the modules can be ordered with different sizes of flash memory, DDR-SDRAM and several configuration options. The SoM provides support for several standard interfaces, such as Ethernet, USB 2.0, SDIO, PCI-Express and SATA2 or SATA3.

All interfaces are accessible through the two 120 pins high-performance Samtec connectors. An additional connector is available for specific purposes, such as debugging, programming and configuration.

Typical power consumption of the whole board is around 5W for the XC7Z012S/XC7Z015 versions and around 7W for the XC7Z030 version. Passive and active cooling precautions can be put in place to support thermal conduction measures suitable for the target application.

The Miami Zynq SoM is supported by means of a Florida GEN carrier board, forming a development kit. The kit consists of a Florida-GEN board, a Miami Zynq SoM 7030 and all cabling to start your development instantly. It has support for Dyplo, an operating system that extends into the FPGA and providing software like capabilities by exploring partial reconfiguration of the FPGA fabric from software application level.

Refer to the Florida GEN product guide for more details on the board.

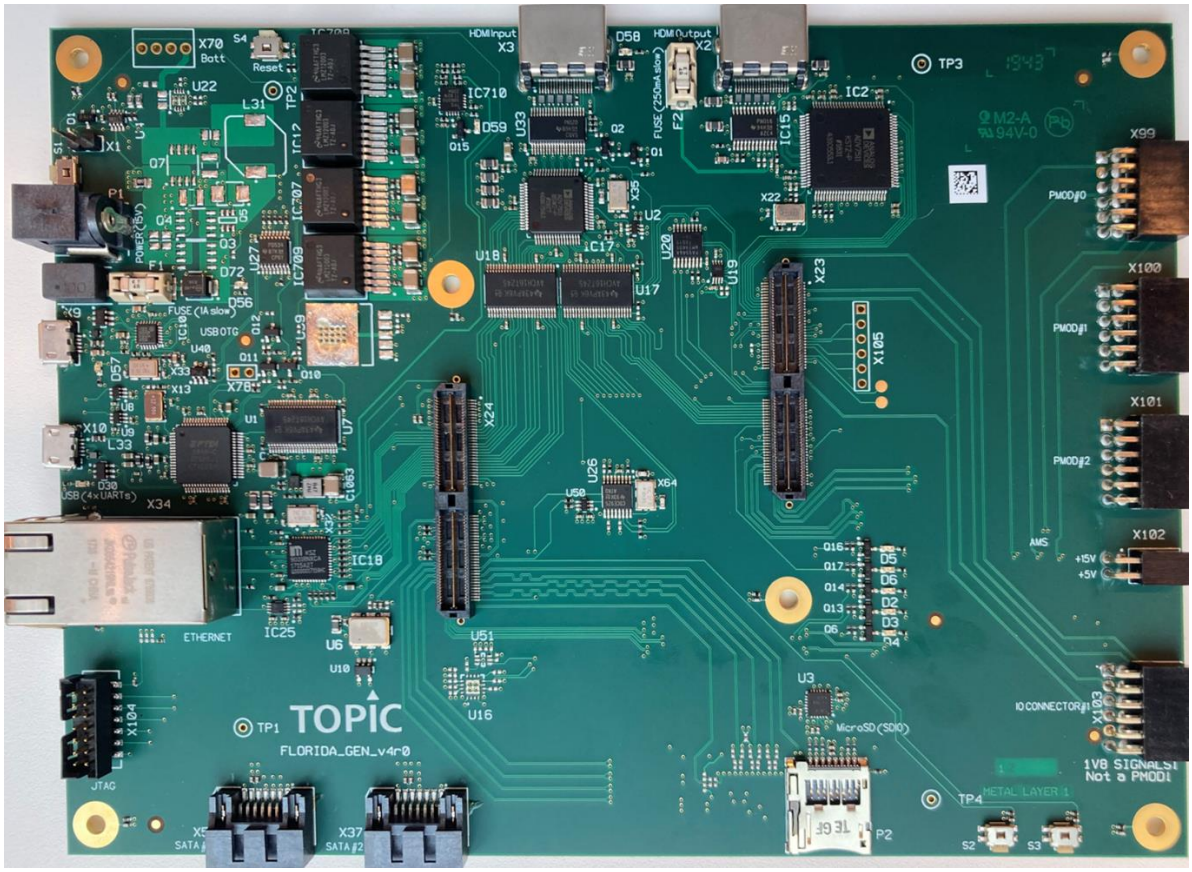


Figure 1 FLORIDA-GEN CARRIER BOARD

2 Installation

The Miami System-on-Modules are delivered with a pre-installed Linux distribution, executed from the NOR flash memory. Powering the board by connecting a debug expansion board or mounting the Miami on a custom carrier board or a Florida evaluation board will automatically boot the Miami board from the NOR flash and gives you a command prompt on the terminal port.

2.1 Software installation

The Miami Zynq SoM comes with a Linux distribution, which can be downloaded from GitHub:

https://github.com/topic-embedded-products/topic-platform

This is an easy starting point for developing your own applications. When accessing this website, you are guided through the steps to download, install and start using the software. The Linux distribution contains:

- Linux configuration and development tools
- Cross compiler for the Zynq/Cortex-A9 processor
- BSP with drivers for all peripherals on the Miami SoMs (including the PCAP to program the FPGA)
- Simple example program for getting started

The Miami Zynq SoMs are not dependent on versions of Vivado tooling. However, example FPGA images are available for Vivado 2018.2 and higher.

For any help or support, please contact us at support@TopicProducts.com.

3 Miami SoM features

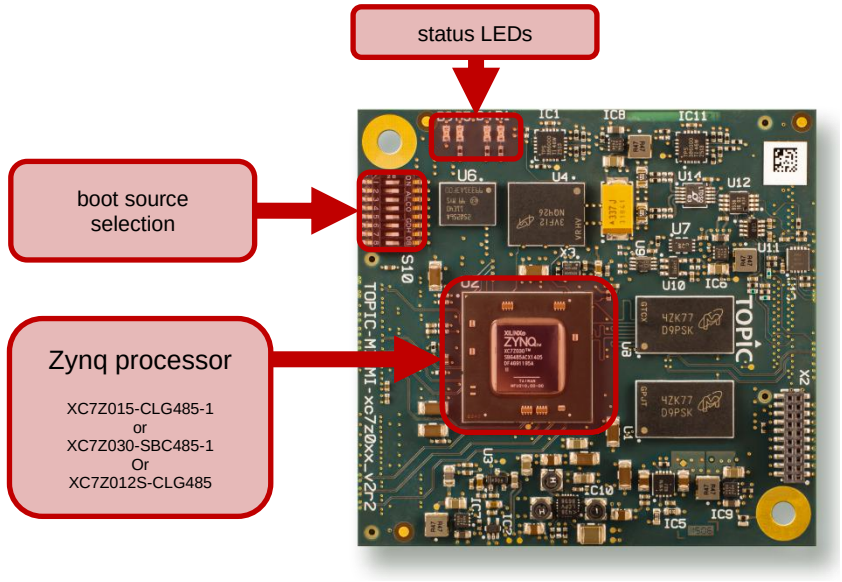
	SOM-MIAMI-XC7015	SOM-MIAMI-XC7030
PROCESSOR SYSTEM		
Processor [1)]	XC7Z015-CLG485-1	XC7Z030-SBG485-1
CPU Architecture	ARM Cortex-A9 (dual core)	
CPU Performance	2x 666MHz	2x 666MHz
Co-Processor	2x ARM NEON™	
MEMORY		
Cache	L1: 32KB instruction/core, 32KB data/core, L2: 512KB	
SDRAM [1)]	DDR3/DDR3L @ 533MHz, 1024 MB	
NOR [1)]	Quad-speed SPI, 32MB	
EEPROM	4 Kb for parameter and production data storage	
FPGA		
Technology	Artix®-7	Kintex®-7
Logic cells	74K	125K
LUTs	46.200	78.600
Flip Flops	92.400	157.200
RAM	410KB	1.160MB
DSP slices	160	400
GTP/GTX transceivers	4x (3.75 Gb/s each)	4x (6.6 Gb/s each)
2x120 pins available on SOM connector for programmable interfaces		
LAN	10/100/1000Mbps Ethernet, additional RMII interface	
Analog	Up to 8 channels differential, 12 bits	
Serial	UART, I2C, SPI, I2S, user defined	
Video	LVDS, SDI, TFT, VGA, LCD	
USB	USB OTG 2.0	
Debug	Debug UART, console	
Miscellaneous	GPIOs SD/SDIO 2.0/MMC 3.31 compliant controllers	
Dedicated interfaces on SOM connector		
Network	1000Mbps Ethernet	
USB	USB OTG 2.0	
SATA	SATA-3	
JTAG	PL JTAG chain for carrier board programming	
Power supply		
Input	3.3V via connector On-board voltage regulation	
Output	Programmable I/O standards and voltages	
Control	Current measurement for PL and PS	
Software		
Bootloader / BSP	U-Boot	
Boot options	JTAG, NOR, (external) SD-Card	
Operating System	Topic Linux 4.x distribution on GitHub	
Dyplo® compatible platform	Yes	Yes
Mechanical and environmental		
Dimensions	65mm x 68.4mm	
Connectors	2x 120 pins Samtec high performance mezzanine carrier board connectors	
Temperature	Industrial grade	

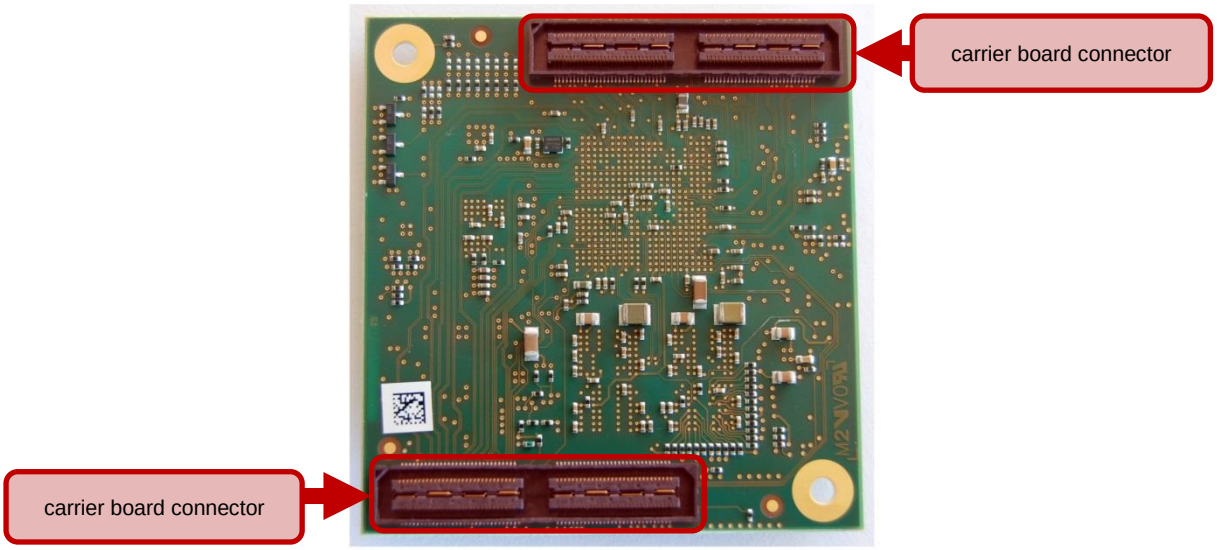
[1)] Other configurations possible at higher volumes.

4 Miami SoM architecture

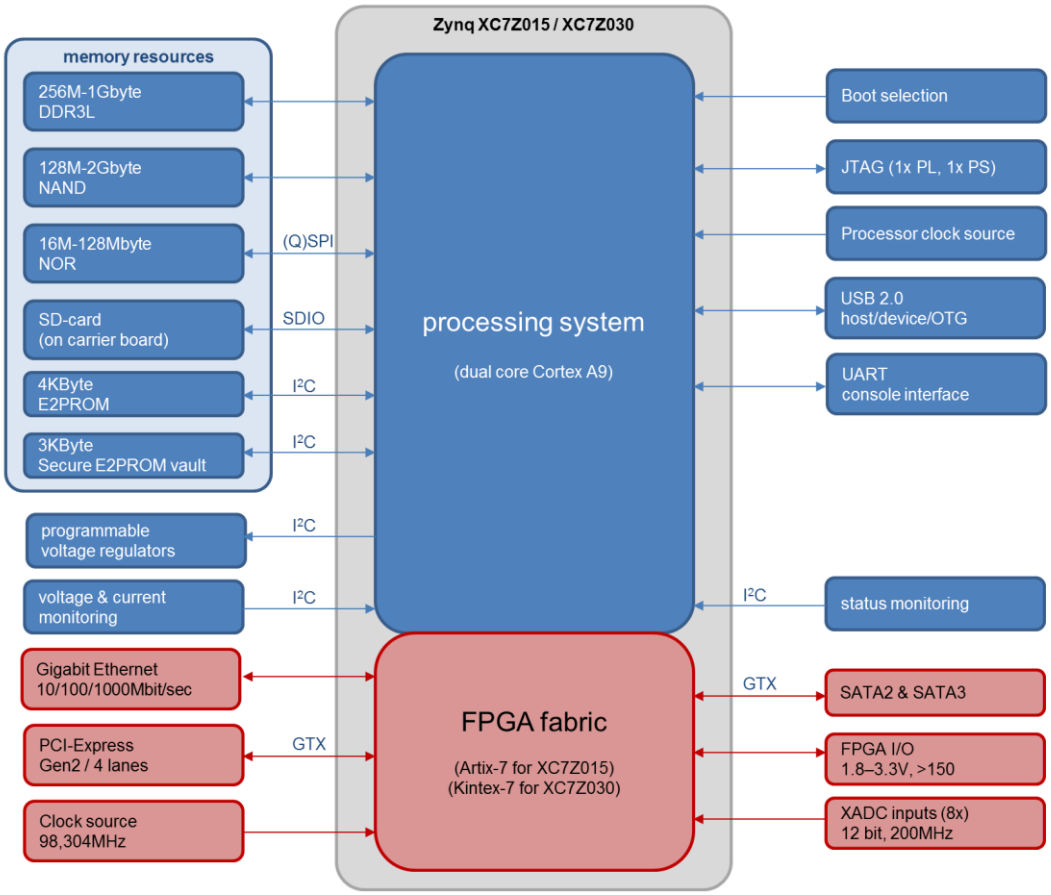
The Miami System-on-Module integrates all peripherals to bring up a full functional processing system. The system connects to the carrier board using two high performance connectors and allows connection of a debug extension board. The following paragraphs give an overview of peripherals and devices which determine the functionality of the board.

4.1 Miami SoM board layout





4.2 Block diagram

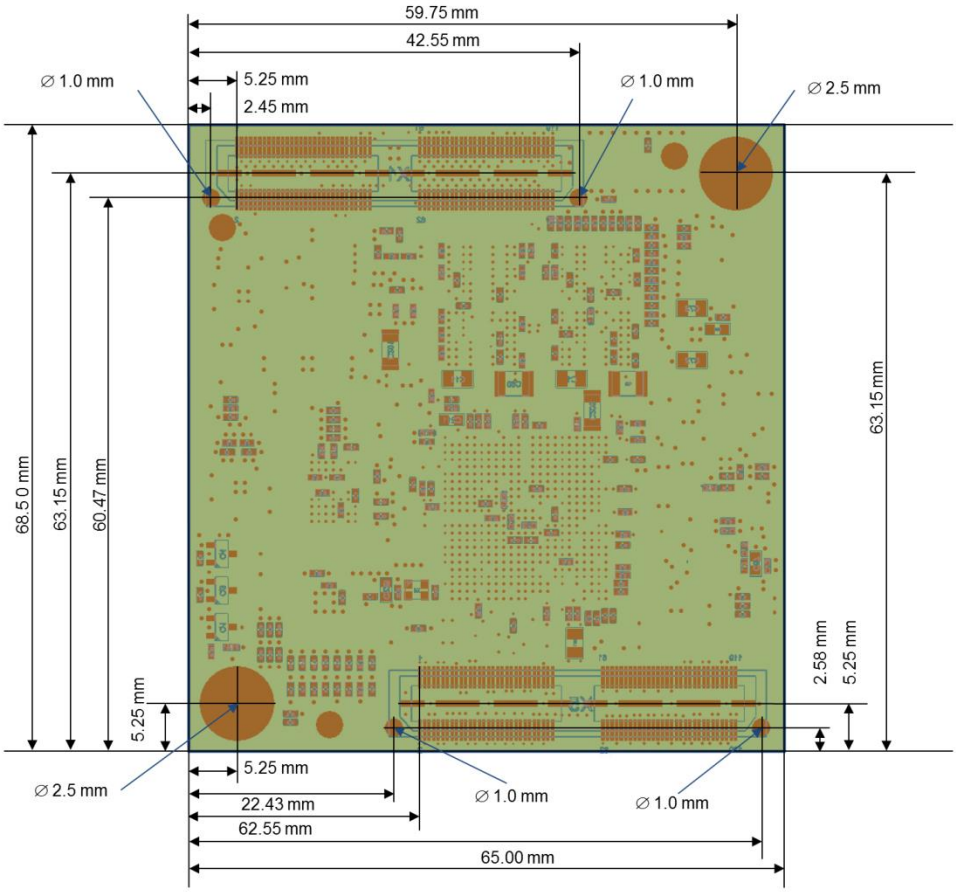


4.3 Mechanical description

The Miami should be fitted on a carrier board using two mating connectors:

Part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm

The exact relative placement details of the connectors, the guide holes for the connectors and the fixation standoff holes are described in the following figure. The exact measurement details can be downloaded from the support website as a DXF object to match the Miami SoM exactly on your carrier board layout placement plan.
An .IDF 3D file is also available, to see how the Miami Zynq SOM module fits in your mechanical environment



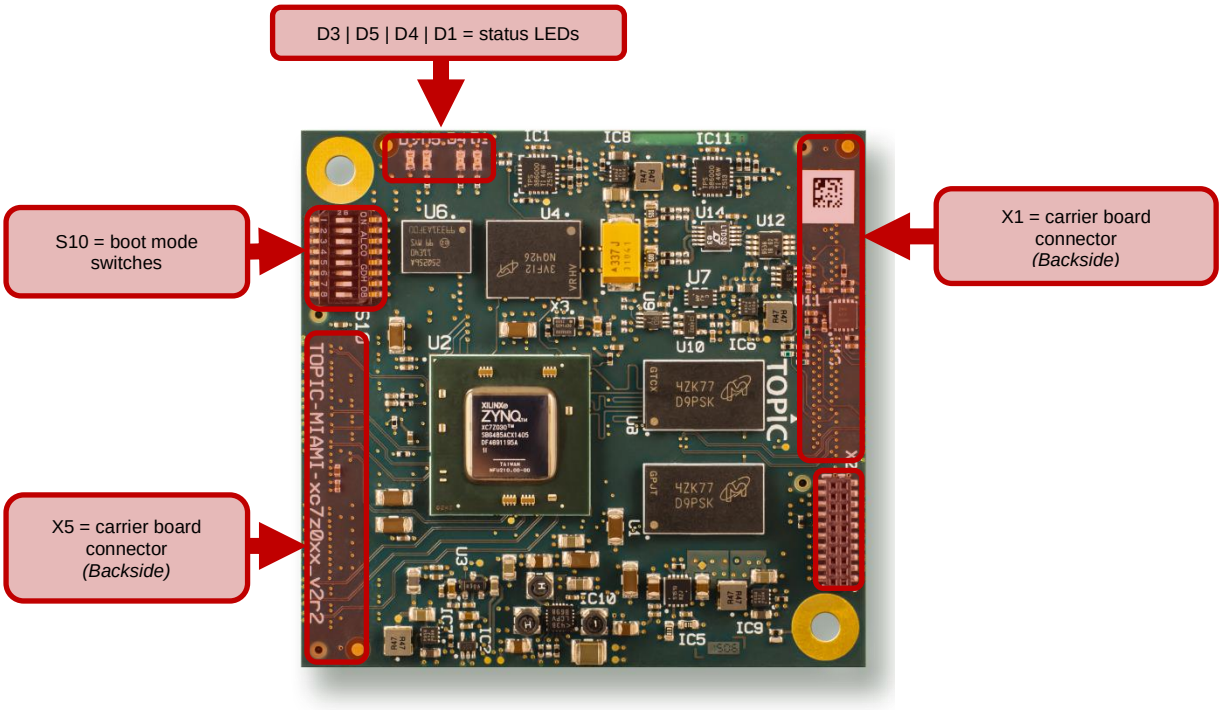
5 Miami SoM board functionality

The functionality of the SoM module can be divided in different function groups:

- Configuration and debug interfaces
- Memory resources
- Communication interfaces
- Miscellaneous functionality
- Power supplies and system integrity

In the following paragraphs the functions will be explained from a user perspective to help understand the context to use and program the functionality.

5.1 Configuration and debug interfaces



5.1.1 Status LEDs

There are 4 status LEDs provided on the Miami boards. These are indicating the operational status of the board from a system and user perspective.

LED reference	FPGA pin	Description
D3	n.a.	Power-good LED. When active, the primary power supplies on the board are up and within operational limits. When the Miami board is powered by 3.3[V] this must be the case.
D4	n.a.	FPGA image not ready. When active, the FPGA part of the Zynq is not loaded yet. When programmed with a valid bit stream, the LED will be off.
D5	F11 (IO-O-13)	CPU alive LED. This LED is controlled by the processor system. By default a heartbeat signal is applied to the LED to indicate proper operation of the software. However, the LED is available for the user to give it a different function.
D1	T16 (PS-MIO25-501)	FPGA user LED. By default this LED will be off. However, the LED is available for the user to give it a different function.

5.1.2 Boot mode selection switches

The first stage boot loader of the processor is able to boot the initial boot code from a selectable source: JTAG, NOR memory, NAND memory of from SD-card. This boot mode strapping is configurable using an 8 positions dipswitch S10 or via a configurable resistor bank. The last option is available as customization option.

Switch S10 settings *(sw1 to sw8)*	**Boot mode**	**Comment**
1 0 1 0 0 1 x x	JTAG	The dip switches control the state of the FPGA boot mode selection signals, located on the FPGA on pin A20 (PS-MIO5-500), F17 (PS_MIO3-500), E19 (PS-MIO4-500) and A21 (PS-MIO2-500). These are only used during power-up state. Otherwise the functionality is shared with the quad SPI and memory controller.
1 0 0 1 0 1 x x	QSPI NOR flash	
0 1 1 0 0 1 x x	NAND flash	
0 1 0 1 0 1 x x	SD-Card flash	
x x x x x x 1 0	JTAG (PL/PS) in cascaded mode	
x x x x x x 0 1	JTAG (PL/PS) in independent mode	
other combinations	Invalid, undefined behavior	

Another boot mode option is the signaling of the supply voltage on the MIO banks 500 and 501 of the processing system. Both banks are configured as 1.8 [V] banks, which is fixed in the Miami context. Another boot mode option is the bypassing of the PLL. This is a customization option, not a dynamic configuration item on the Miami.

Refer to Xilinx document UG585 (Zynq technical reference guide) chapter 6 for more details on booting strategies.

5.1.3 JTAG interfaces

The Zynq processor of Xilinx has two JTAG ports:

- PL_JTAG. This is the default JTAG port, connected to the dedicated JTAG pins on the Zynq. It is using 3.3[V] signal levels. The applicable pull-up resistors are integrated on the Miami board. Using the PL-JTAG port you can:
  - Program the FPGA fabric
  - Use the ChipScope logic analyzer to debug the programmed FPGA logic
  - Boundary scan for production verification
  - Debug the processor software using the ARM CoreSight Debug Access Port (DAP)

PL_JTAG signals	FPGA pin	Description
TDI	H9 (TDI_O)	Dedicated package pin
TDO	G9 (TDO_O)	Dedicated package pin
TCK	H11 (TCK_O)	Dedicated package pin
TMS	H10 (TMS_O)	Dedicated package pin

- PS_JTAG. This additional JTAG port is provided to be able to have two debuggers simultaneously access the processor system and the FPGA fabric. This gives some unique debug capabilities. *Refer to the ARM Development Studio 5 product information for more details*. On the Miami SoMs the PS-JTAG signals are connected to the pins described in the following table. When not required, the PS_JTAG signals can be applied to assign different functionality. The signal levels are fixed at 1.8[V].

PS_JTAG signals	FPGA pin	Description
TDI	D11 (PS-MIO46-501)	When not used for debugging purposes, this pin is available as direct processor controlled signals.
TDO	B13 (PS-MIO47-501)	When not used for debugging purposes, this pin is available as direct processor controlled signals.
TCK	D12 (PS-MIO48-501)	When not used for debugging purposes, this pin is available as direct processor controlled signals.
TMS	C9 (PS-MIO49-501)	When not used for debugging purposes, this pin is available as direct processor controlled signals.

5.1.4 Console interfaces

A primary software development interface is the console connection with the processing system. The Miami provides a fixed console connection directly on the MIO port of the processing system.

Console signals	FPGA pin	Description
UART_RXD	A10 (PS_MIO26_501_O)	Serial data from processor to other device. Can be used for other functionality if needed.
UART_TXD	D16 (PS_MIO27_502_O)	Serial data from other device to processor. Can be used for other functionality if needed.

The console signals are available on the both the carrier board connector X1 and debug expansion header X2. The signals are provided 1.8[V] CMOS logic levels compatible. Make sure that you implement provisions when allowing simultaneous access to the console signals using the debug expansion header in combination with a carrier board. The console interface runs on a default 115200 baud rate, 8 data bits, 1 stop bit and no parity or flow control.

Console signal	Connector pin	FPGA pin	Description
UART_RXD	X1.63	A10	Shared signal with X2.14
UART_RXD	X2.14	A10	Shared signal with X1.63
UART_TXD	X1.61	D16	Shared signal with X2.7
UART_TXD	X2.7	D16	Shared signal with X1.61

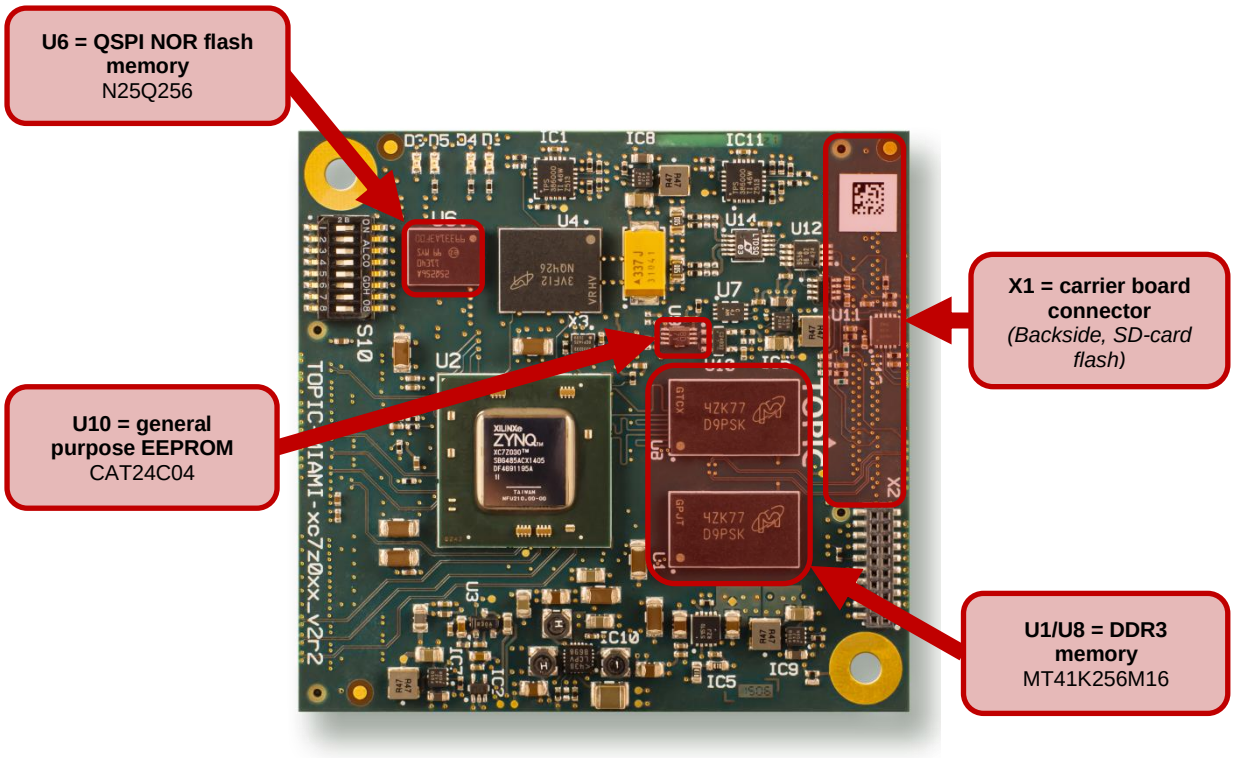
5.1.5 Resetting the Miami SOM

The Miami Zynq facilitates different reset options (all signals are active low). See the table below.

Pin label	Connector pin	Description
SOM_RST_N	X1.10	Hardware reset signal of the SOM, this pin activates the POR Reset (PS_POR_B_500 FPGA pin) of the FPGA.
SW_RST_N	X1.65	An active signal on these pins activates the non-POR Reset (debug mode) (PS_SRST_B_500 FPGA pin) of the FPGA.
PL_JTAG_RST_N	X1.111	
USB_RESET	X1.91	Reset signal intended for resetting USB devices. If not used, this signal can be used for I/O purposes.

Refer to Xilinx document UG585 (Zynq technical reference guide) for more details on resetting sources.

5.2 Memory resources



5.2.1 DDR3 SDRAM memory (MT41K256M16)

A low-power DDR3 SDRAM memory solution is provided as the main background memory. The RAM memory has a 32-bit interface and can be clocked up to 533 [MHz]. The DDR clock frequency is configured by the software configuration using PLL1 clock output 2, which the standard DDR clock output. The SDRAM memory size can be ordered[1] in sizes of 256[MB], 512[MB] and 1[GB] (default).

The solution is build using two 16-bit wide DDR3 memory chips (Micron MT41K256M16). The devices are connected to the dedicated DDR memory controller interface on the Zynq. They can be supplied by a 1.5[V] (default) or a 1.35[V] supply. The supply level is a hard-configuration option[2] of the module.

[1] *Minimum order volume = 50 pieces*
[2] *Minimum order volume = 50 pieces*

5.2.2 Serial quad SPI NOR flash memory (N25Q256)

The on-board quad SPI NOR flash memory offers a reliable boot memory source with sufficient storage capacity to hold a moderate embedded Linux distribution. The Miami applies the Micron N25Q256 device, offering 32[MB]. This is a configuration option[3], which allows customization of the memory capacity to 16[MB], 64[MB] or 128[MB].

The Miami assigns the NOR flash to fixed processing system MIO pins, partially shared with the NAND flash interface. Therefore, these pins are not available for user functionality. The following table describes which pins are being used by the quad SPI controller and not to be used by the user.

SPI NOR flash signal name	FPGA pin	FPGA pin label
QSPI_DQ0	A21	PS_MIO2_500
QSPI_DQ1	F17	PS_MIO3_500
QSPI_DQ2	E19	PS_MIO4_500
QSPI_DQ3	A20	PS_MIO5_500
QSPI_SCK	A19	PS_MIO6_500
QSPI_CS	A22	PS_MIO1_500

5.2.3 SD-card memory interface

Optionally, the Miami SoMs can be booted from an SD-card, mounted on the carrier board if implemented. The pin location on the connector is fixed when it is required for booting. If not required, the SDIO interface may be routed via the programmable logic and connected to any valid I/O pad. Under these conditions, the MIO signals on the processing system can be used for other purposes.

The SDIO interface is operated at 1.8[V]. This may require the use of a level converter on the carrier board to properly interface with the SDIO controller. The following table addresses the involved signals for proper carrier board implementation and software control.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
SDIO_uSD_CLK	X1.48	E9	PS_MIO40_501
SDIO_uSD_CMD	X1.54	C15	PS_MIO41_501
SDIO_uSD_DQ0	X1.58	D15	PS_MIO42_501
SDIO_uSD_DQ1	X1.50	B12	PS_MIO43_501
SDIO_uSD_DQ2	X1.46	E10	PS_MIO44_501
SDIO_uSD_DQ3	X1.52	B14	PS_MIO45_501
SDIO_DETECT	X1.56	B16	PS_MIO24_501

5.2.4 EEPROM memory (CAT24C04)

The SoM provides a 4Kbit I²C connected CAT24C04 EEPROM device for storing parameters and other configuration and user settings. This device is connected to the Miami system I²C bus, accessible via the following MIO pins of the processor system. *Refer to the datasheet of the CAT24C04 regarding information how to use this device. Be aware that 16 highest address words of the 512 available words are reserved by the system for the serial number and administrative parameters. Do not overwrite this data.*

I2C bus signal name	FPGA pin	FPGA pin label
SYS_SCL	D13	PS_MIO52_500
SYS_SDA	C11	PS_MIO53_500

I²C address E²PROM memory	0xA0

[3] *Minimum order volume = 50 pieces*

5.3 Communication interfaces

5.3.1 Gigabit Ethernet

The Zynq processor contains 2 gigabit Ethernet controllers. These controllers are to be connected via the EMIO interface with the programmable logic and then routed to the I/O pads. Be aware that the use of common RMII Gigabit PHY devices requires an IP block in the FPGA converting the provided MII. This is because RMII via the EMIO is not supported by the Zynq. IP blocks covering this functionality are available via our web shop. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the high-end performance capabilities of the Gigabit Ethernet Controller (GEM) refer to Xilinx document UG585 (Zynq technical reference guide) chapter 16.*

5.3.2 USB 2.0 OTG

The Miami SoM supports one of the two integrated USB OTG controllers. These are only accessible via the MIO connected I/O pads, not the programmable logic. When the second USB controller is required, other MIO peripherals must be moved to other pin locations or functionally dropped. When USB is required, the USB control signals to the carrier board have to be connected using the designated signals on the connector and the corresponding signals on the Zynq device as described in the following table.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
USB_CLK	X1.83	A14	PS_MIO36_501
USB_DIR	X1.87	E15	PS_MIO29_501
USB_STP	X1.81	A12	PS_MIO30_501
USB_NXT	X1.85	F14	PS_MIO31_501
USB_DQ0	X1.89	C16	PS_MIO32_501
USB_DQ1	X1.79	G11	PS_MIO33_501
USB_DQ2	X1.75	B11	PS_MIO34_501
USB_DQ3	X1.67	F9	PS_MIO35_501
USB_DQ4	X1.73	A11	PS_MIO28_501
USB_DQ5	X1.69	B9	PS_MIO37_501
USB_DQ6	X1.77	F10	PS_MIO38_501
USB_DQ7	X1.71	C10	PS_MIO39_501
USB_RESET	X1.91	n.a.	Connected to the processor system using the PCA9536 I^2C I/O expander on address 0x82 on the Miami system I^2C bus. The signal can be accessed by addressing I/O pin IO[0].

5.3.3 SDIO

The Zynq processor contains 2 embedded SDIO controllers. The first controller can be used for booting the processor system. In this case it is bound to be connected to a particular set of MIO pins. When it is not required to boot from an SDIO connected SD-card image, both SDIO controllers can be accessed via the MIO processor pins or via the FPGA fabric. Be aware that the use of SDIO interface via FPGA fabric requires specific design constraints for proper operation. IP blocks covering this functionality are available via our webshop. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the usage of the SDIO controller refer to Xilinx document UG585 (Zynq technical reference guide) chapter 13.*

5.3.4 SATA

SATA-2 and SATA-3 compatible storage devices can be connected using the GTX transceivers on the Miami SoM. A total of 4 differential transceiver pairs are available on the carrier board connector, offering the ability to implement up to 4 SATA-3 devices. The GTX transceivers can support up to 6.125[Gbit/sec]. To make use of SATA on the Miami, an additional IP block must be purchased, e.g. via the Topic Embedded Products webshop, interfacing the transceivers with the processing system by means of a SATA media access controller (MAC) in FPGA fabric and a software driver for the applicable operating system e.g. Linux.

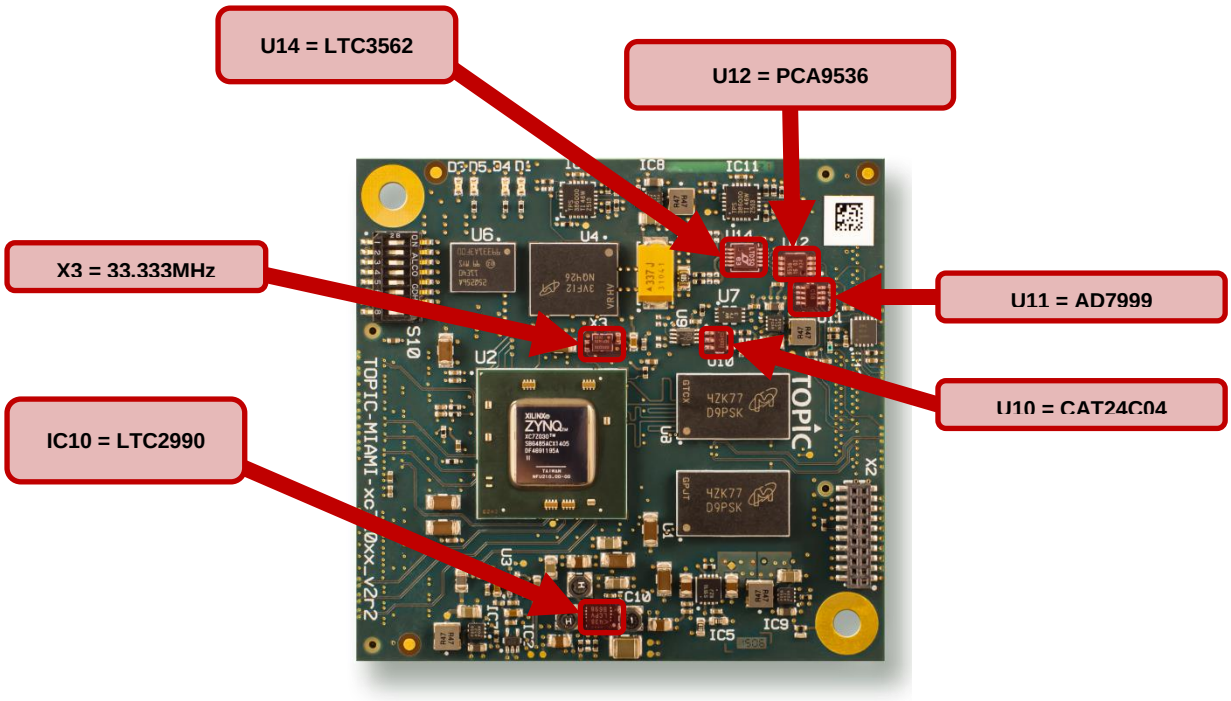
The SATA interface can be connected to any of the transceiver pairs. Keep in mind that you are required to provide a differential clock source for driving one or both of the GTX transceivers dedicated clock sources through the carrier board connector. It is not possible to provide a clock directly from within the FPGA fabric.

The following table gives an overview of the signals involved with the SATA interface.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
GTP_REF_CLK_0_P	X5.87	U9	MGTREFCLK0P_112
GTP_REF_CLK_0_N	X5.89	V9	MGTREFCLK0N_112
GTP_REF_CLK_1_P	X5.64	U5	MGTREFCLK1P_112
GTP_REF_CLK_1_N	X5.66	V5	MGTREFCLK1N_112
GTP_TX_0_P	X5.75	AA3	MGTPTXP0_112
GTP_TX_0_N	X5.77	AB3	MGTPTXN0_112
GTP_TX_1_P	X5.63	W4	MGTPTXP1_112
GTP_TX_1_N	X5.65	Y4	MGTPTXN1_112
GTP_TX_2_P	X5.81	AA5	MGTPTXP2_112
GTP_TX_2_N	X5.83	AB5	MGTPTXN2_112
GTP_TX_3_P	X5.69	W2	MGTPTXP3_112
GTP_TX_3_N	X5.71	Y2	MGTPTXN3_112
GTP_RX_0_P	X5.76	AA7	MGTPRXP0_112
GTP_RX_0_N	X5.78	AB7	MGTPRXN0_112
GTP_RX_1_P	X5.82	W8	MGTPRXP1_112
GTP_RX_1_N	X5.84	Y8	MGTPRXN1_112
GTP_RX_2_P	X5.88	AA9	MGTPRXP2_112
GTP_RX_2_N	X5.90	AB9	MGTPRXN2_112
GTP_RX_3_P	X5.70	W6	MGTPRXP3_112
GTP_RX_3_N	X5.72	Y6	MGTPRXN3_112

Important: *for AC coupling reasons, the transmitter lines are coupled with a 100[nF] bypass capacitor. You have to take care that the carrier board implements the bypass capacitor on the transmitter side of the return signal. The signals are routed differentially with a controlled impedance of 100[Ohm].*

5.4 Miscellaneous resources



5.4.1 Clocking resources

The Miami SoM integrates two clock sources: the first (33.3333[MHz]) is intended for the processor system, the second (98.304[MHz]) is available for the programmable logic. Based on the PS_CLOCK, the processing system generates the clocks to drive the CPU cores, DDR memory and the bus clock. This clock is also available for the user in the FPGA fabric. The PL_CLOCK is especially applicable for clocking the FPGA fabric. The chosen clock rate is a 3000 multiple of 32768Hz, which is the base frequency of many time synchronous applications.

Alternative clock sources can be connected via the SoM connector using the clock capable pins of the FPGA on bank 13, 34 or 35.

Clock signal name	FPGA pin	FPGA pin label	Description
PL_CLOCK	L5	IO_L12P_T1_MRCC_34	98.304 MHz, 20 ppm
PS_CLOCK	F16	PS_CLK_500	33.333 MHz, 20 ppm

5.4.2 I2C connected support peripherals

The Miami SoM implements two I²C chains via the MIO pads directly with the processing system. The following table gives an overview of the involved pins on the Zynq and the carrier board pins. The SYS I²C bus implements peripherals on the Miami SoM and may be used to connect system-level functionality on a carrier board, e.g. battery monitoring. The use of the SYS I²C bus is NOT recommended on the carrier board. The PS I²C bus is especially intended for user controlled chains on the carrier boards. However, the I²C controller is also accessible via the EMIO ports via the programmable logic pins. This allows the user to use the involved pins on the MIO for other purposes.

I2C bus signal name	SoM pin	FPGA pin	FPGA pin label
SYS_SCL	X1.51	D13	PS_MIO52_500
SYS_SDA	X1.53	C11	PS_MIO53_500
PS_SCL	X1.47	D10	PS_MIO50_500
PS_SDA	X1.49	C13	PS_MIO51_500

The SYS I²C has multiple connected peripherals to control and maintain consistent operation of the modules. The devices are available for the user, but care must be taken as certain configurations may harm reliable operation. The following table lists the peripherals integrated as well as the functionality they provide on the board.

I2C peripheral	I2C address	Description
LTC2990	0b1001100x = 0x98 0b1110111x = 0xEE (broadcast address)	AD converter for determining current consumption core power supply. The supply current is measured via a 5[mOhm] shunt resistor. - V1 = +1.0[V] PS supply (+) - V2 = +1.0[V] PS supply (-) - V3 = +1.0[V] PL supply (+) - V4 = +1.0[V] PL supply (-)
LTC3562	0b1100101x = 0xCA	Programmable power supplies for FPGA I/O banks 13, 34 and 35. - Bank 13 = Vcc00 = SW600B (600[mA] maximum) - Bank 35 = Vcc01 = SW600A (600[mA] maximum) - Bank 34 = Vcc02 = SW400B (400[mA] maximum)
CAT24C04	0b1010000x = 0xA0	General purpose EEPROM memory. Refer to the datasheet of the CAT24C04 for information how to access this device.
PCA9536	0b1000001x = 0x82	General purpose IO digital I/O expander (4 I/Os). - I/O 0 = USB_RESET = output = USB PHY reset signal - I/O 1 = VTT_SHDWN_N = output = disable DDR termination resistors power supply - I/O 2 = V_PRESENT = input = Carrier board JTAG chain presence detected - I/O 3 = DEBUG_PRESENT = input = debug expansion board detected.
AD7999	0b0101001x = 0x52	4 input A/D converter. - VDD = +3V3 - Vin0 = Vcc00 = programmable supply bank 13 - Vin1 = Vcc01 = programmable supply bank 35 - Vin2 = Vcc02 = programmable supply bank 34 - Vin3 = Vddr = power supply DDR memory

5.5 Power supplies

For powering the Miami SoM a single 3.3[V] power supply is sufficient. The maximum current of the module is depending on:

- Type of the module (Miami SoM XC7Z015 or Miami SoM XC7Z030)
- Operational frequency of the processor
- Load, execution profile and clock speed of the FPGA logic
- Type of I/O interfaces in use (especially the GTX transceivers consume much energy)

Power profile	Miami SoM XC7Z015	Miami SoM XC7Z030
Nominal power supply	3.3 [V] +/- 5%	3.3 [V] +/- 5%
Maximum current allowed	4.0 [A]	4.0 [A]

The Miami SoM can be powered from 2 sources:

- From the carrier board using the dual Samtec socket connectors
- From the debug expansion connector

It is not allowed to supply the Miami boards with power via both sources simultaneously as there are no protective measures in place to facilitate this on the Miami boards.

The power supply connections are provided on the following carrier board and debug expansion connectors:

Carrier board connector X1			
Signal name	**Connector pin**	**Direction**	**Description**
+3V3	X1.1	In	Supply input from carrier board (max. 4[A])
+3V3	X1.2	In	Supply input from carrier board (max. 4[A])
+3V3	X1.3	In	Supply input from carrier board (max. 4[A])
+3V3	X1.4	In	Supply input from carrier board (max. 4[A])
Vbat	X1.6	In	Battery backed-up supply from carrier board
+1V8	X1.57	Out	Logic supply for logic level matching PS I/O bank 500 and 501 (recommended max .100[mA])
+1V8	X1.59	Out	Logic supply for logic level matching PS I/O bank 500 and 501 (recommended max. 100[mA])
+1.25A	X1.84	Out	Analogue power supply for on-board XADC
Vcc00	X1.95	Out	Programmable (1.8V-3.3V) logic supply for logic level matching FPGA I/O bank 13 (recommended max.100[mA])
Vcc01	X1.97	Out	Programmable (1.8V-3.3V) logic supply for logic level matching FPGA I/O bank 34 (recommended max.100[mA])
Vcc02	X1.99	Out	Programmable (1.8V-3.3V) logic supply for logic level matching FPGA I/O bank 35 (recommended max.100[mA])
GND	X1.8	Ref	Supply ground reference
GND	X1.37	Ref	Supply ground reference
GND	X1.55	Ref	Supply ground reference
GND_XADC	X1.84	Ref	Ground reference for on-board XADC
GND	X1.93	Ref	Supply ground reference
GND_XADC	X1.101	Ref	Supply ground reference
GND	X1 ground strip	Ref	Ground reference for on-board XADC

Carrier board connector X5			
Signal name	**Connector pin**	**Direction**	**Description**
GND	X5.17	Ref	Supply ground reference
GND	X5.17	Ref	Supply ground reference
GND	X5.18	Ref	Supply ground reference
GND	X5.55	Ref	Supply ground reference
GND	X5.56	Ref	Supply ground reference
GND	X5.61	Ref	Supply ground reference for GTX transceivers
GND	X5.62	Ref	Supply ground reference for GTX transceivers
GND	X5.67	Ref	Supply ground reference for GTX transceivers
GND	X5.68	Ref	Supply ground reference for GTX transceivers
GND	X5.73	Ref	Supply ground reference for GTX transceivers
GND	X5.74	Ref	Supply ground reference for GTX transceivers
GND	X5.79	Ref	Supply ground reference for GTX transceivers
GND	X5.80	Ref	Supply ground reference for GTX transceivers
GND	X5.85	Ref	Supply ground reference for GTX transceivers
GND	X5.86	Ref	Supply ground reference for GTX transceivers
GND	X5.91	Ref	Supply ground reference for GTX transceivers
GND	X5.92	Ref	Supply ground reference for GTX transceivers
GND	X5 ground strip	Ref	Supply ground reference

Debug expansion board connector X2			
Signal name	**Connector pin**	**Direction**	**Description**
+3V3	X2.9	In	Supply input from expansion board (max. 2[A])
+3V3	X2.10	In	Supply input from expansion board (max. 2[A])
+3V3	X2.11	In	Supply input from expansion board (max. 2[A])
GND	X2.1	Ref	Supply ground reference
GND	X2.2	Ref	Supply ground reference
GND	X2.19	Ref	Supply ground reference
GND	X2.20	Ref	Supply ground reference

5.5.1 Battery backup supply

The FPGA facilitates a battery-backup supply pin for holding specific functions active during power-down of the device. By supplying this pin, the functionality behind this is guaranteed. *Refer to Xilinx user guide UG585 for more information on this functionality.*

5.5.2 I/O reference supplies

The used processor I/O banks (bank 500, 501, 13, 34 and 35) are powered with different supply voltages and interface with signals present on the carrier board connector. To facilitate proper level conversion or limited logic supply loading, the supply of each I/O bank is made available. It is recommended not to exceed 100mA loading per supply pin presented on the connector.

5.5.3 Analogue supply

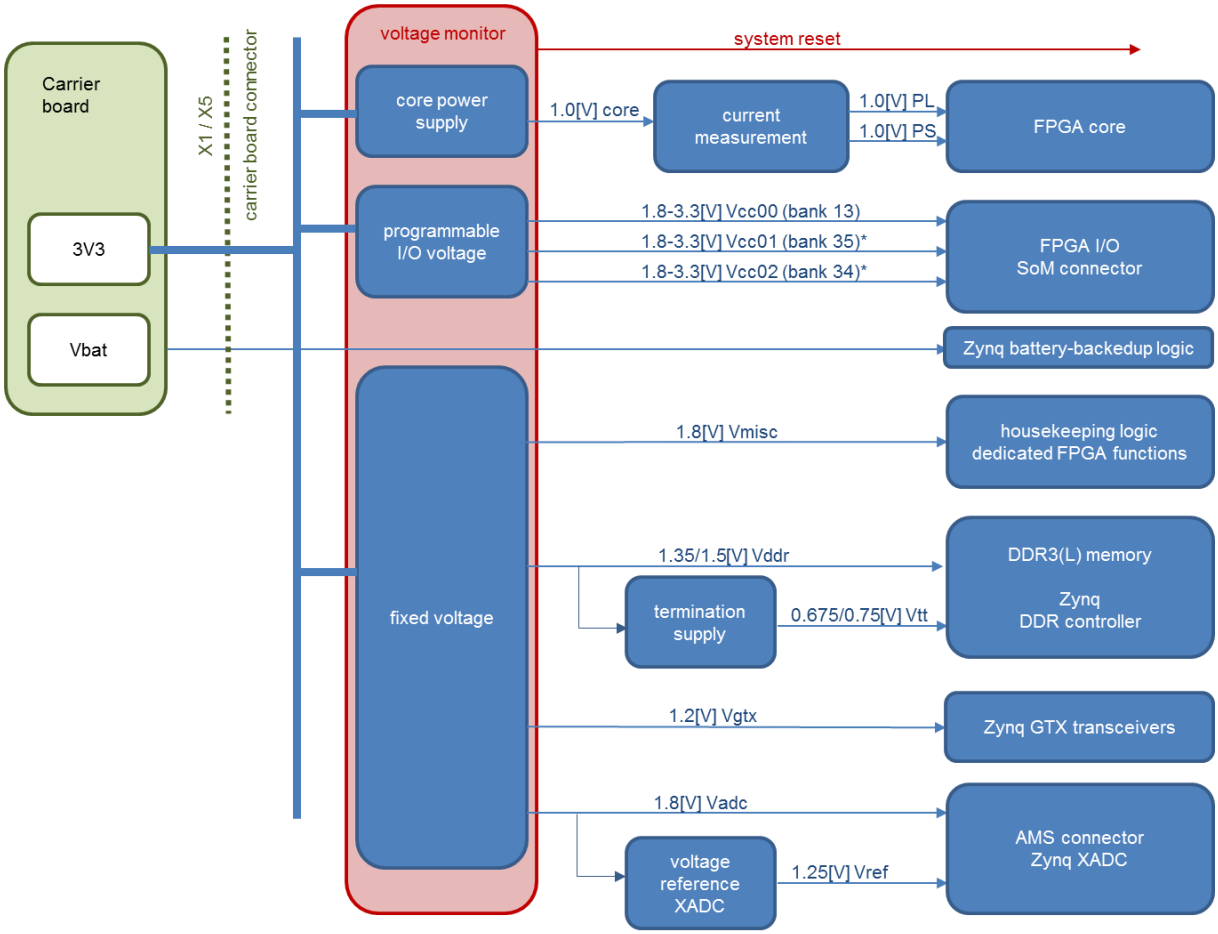
The analogue supply is provided as reference for the FPGA integrated XADC. It is not intended for supplying devices with relative high loads. Care must be taken to load this supply with as little as possible noise as it will influence the accuracy of the AD converter result.

5.5.4 Programmable logic supply (LTC3562)

The Miami provides a programmable logic supply. This supply can be programmed to match the logic voltage that is required of banks 13, 34 or 35. This supply can be programmed from 1.8V-3.3V in 25mV increments. It is recommended not to exceed 100mA loading per supply pin presented on the connector. *Refer to the datasheet of the LTC3562 regarding information how to use this device.*

Note: For the Miami 7030, VCCO1 & VCCO2 MUST not exceed 1V8. Since these are high performance banks and can only operate at 1V8.

5.5.5 Power distribution

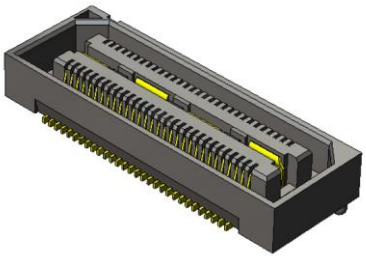


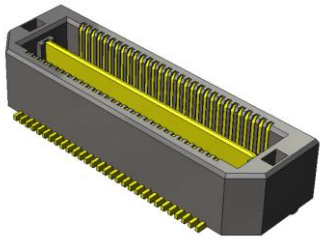
*Miami Zynq 7015 only

6 Connector pin assignments

6.1 X1: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm

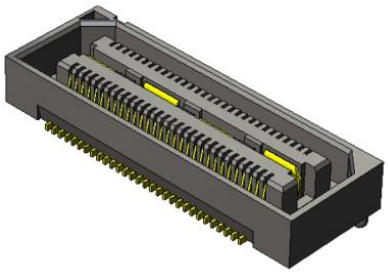


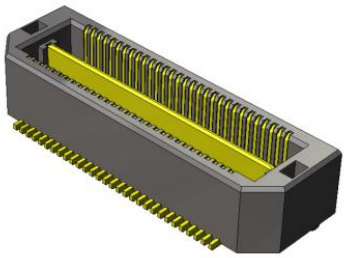


Pin	Signal	FPGA pin	Dir.	I/O level	Type		Type	I/O level	Dir.	FPGA pin	Signal	Pin
1	+3V3	-	In	+3V3	PWR		PWR	+3V3	In	-	+3V3	2
3	+3V3	-	In	+3V3	PWR		PWR	+3V3	In	-	+3V3	4
5	IO_L4N_T0_35	G7	I/O	+VCCO1	B35		PWR		In	-	Vbat	6
7	IO_L4P_T0_35	G8	I/O	+VCCO1	B35		PWR	0V	Ref	-	GND	8
9	IO_L6N_T0_VREF_35	F6	I/O	+VCCO1	B35		n.a.	+3V3	In	-	SOM_RST_N	10
11	IO_L1P_T0_AD0P_35	F7	I/O	+VCCO1	B35		B35	+VCCO1	I/O	E2	IO_L17P_T2_AD5P_35	12
13	IO_L1N_T0_AD0N_35	E7	I/O	+VCCO1	B35		B35	+VCCO1	I/O	D2	IO_L17N_T2_AD5N_35	14
15	IO_L2N_T0_AD8N_35	D6	I/O	+VCCO1	B35		B35	+VCCO1	I/O	D1	IO_L16P_T2_35	16
17	IO_L2P_T0_AD8P_35	D7	I/O	+VCCO1	B35		B35	+VCCO1	I/O	C1	IO_L16N_T2_35	18
19	IO_L10P_T1_AD11P_35	A5	I/O	+VCCO1	B35		B35	+VCCO1	I/O	D3	IO_L14P_T2_AD4P_SRCC_35	20
21	IO_L12N_T1_MRCC_35	C4	I/O	+VCCO1	B35		B35	+VCCO1	I/O	C3	IO_L14N_T2_AD4N_SRCC_35	22
23	IO_L8P_T1_AD10P_35	B7	I/O	+VCCO1	B35		B35	+VCCO1	I/O	B3	IO_L13N_T2_MRCC_35	24
25	IO_L6P_T0_35	G6	I/O	+VCCO1	B35		B35	+VCCO1	I/O	B4	IO_L13P_T2_MRCC_35	26
27	IO_L12P_T1_MRCC_35	D5	I/O	+VCCO1	B35		B35	+VCCO1	I/O	C5	IO_L11N_T1_SRCC_35	28
29	IO_L8N_T1_AD10N_35	B6	I/O	+VCCO1	B35		B35	+VCCO1	I/O	C6	IO_L11P_T1_SRCC_35	30
31	IO_L10N_T1_AD11N_35	A4	I/O	+VCCO1	B35		B35	+VCCO1	I/O	A6	IO_L9N_T1_DQS_AD3N_35	32
33	IO_L15P_T2_AD12P_35	A2	I/O	+VCCO1	B35		B35	+VCCO1	I/O	A7	IO_L9P_T1_DQS_AD3P_35	34
35	IO_L15N_T2_AD12N_35	A1	I/O	+VCCO1	B35		B35	+VCCO1	I/O	B8	IO_L7N_T1_AD2N_35	36
37	GND	-	Ref	0V	PWR		B35	+VCCO1	I/O	C8	IO_L7P_T1_AD2P_35	38
39	PS_JTAG_TDI	D11	I/O	+1V8	B501		B35	+VCCO1	I/O	D8	IO_L3N_T0_DQS_AD1N_35	40
41	PS_JTAG_TCK	D12	I/O	+1V8	B501		B35	+VCCO1	I/O	E8	IO_L3P_T0_DQS_AD1P_35	42
43	PS_JTAG_TDO	B13	I/O	+1V8	B501		n.a.	+3V3	-	-	V_PRESENT	44
45	PS_JTAG_TMS	C9	I/O	+1V8	B501		B501	+1V8	I/O	E10	SDIO_uSD_DQ2	46
47	PS_SCL	D10	I/O	+1V8	B501		B501	+1V8	I/O	E9	SDIO_uSD_CLK	48
49	PS_SDA	C13	I/O	+1V8	B501		B501	+1V8	I/O	B12	SDIO_uSD_DQ1	50
51	SCL_1V8	D13	I/O	+1V8	B501		B501	+1V8	I/O	B14	SDIO_uSD_DQ3	52
53	SDA_1V8	C11	I/O	+1V8	B501		B501	+1V8	I/O	C15	SDIO_uSD_CMD	54
55	GND	-	Ref	0V	PWR		B501	+1V8	I/O	B16	SDIO_DETECT	56
57	+1V8	-	Out	+1V8	PWR		B501	+1V8	I/O	D15	SDIO_uSD_DQ0	58
59	+1V8	-	Out	+1V8	PWR		B500	+1V8	I/O	E17	PS_MIO15_500	60
61	UART_TXD	D16	Out	+1V8	B501		B34	+VCCO2	I/O	J7	IO_L2P_T0_34	62
63	UART_RXD	A10	In	+1V8	B501		B34	+VCCO2	I/O	J6	IO_L2N_T0_34	64
65	SW_RST_N	-	In	+3V3	n.a.		B34	+VCCO2	I/O	K5	IO_L7N_T1_34	66
67	USB_DQ3	F9	I/O	+1V8	B501		B34	+VCCO2	I/O	L6	IO_L4P_T0_34	68
69	USB_DQ5	B9	I/O	+1V8	B501		B34	+VCCO2	I/O	P7	IO_L24P_T1_34	70
71	USB_DQ7	C10	I/O	+1V8	B501		B34	+VCCO2	I/O	P8	IO_L5N_T0_34	72
73	USB_DQ4	A11	I/O	+1V8	B501		B34	+VCCO2	I/O	L4	IO_L12N_T1_34	74
75	USB_DQ2	B11	I/O	+1V8	B501		B34	+VCCO2	I/O	N8	IO_L5P_T0_34	76
77	USB_DQ6	F10	I/O	+1V8	B501		B34	+VCCO2	I/O	J5	IO_L7P_T1_34	78
79	USB_DQ1	G11	I/O	+1V8	B501		B34	+VCCO2	I/O	R7	IO_L24N_T1_34	80
81	USB_STP	A12	I/O	+1V8	B501		B34	+VCCO2	I/O	M6	IO_L4N_T0_34	82
83	USB_CLK	A14	I/O	+1V8	B501		PWR	+1V25A	Out	-	+1V25A	84
85	USB_NXT	F14	I/O	+1V8	B501		PWR	0V	Ref	-	GND_XADC	86
87	USB_DIR	E15	I/O	+1V8	B501		B13	+VCCO0	I/O	V13	IO_L1P_T0_13	88
89	USB_DQ0	C16	I/O	+1V8	B501		B13	+VCCO0	I/O	U16	IO_25_13	90
91	USB_RESET	-	In	+3V3	n.a.		B13	+VCCO0	I/O	U18	IO_L22N_T3_13	92
93	GND	-	Ref	0V	PWR		B13	+VCCO0	I/O	V14	IO_L1N_T0_13	94
95	+VCCO0	-	Out	+VCCO0	PWR		B13	+VCCO0	I/O	U19	IO_L20P_T3_13	96
97	+VCCO1	-	Out	+VCCO1	PWR		B13	+VCCO0	I/O	V18	IO_L21P_T3_DQS_13	98
99	+VCCO2	-	Out	+VCCO2	PWR		B13	+VCCO0	I/O	V19	IO_L20N_T3_13	100
101	GND_XADC	-	Ref	0V	PWR		B13	+VCCO0	I/O	W18	IO_L21N_T3_DQS_13	102
103	XADC_VP	L12	In	+1V25A	B0		B13	+VCCO0	I/O	U17	IO_L22P_T3_13	104
105	XADC_VN	M11	In	+1V25A	B0		B13	+VCCO0	I/O	AB22	IO_L15N_T2_DQS_13	106
107	XADC_DXP	N12	In	+1V25A	B0		B13	+VCCO0	I/O	AB21	IO_L15P_T2_DQS_13	108
109	XADC_DXN	N11	In	+1V25A	B0		B13	+VCCO0	I/O	R17	IO_L19P_T3_13	110
111	PL_JTAG_RSTN	-	In	+3V3	B0		B13	+VCCO0	I/O	T17	IO_L19N_T3_VREF_13	112
113	PL_JTAG_TDI_F	H9	In	+3V3	B0		B13	+VCCO0	I/O	U12	IO_L5N_T0_13	114
115	PL_JTAG_TMS	H10	In	+3V3	B0		B13	+VCCO0	I/O	U11	IO_L5P_t0_13	116
117	PL_JTAG_TCK	H11	In	+3V3	B0		B13	+VCCO0	I/O	U14	IO_L6N_T0_VREF_13	118
119	PL_JTAG_TDO_F	G9	Out	+3V3	B0		B13	+VCCO0	I/O	U13	IO_L6P_T0_13	120

6.2 X5: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm





Pin	Signal	FPGA pin	Dir.	I/O level	Type		Type	I/O level	Dir.	FGPA pin	Signal	Pin
1	IO_L5N_T0_AD9N_35	E5	I/O	+VCCO1	B35		B35	+VCCO1	I/O	B2	IO_L18P_T2_AD13P_35	2
3	IO_L5P_T0_AD9P_35	F5	I/O	+VCCO1	B35		B35	+VCCO1	I/O	B1	IO_L18N_T2_AD13N_35	4
5	IO_L22P_T3_AD7P_35	G3	I/O	+VCCO1	B35		B35	+VCCO1	I/O	F2	IO_L23P_T3_35	6
7	IO_L22N_T3_AD7N_35	G2	I/O	+VCCO1	B35		B35	+VCCO1	I/O	F1	IO_L23N_T3_35	8
9	IO_L20N_T3_AD6N_35	F4	I/O	+VCCO1	B35		B35	+VCCO1	I/O	E4	IO_L21P_T3_AD14P_35	10
11	IO_L20P_T3_AD6P_35	G4	I/O	+VCCO1	B35		B35	+VCCO1	I/O	E3	IO_L21N_T3_AD14N_35	12
13	IO_L19P_T3_35	H4	I/O	+VCCO1	B35		B35	+VCCO1	I/O	G1	IO_L24N_T3_AD15N_35	14
15	IO_L19N_T3_VREF_35	H3	I/O	+VCCO1	B35		B35	+VCCO1	I/O	H1	IO_L24P_T3_AD15P_35	16
17	GND	-	Ref	0V	PWR		PWR	0V	Ref	-	GND	18
19	IO_L1P_T0_34	J8	I/O	+VCCO2	B34		B34	+VCCO2	I/O	M8	IO_L6P_T0_34	20
21	IO_L1N_T0_34	K8	I/O	+VCCO2	B34		B34	+VCCO2	I/O	M7	IO_L6N_T0_VREF_34	22
23	IO_L8P_T1_34	J2	I/O	+VCCO2	B34		B34	+VCCO2	I/O	K7	IO_L3P_T0_DQS_PUDC_B_34	24
25	IO_L8N_T1_34	J1	I/O	+VCCO2	B34		B34	+VCCO2	I/O	L7	IO_L3N_T0_DQS_34	26
27	IO_L11P_T1_SRCC_34	K4	I/O	+VCCO2	B34		B34	+VCCO2	I/O	J3	IO_L9P_T1_DQS_34	28
29	IO_L11N_T1_SRCC_34	K3	I/O	+VCCO2	B34		B34	+VCCO2	I/O	K2	IO_L9N_T1_DQS_34	30
31	IO_L10P_T1_34	L2	I/O	+VCCO2	B34		B34	+VCCO2	I/O	M4	IO_L22P_T3_34	32
33	IO_L10N_T1_34	L1	I/O	+VCCO2	B34		B34	+VCCO2	I/O	M3	IO_L22N_T3_34	34
35	IO_L21P_T3_DQS_34	N4	I/O	+VCCO2	B34		B34	+VCCO2	I/O	N1	IO_L16P_T2_34	36
37	IO_L21N_T3_DQS_34	N3	I/O	+VCCO2	B34		B34	+VCCO2	I/O	P1	IO_L16N_T2_34	38
39	IO_L15P_T1_34	M2	I/O	+VCCO2	B34		B34	+VCCO2	I/O	P3	IO_L18P_T2_34	40
41	IO_L15N_T1_34	M1	I/O	+VCCO2	B34		B34	+VCCO2	I/O	P2	IO_L18N_T2_34	42
43	IO_L17P_T2_34	R3	I/O	+VCCO2	B34		B34	+VCCO2	I/O	T2	IO_L13P_T2_MRCC_34	44
45	IO_L17N_T2_34	R2	I/O	+VCCO2	B34		B34	+VCCO2	I/O	T1	IO_L13N_T2_MRCC_34	46
47	IO_L19P_T3_34	N6	I/O	+VCCO2	B34		B34	+VCCO2	I/O	R5	IO_L23P_T3_34	48
49	IO_L19N_T3_VREF_34	N5	I/O	+VCCO2	B34		B34	+VCCO2	I/O	R4	IO_L23N_T3_34	50
51	IO_L20P_T3_34	P6	I/O	+VCCO2	B34		B34	+VCCO2	I/O	U2	IO_L14P_T2_SRCC_34	52
53	IO_L20N_T3_34	P5	I/O	+VCCO2	B34		B34	+VCCO2	I/O	U1	IO_L14N_T2_SRCC_34	54
55	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	56
57	IO_L8P_T1_13	AA12	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AA11	IO_L7P_T1_13	58
59	IO_L8N_T1_13	AB12	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB11	IO_L7N_T1_13	60
61	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	62
63	GTP_TX_1_P	W4	Out	+1V2	B112		B112	+1V2	In	U5	GTP_REF_CLK_1_P	64
65	GTP_TX_1_N	Y4	Out	+1V2	B112		B112	+1V2	In	V5	GTP_REF_CLK_1_N	66
67	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	68
69	GTP_TX_3_P	W2	Out	+1V2	B112		B112	+1V2	In	W6	GTP_RX_3_P	70
71	GTP_TX_3_N	Y2	Out	+1V2	B112		B112	+1V2	In	Y6	GTP_RX_3_N	72
73	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	74
75	GTP_TX_0_P	AA3	Out	+1V2	B112		B112	+1V2	In	AA7	GTP_RX_0_P	76
77	GTP_TX_0_N	AB3	Out	+1V2	B112		B112	+1V2	In	AB7	GTP_RX_0_N	78
79	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	80
81	GTP_TX_2_P	AA5	Out	+1V2	B112		B112	+1V2	In	W8	GTP_RX_1_P	82
83	GTP_TX_2_N	AB5	Out	+1V2	B112		B112	+1V2	In	Y8	GTP_RX_1_N	84
85	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	86
87	GTP_REF_CLK_0_P	U9	In	+1V2	B112		B112	+1V2	In	AA9	GTP_RX_2_P	88
89	GTP_REF_CLK_0_N	V9	In	+1V2	B112		B112	+1V2	In	AB9	GTP_RX_2_N	90
91	GND	-	Ref	V0	PWR		PWR	V0	Ref	-	GND	92
93	IO_L10P_T1_13	Y12	I/O	+VCCO0	B13		B13	+VCCO0	I/O	V11	IO_L4P_T0_13	94
95	IO_L10N_T1_13	Y13	I/O	+VCCO0	B13		B13	+VCCO0	I/O	W11	IO_L4N_T0_13	96
97	IO_L11P_T1_SRCC_13	AA14	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB13	IO_L9P_T1_DQS_13	98
99	IO_L11N_T1_SRCC_13	AA15	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB14	IO_L9N_T1_DQS_13	100
101	IO_L12P_T1_MRCC_13	Y14	I/O	+VCCO0	B13		B13	+VCCO0	I/O	W12	IO_L3P_T0_DQS_13	102
103	IO_L12N_T1_MRCC_13	Y15	I/O	+VCCO0	B13		B13	+VCCO0	I/O	W13	IO_L3N_T0_DQS_13	104
105	IO_L23P_T3_13	V16	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB16	IO_L17P_T2_13	106
107	IO_L23N_T3_13	W16	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB17	IO_L17N_T2_13	108
109	IO_L14P_T2_SRCC_13	AA16	I/O	+VCCO0	B13		B13	+VCCO0	I/O	V15	IO_L2P_T0_13	110
111	IO_L14N_T2_SRCC_13	AA17	I/O	+VCCO0	B13		B13	+VCCO0	I/O	W15	IO_L2N_T0_13	112
113	IO_L18P_T2_13	AA19	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB18	IO_L16P_T2_13	114
115	IO_L18N_T2_13	AA20	I/O	+VCCO0	B13		B13	+VCCO0	I/O	AB19	IO_L16N_T2_13	116
117	IO_L13P_T2_MRCC_13	Y18	I/O	+VCCO0	B13		B13	+VCCO0	I/O	W17	IO_L24P_T3_13	118
119	IO_L13N_T2_MRCC_13	Y19	I/O	+VCCO0	B13		B13	+VCCO0	I/O	Y17	IO_L24N_T3_13	120

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

7 Electrical characteristics

7.1 Electrical specifications

Supply voltage	3.3 [V], +/-5%
Current consumption	1.5 [A] typically (XC7Z012S/XC7Z015) , 2.0 [A] typically (XC7Z030)

7.2 Environment specifications

Extended operating temperature	-40 … +85[°C]
Storage temperature	-40 … +85[°C]
Relative humidity	0 … 95%, non-condensing

7.3 Mechanical specifications

Weight	approximately 20 [gram]
Board	glass epoxy FR-4, UL-listed, 12 layers, 1.6 [mm]
Dimensions	68.4 [mm] x 65.0 [mm] x 10.0 [mm] (length x width x height)

7.4 Regulatory conformation

CE (EMC, EMI)	Report available on request
Temperature and humidity	Report available on request
RoHS	All applied components, printed circuit board material, production of the printed circuit board as well as the assembly of the boards are conducted in compliance with the RoHS legislation.

8 Revision history

Date	Revision	Description of Revision
25-Jun-2017	V2R2 – Rev. A	• Added AD7999 VDD level • Changed available RAM in FPGA fabric, GTP speed and PCIe speed. • Added boot switch settings for cascaded / independed mode • Added paragraph; resetting the Miami SOM • Added description of the mechanical 3D file • Added default UART baud rate • Added exception for voltage level on VCCO1 and VCCO2 in case of a ZYNQ 7030
8-Apr-2021	V2R2 – Rev. B	• Removed NAND flash references • Removed memory vault references