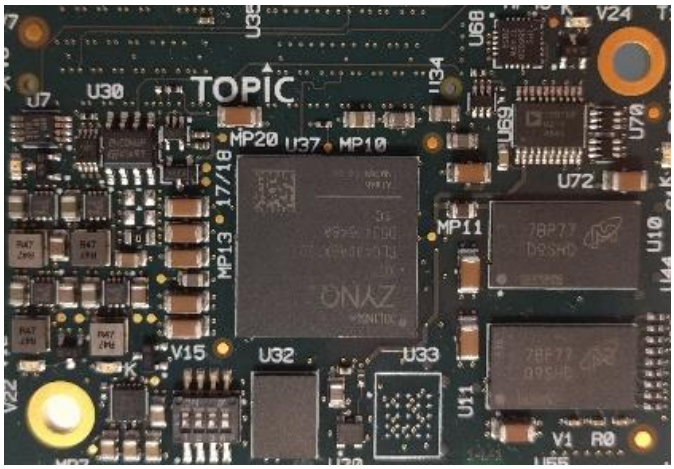
MIAMI-ZYNQ LITE (7007/7010/7014/7020)

Product Guide

V2R0 / 2/3/21



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1 Introduction

The Miami Zynq LITE System-on-Module (SOM) processor module is a 68.4x40.0mm sized CPU board based on the Xilinx Zynq XC7Z010, XC7Z020, XC7Z007 and XC7Z004 processors. The 7010 and 7020 include a dual-core ARM Cortex A9 processor integrated with FPGA fabric, adding programmable logic and high-performance computing capabilities to the processor platform. The 7007 and 7014 versions incorporate just a single core processor.

The XC7Z007/010/014/020 SOCs are based on Artix FPGA technology, providing flexible I/O technology and DSP capabilities with over 150GMAC fixed-point operations per second for the largest device.

The processor cores run up to 666MHz and include a variety of functions required for multimedia, medical or industrial applications. These include encryption, encoding, accelerators, display interface, camera interfacing, LVDS interfaces, audio interfaces and general purpose inputs and outputs.

When placing a production order of 50 units or more, the modules can be ordered with different sizes of flash memory, DDR-SDRAM and several configuration options. The SoM provides support for several standard interfaces, such as Ethernet, USB 2.0 OTG, SDIO, etc.

All interfaces are accessible using a 120 pins high-performance Samtec mezzanine connector. Other connectors are not foreseen.

Typical power consumption of the whole board is only a few Watts, maximum 5W for the largest devices with maximum loading. Passive and active cooling precautions can be put in place to support thermal conduction measures suitable for the target application.

The Miami Zynq Lite is intended for cost-sensitive application, requiring FPGA fabric to resolve board complexity, real-time performance issues or high-performance processing requirements.

2 Installation

The Miami System-on-Modules are delivered with a pre-installed Linux distribution, executed from the NOR flash memory. Powering a mounted Miami Lite on a custom carrier board or a Florida evaluation board will automatically boot the Miami board from the NOR flash and gives you a command prompt on the console terminal port .

2.1 Software installation

The Miami SoM comes with a Linux distribution, which can be downloaded from GitHub:

https://github.com/topic-embedded-products/topic-platform

This is an easy starting point for developing your own applications. When accessing this website, you are guided through the steps to download, install and start using the software. The Linux distribution contains:

- Linux configuration and development tools
- Cross compiler for the Zynq/Cortex-A9 processor
- BSP with drivers for all peripherals on the Miami SoMs (including the PCAP to program the FPGA)
- Simple example program for getting started

The Miami SoMs are not dependent on versions of Vivado tooling. However, example FPGA images are available for Vivado 2018.2 and higher.

For any help or support, please contact us at support@TopicProducts.com.

3 Miami SoM features

Miami Som	7010	7020	7007S	7014S
FPGA Technology				
7 Series PL Equivalent	Artix®-7	Artix®-7	Artix®-7	Artix®-7
Logic Cells	28K	85K	23K	65K
LUTs	17,600	53,200	14,400	40,600
FlipFlops	35,200	106,400	28,800	81,200
RAM	2.1Mb	4.9Mb	1.8Mb	3.8Mb
DSP slices	80	220	66	170
Processor Units				
CPU architecture	ARMCortex-A9 MPCore (Dual-Core)		ARM® Cortex™-A9 MPCore™ (Single core)	
External Memory Support	DDR3 L			
On-chip Memory	256KB			
L1 Cache	32kb Instruction, 32 KB Data per processor			
L2 Cache	512kb			
SDRAM	DDR3/DDR3L @ 533MHz, 1GB			
NOR	64 MB Quad SPI			
EEPROM	4 Kb I^2C storage			
DMA Channels	8 (4 dedicated to PL)			
Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
Peripherals w/ built-in DMA(2)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO			
User programmable/configurable Interfaces				
Analog	Up to 14 channels differential, 12 bits			
Serial	UART, 12C, SPI, 12 S, User defined			
Video	LVDS, TFT, VGA, LCD			
USB	USB OTG 2.0			
CAN	Up to 2x CAN			
Debug	Debug UART, console			
Miscellaneous	GPIOs / SD/SDIO 2.0/MMC 3.31 compliant controllers			
Dedicated interfaces on SoM connectors				
Network	10/100/1000Mbps Ethernet, IEEE1558 support			
USB	USB OTG 2.0			
JTAG	PL JTAG Chain for carrier board programming			
Power Supply				
Input	3.3V via connector On-board voltage regulation			
Output	Configurable I/O standards and voltages			
Control	Current measurement for PL and PS			
Software				
Bootloader/BSP	U-Boot			
Boot options	JTAG, NOR, (external) SD-card			
Operating System	Topic Linux 4.x distribution via GitHub (META-TOPIC)			
Dyplo® compatible platform	Yes			
Mechanical and environmental				
Dimensions	65mm x 45mm			
Connectors	1x 120 pin Samtec high performance mezzanine carrier board connectors			
Temperature	Industrial graded, IEC 60068-2-38 2009			
Humidity	0%-95%, non-condensing, IEC 60068-2-38-2009			
EMC	EN 55032			
EMI	IEC 61132, EN 61326, IEC 55024			

[1)] *Other configurations possible at higher volumes.*

4 Miami LITE Zynq SoM architecture

The Miami LITE Zynq System-on-Module integrates all peripherals to bring up a full functional processing system. The system connects to the carrier board using a high performance connector. The following paragraphs give an overview of peripherals and devices which determine the functionality of the board.

4.1 Miami LITE Zynq SoM board layout

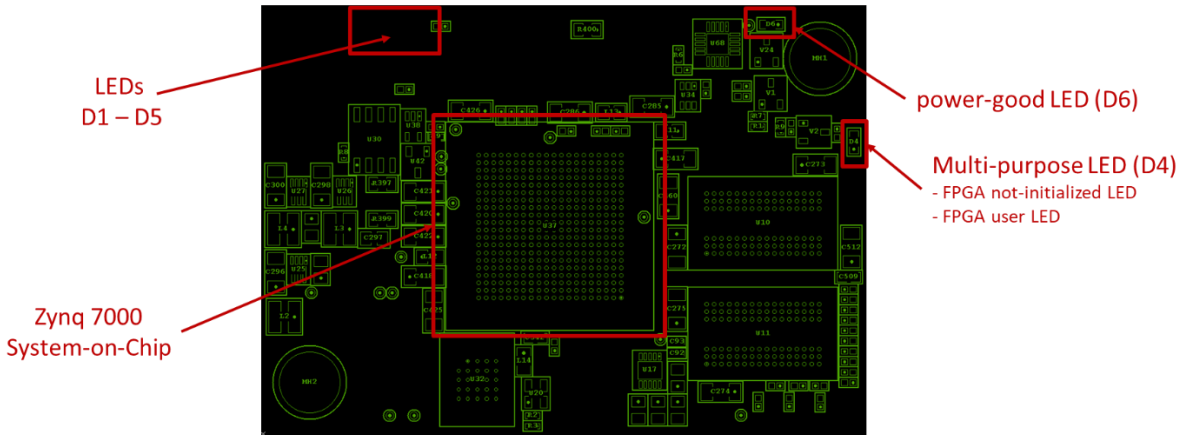


Figure 4.1: Miami Zynq Lite board top view

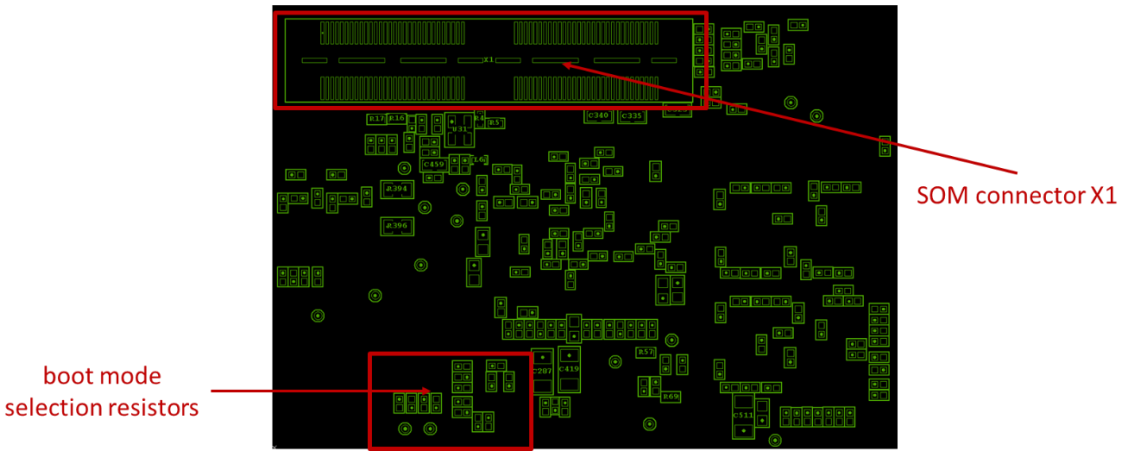


Figure 4.2: Miami Zynq Lite board bottom view

4.2 Block diagram

The block diagram in Figure 4.2 illustrates the general functionality of the board, divided by FPGA and processor bound functionality. It is clear that the processor connected functionality is more dedicated than the free-programmable functionality of the FPGA fabric.

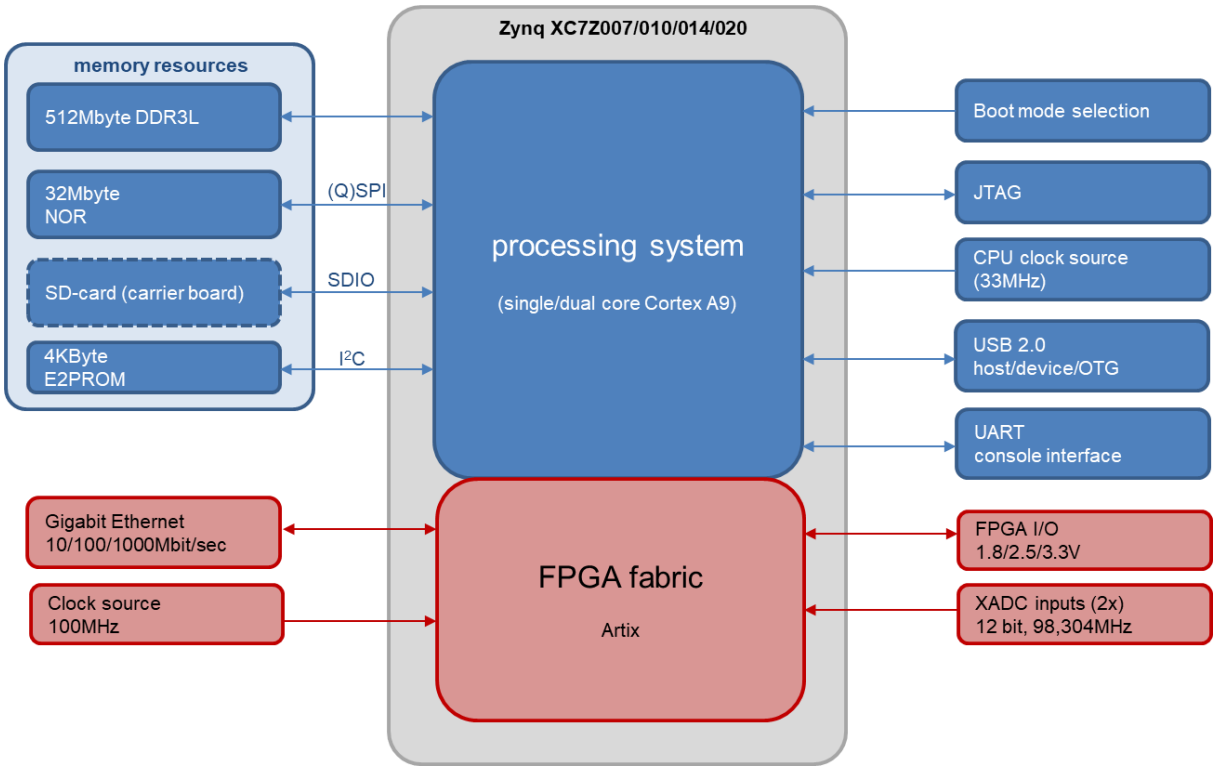


Figure 4.2: Block diagram of the Miami Zynq Lite SOM

4.3 Mechanical description

The Miami should be fitted on a carrier board using two mating connectors:

Part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm

The exact relative placement details of the connectors, the guide holes for the connectors and the fixation standoff holes are described in the following figure. The exact measurement details can be downloaded from the support website as a DXF object to match the Miami SoM exactly on your carrier board layout placement plan.

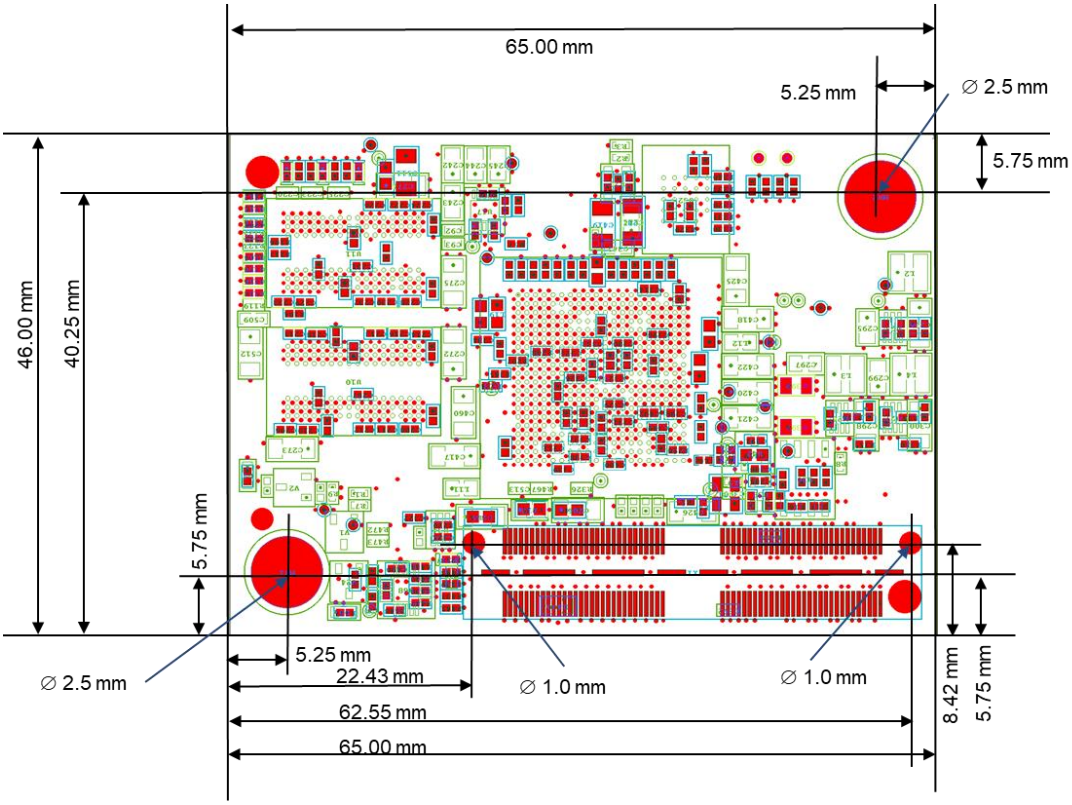


Figure 4.3:Mechanical dimensions Miami Zynq Lite

Special attention must be given for mounting and removing the SOM from the carrier board. Samtec recommends lifting the connectors in a straight vertical movement. This requires specific tooling which is not standard available. Alternatively, careful alternating twisting with small force in the length direction removes the module from the carrier board. Due to the limited mating cycles of the connectors, this should be performed as little as possible. A maximum of 200 mating cycles is specified by Samtec.

5 Miami SoM board functionality

The functionality of the SoM module can be divided in different function groups:

- Configuration and debug interfaces
- Memory resources
- Communication interfaces
- Miscellaneous functionality
- Power supplies and system integrity

In the following paragraphs the functions will be explained from a user perspective to help understand the context to use and program the functionality.

5.1 Configuration and debug interfaces

In figure 5.1 the configuration and debug interfaces of the Miami Zynq Lite are illustrated. The figure illustrates clearly that most signals required for this are accessible via the SOM connector and have to be disclosed via the carrier board. All Topic Florida carrier boards allow access to these interfaces.

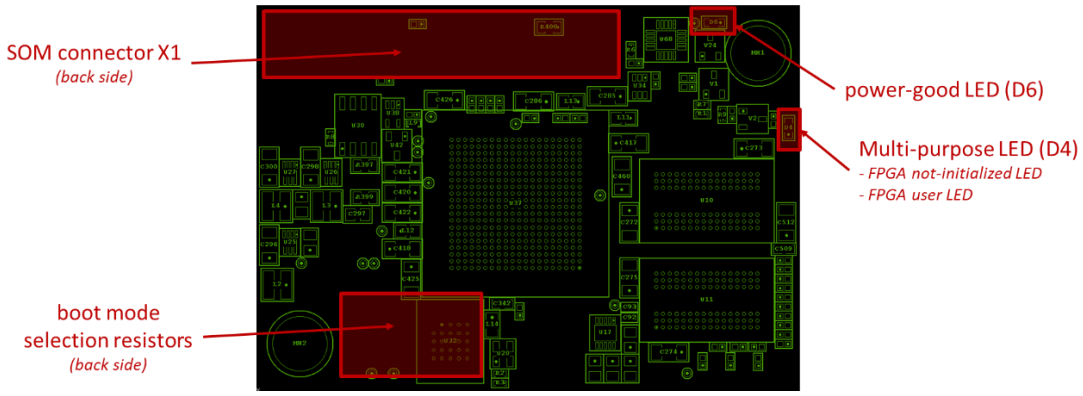


Figure 5.1: Configuration and debug interfaces

5.1.1 Status LEDs

There are 2 status LEDs provided on the SOM board. These are indicating the operational status of the board from a system and user perspective.

LED reference	FPGA pin	Description
D6	B5 (PS-MIO9-500)	Power good/kernel alive indication - Power-good LED. When active, the primary power supplies on the board are up and within operational limits. When the Miami board is powered at 3.3[V] this must be the case. - By default, the Power-Good LED is active. It is possible to use MIO pin 9 to turn off the LED. By default, the Topic Linux distribution toggles this signal at a 2 seconds rate to implement a software heartbeat.
D4	J15 (IO-25-35)	FPGA image not ready/FPGA user LED - Directly after power-up and when active, the FPGA part of the Zynq is not loaded yet. When programmed with a valid bit stream, the LED will be off. - During normal operation, the FPGA user LED functionality is attached to this led. By default this LED will be off. However, the LED is available for the user to give it a different function, like a heart beat.

5.1.2 Boot mode selection resistors

From the different boot modes supported by the Zynq 7000 series devices, only the JTAG, QSPI NOR flash and SD-card boot modes are supported. The recommended boot methodology is using to initiate the booting of the device from the QSPI NOR flash and, depending on the application, continue booting from the SD-card. This is the most reliable boot methodology. Remind that the SD-card interface is exposed on the SOM connector and must be implemented on the carrier board.

The boot mode selection is realized using pin strapping of the QSPI flash memory control lines using 20K resistors. For the Miami Zynq Lite, it was decided to boot by default from NOR flash. To be able to boot directly from the SD-card, a resistor swap needs to be soldered. This is a production option for the Miami Zynq Lite.

Resistor settings	Boot mode	Comment
R343 = 20K, R339 = not assembled	QSPI NOR flash	Default configuration
R343 = not assembled, R339 = 20K	SD-Card flash	User configurable, production option
other combinations	Invalid, undefined behavior	-

Refer to Xilinx document UG585 (Zynq technical reference guide) chapter 6 for more details on booting strategies.

5.1.3 JTAG interfaces

The Zynq processor of Xilinx has a JTAG port connected to the dedicated JTAG pins on the Zynq. It is using 1.8[V] signal levels. The applicable pull-up resistors are integrated on the Miami board. Using the PL-JTAG port you can:

- Program the FPGA fabric
- Use the ChipScope logic analyzer to debug the programmed FPGA logic
- Boundary scan for production verification
- Debug the processor software using the ARM CoreSight Debug Access Port (DAP)

PL_JTAG signals	FPGA pin	Description
TDI	G6 (TDI_O)	Dedicated package pin
TDO	F6 (TDO_O)	Dedicated package pin
TCK	F9 (TCK_O)	Dedicated package pin
TMS	J6 (TMS_O)	Dedicated package pin

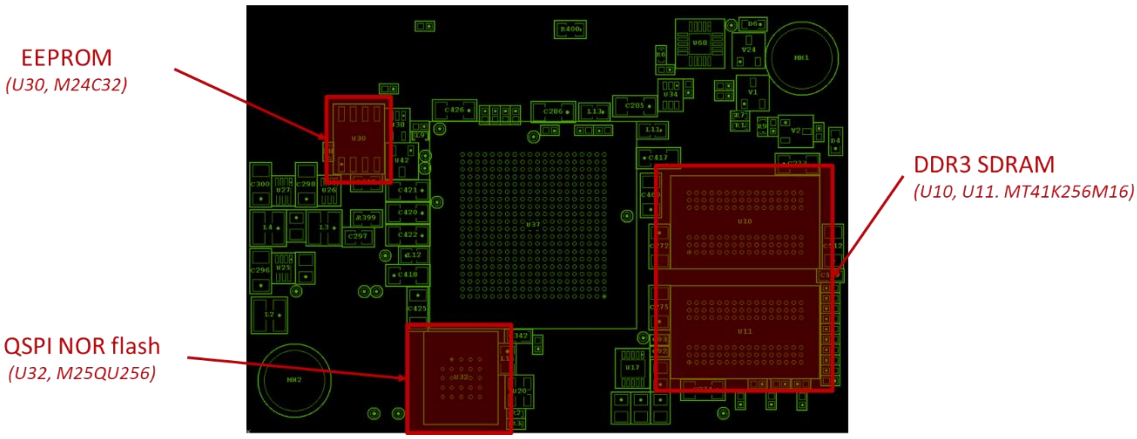
The JTAG ports can be accessed from the carrier board using the SOM connector X1.

5.1.4 Console interfaces

A primary software development interface is the console connection with the processing system. The Miami provides a fixed console connection directly on the MIO port of the processing system. The console signals are available on the carrier board connector X1. The signals are provided 1.8[V] CMOS logic levels compatible.

Console signal	Connector pin	FPGA pin	Description
UART_RXD	X1.B3	C5	Serial data from processor to other device. Can be used for other functionality if needed.
UART_TXD	X1.B1	C8	Serial data from other device to processor. Can be used for other functionality if needed.

5.2 Memory resources



5.2.1 DDR3 SDRAM memory (MT41K256M16)

A low-power DDR3 SDRAM memory solution is provided as the main system memory. The RAM memory has a 32-bit interface and can be clocked up to 533 [MHz]. The DDR clock frequency is configured by the software configuration using PLL1 clock output 2, which the standard DDR clock output. The SDRAM memory size can be ordered[1] in sizes of 256[MB], 512[MB] and 1[GB] (default).

The solution is build using two 16-bit wide DDR3 memory chips (Micron MT41K256M16). The devices are connected to the dedicated DDR memory controller interface on the Zynq. They can be supplied by a 1.5[V] (default) or a 1.35[V] supply. The supply level is a hard-configuration option[2] of the module. As the module is intended as a low-cost solution, by default 512Mbyte using 1 DDR memory device is implemented. Other configurations are production options.

5.2.2 Serial quad SPI NOR flash memory (M25QU256)

The on-board quad SPI NOR flash memory offers a reliable boot memory source with sufficient storage capacity to hold a moderate embedded Linux distribution. The Miami applies the Micron M25QU256 device, offering 32[MB]. This is a configuration option[3], which allows customization of the memory capacity to 16[MB], 64[MB] or 128[MB].

The Miami assigns the NOR flash to fixed processing system MIO pins, partially shared with the NAND flash interface. Therefore, these pins are not available for user functionality. The following table describes which pins are being used by the quad SPI controller and not to be used by the user.

SPI NOR flash signal name	FPGA pin	FPGA pin label
QSPI_DQ0	B8	PS_MIO2_500
QSPI_DQ1	D6	PS_MIO3_500
QSPI_DQ2	B7	PS_MIO4_500
QSPI_DQ3	A6	PS_MIO5_500
QSPI_SCK	A5	PS_MIO6_500
QSPI_CS	A7	PS_MIO1_500

[1] *Minimum order volume = 50 pieces*
[2] *Minimum order volume = 50 pieces*
[3] *Minimum order volume = 50 pieces*

5.2.3 SD-card memory interface

Optionally, the Miami SoMs can be booted from an SD-card, mounted on the carrier board if implemented. The pin location on the connector is fixed when it is required for booting. If not required, the SDIO interface may be routed via the programmable logic and connected to any valid I/O pad. Under these conditions, the MIO signals on the processing system can be used for other purposes.

The SDIO interface is operated at 1.8[V]. This may require the use of a level converter on the carrier board to properly interface with the SDIO controller. The following table addresses the involved signals for proper carrier board implementation and software control.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
SDIO_uSD_CLK	X1.48	E9	PS_MIO40_501
SDIO_uSD_CMD	X1.54	C15	PS_MIO41_501
SDIO_uSD_DQ0	X1.58	D15	PS_MIO42_501
SDIO_uSD_DQ1	X1.50	B12	PS_MIO43_501
SDIO_uSD_DQ2	X1.46	E10	PS_MIO44_501
SDIO_uSD_DQ3	X1.52	B14	PS_MIO45_501
SDIO_DETECT	X1.56	B16	PS_MIO24_501

5.2.4 EEPROM memory (M24C04-RMN6TP)

The SoM provides a 4Kbit I^2C connected M24C04 EEPROM device for storing parameters and other configuration and user settings. This device is connected to the Miami system I^2C bus, accessible via the following MIO pins of the processor system. *Refer to the datasheet of the M24C04-RMN6TP regarding information how to use this device. Be aware that 16 highest address words of the 512 available words are reserved by the system for the serial number and administrative parameters. Do not overwrite this data.*

I2C bus signal name	FPGA pin	FPGA pin label
SYS_SCL	D13	PS_MIO52_500
SYS_SDA	C11	PS_MIO53_500

I^2C address E^2PROM memory	0xA0

5.3 Communication interfaces

5.3.1 Gigabit Ethernet

The Zynq processor contains 2 Gigabit Ethernet controllers. These controllers are to be connected either directly via the MIO I/O pins or via the EMIO interface with the programmable logic and then routed to the I/O pads. Be aware that the use of common RMII Gigabit PHY devices requires an IP block in the FPGA converting the provided MII. This is because RMII via the EMIO is not supported by the Zynq. IP blocks covering this functionality are available via our web shop. *For more information on this subject, contact support@TopicProducts.com. Regarding the high-end performance capabilities of the Gigabit Ethernet Controller (GEC) refer to Xilinx document UG585 (Zynq technical reference guide) chapter 16.*

5.3.2 USB 2.0 OTG

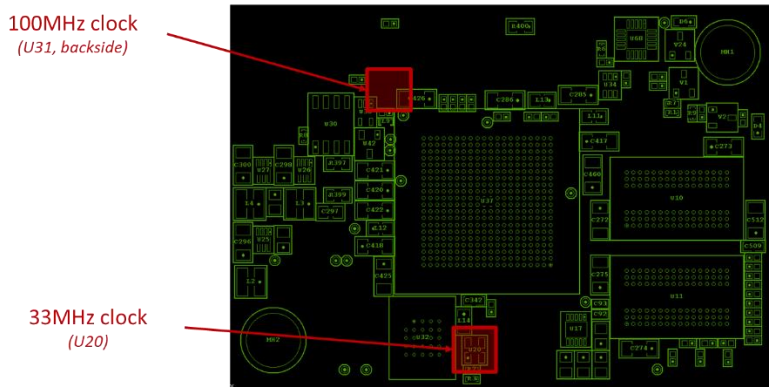
The Miami SoM supports one of the two integrated USB OTG controllers. These are only accessible via the MIO connected I/O pads, not the programmable logic. When the second USB controller is required, other MIO peripherals must be moved to other pin locations or functionally dropped. When USB is required, the USB control signals to the carrier board have to be connected using the designated signals on the connector and the corresponding signals on the Zynq device as described in the following table.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
USB_CLK	X1.83	A14	PS_MIO36_501
USB_DIR	X1.87	E15	PS_MIO29_501
USB_STP	X1.81	A12	PS_MIO30_501
USB_NXT	X1.85	F14	PS_MIO31_501
USB_DQ0	X1.89	C16	PS_MIO32_501
USB_DQ1	X1.79	G11	PS_MIO33_501
USB_DQ2	X1.75	B11	PS_MIO34_501
USB_DQ3	X1.67	F9	PS_MIO35_501
USB_DQ4	X1.73	A11	PS_MIO28_501
USB_DQ5	X1.69	B9	PS_MIO37_501
USB_DQ6	X1.77	F10	PS_MIO38_501
USB_DQ7	X1.71	C10	PS_MIO39_501
USB_RESET	X1.91	n.a.	Connected to the processor system using the PCA9536 I^2C I/O expander on address 0x82 on the Miami system I^2C bus. The signal can be accessed by addressing I/O pin IO[0].

5.3.3 SDIO

The Zynq processor contains 2 embedded SDIO controllers. The first controller can be used for booting the processor system. In this case it is bound to be connected to a particular set of MIO pins. When it is not required to boot from an SDIO connected SD-card image, both SDIO controllers can be accessed via the MIO processor pins or via the FPGA fabric. Be aware that the use of SDIO interface via FPGA fabric requires specific design constraints for proper operation. IP blocks covering this functionality are available via our webshop. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the usage of the SDIO controller refer to Xilinx document UG585 (Zynq technical reference guide) chapter 13.*

5.4 Miscellaneous resources



5.4.1 Clocking resources

The Miami SoM integrates two clock sources: the first (33.3333[MHz]) is intended for the processor system, the second (98.304[MHz]) is available for the programmable logic. Based on the PS_CLOCK, the processing system generates the clocks to drive the CPU cores, DDR memory and the bus clock. This clock is also available for the user in the FPGA fabric. The PL_CLOCK is especially applicable for clocking the FPGA fabric. The chosen clock rate is a 100MHz. Using the internal MMCM PLLs, other frequencies can be synthesized.

Alternative clock sources can be connected via the SoM connector using the clock capable pins of the FPGA on bank 13, 34 or 35.

Clock signal name	FPGA pin	FPGA pin label	Description
PL_CLOCK	L5	IO_L12P_T1_MRCC_34	100 MHz, 20 ppm
PS_CLOCK	F16	PS_CLK_500	33.333 MHz, 20 ppm

5.4.2 I2C connected support peripherals

The Miami SoM implements two I²C chains via the MIO pads directly with the processing system. The following table gives an overview of the involved pins on the Zynq and the carrier board pins. The SYS I²C bus implements peripherals on the Miami SoM and may be used to connect system-level functionality on a carrier board, e.g. battery monitoring. The use of the SYS I²C bus is NOT recommended on the carrier board. The PS I²C bus is especially intended for user controlled chains on the carrier boards. However, the I²C controller is also accessible via the EMIO ports via the programmable logic pins. This allows the user to use the involved pins on the MIO for other purposes.

I2C bus signal name	SoM pin	FPGA pin	FPGA pin label
SYS_SCL	X1.51	D13	PS_MIO52_500
SYS_SDA	X1.53	C11	PS_MIO53_500
PS_SCL	X1.47	D10	PS_MIO50_500
PS_SDA	X1.49	C13	PS_MIO51_500

The SYS I²C has multiple connected peripherals to control and maintain consistent operation of the modules. The devices are available for the user, but care must be taken as certain configurations may harm reliable operation. The following table lists the peripherals integrated as well as the functionality they provide on the board.

I2C peripheral	I2C address	Description
CAT24C04	0b1010000x = 0xA0	General purpose EEPROM memory. Refer to the datasheet of the M24C04 for information how to access this device.

5.5 Power supplies

For powering the Miami LITE SoM a single 3.3[V] power supply is sufficient. The maximum current of the module is depending on:

- Type of the module (Miami SoM XC7Z007S, 014S, 010 or 020)
- Operational frequency of the processor
- Load, execution profile and clock speed of the FPGA logic
- Type of I/O interfaces in use

Power profile	Miami SoM
Nominal power supply	3.3 [V] +/- 5%
Absolute maximum current allowed	4.8 [A]
Absolute maximum power rating	15 [W]

The power supply connections are provided on the following carrier board and debug expansion connectors:

Carrier board connector X1			
Signal name	**Connector pin**	**Direction**	**Description**
+3V3	X1.A1	In	Supply input from carrier board
+3V3	X1.A2	In	Supply input from carrier board
+3V3	X1.A3	In	Supply input from carrier board
+3V3	X1.A4	In	Supply input from carrier board
Vbat	X1.A6	In	Battery backed-up supply from carrier board
+1V8	X1.A57	Out	Logic supply for logic level matching PS I/O bank 500 and 501 (recommended max .100[mA])
+1V8	X1.A59	Out	Logic supply for logic level matching PS I/O bank 500 and 501 (recommended max. 100[mA])
+1.25A	X1.B24	Out	Analogue power supply for on-board XADC
Vcc00	X1.B35	Out	Selectable (1.8V-3.3V) logic supply for logic level matching FPGA I/O bank 34 (recommended max.100[mA])
Vcc01	X1.B37	Out	Selectable (1.8V-3.3V) logic supply for logic level matching FPGA I/O bank 35 (recommended max.100[mA])
GND	X1.A8	Ref	Supply ground reference
GND	X1.A37	Ref	Supply ground reference
GND	X1.A55	Ref	Supply ground reference
GND_XADC	X1.A24	Ref	Ground reference for on-board XADC
GND	X1.A33	Ref	Supply ground reference
GND_XADC	X1.A41	Ref	Supply ground reference
GND	X1 ground strip	Ref	Ground reference for on-board XADC

5.5.1 Battery backup supply

The FPGA facilitates a battery-backup supply pin for holding specific functions active during power-down of the device. By supplying this pin, the functionality behind this is guaranteed. *Refer to Xilinx user guide UG585 for more information on this functionality.*

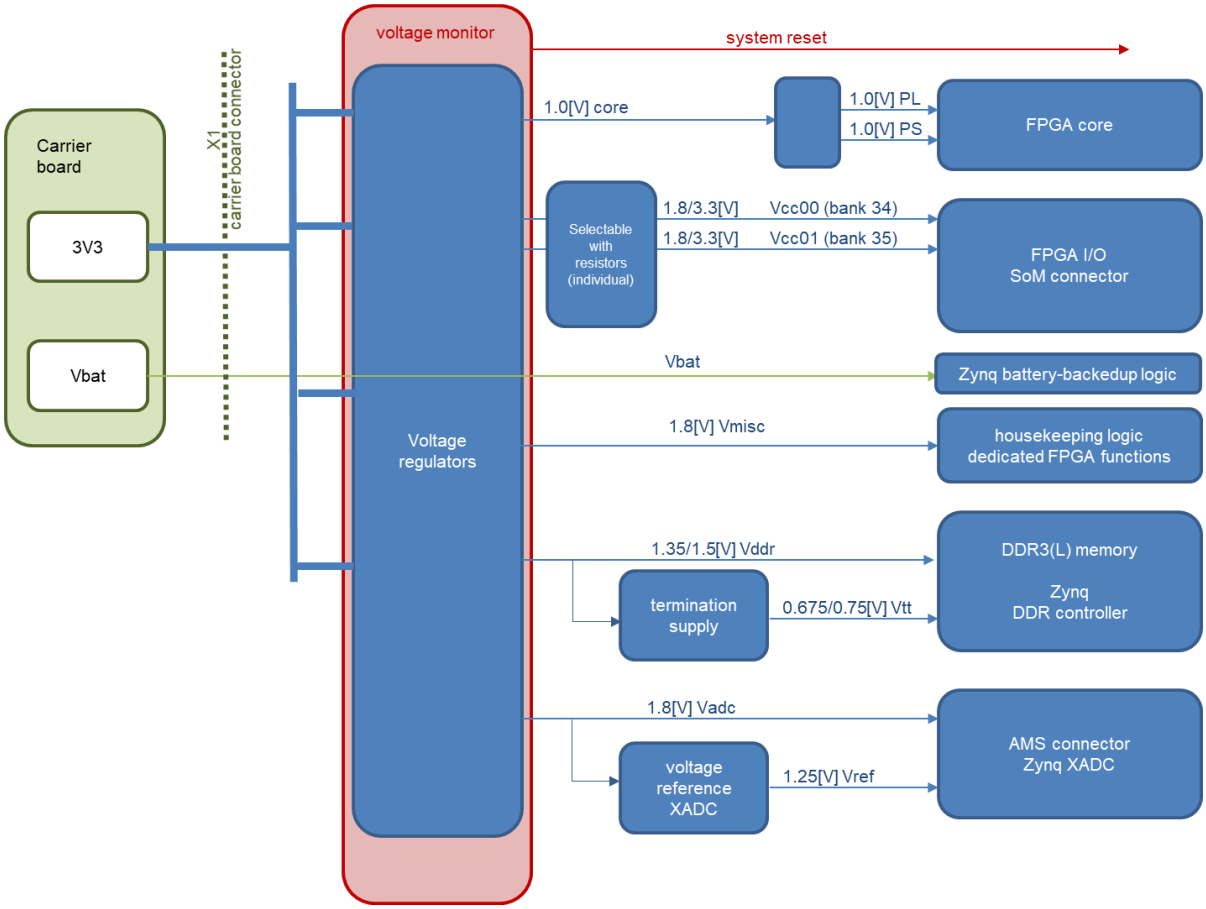
5.5.2 I/O reference supplies

The used processor I/O banks (bank 500, 501, 34 and 35) are powered with different supply voltages and interface with signals present on the carrier board connector. To facilitate proper level conversion or limited logic supply loading, the supply of each I/O bank is made available. It is recommended not to exceed 100mA loading per supply pin presented on the connector.

5.5.3 Analogue supply

The analogue supply is provided as reference for the FPGA integrated XADC. It is not intended for supplying devices with relative high loads. Care must be taken to load this supply with as little as possible noise as it will influence the accuracy of the AD converter result.

5.5.4 Power distribution

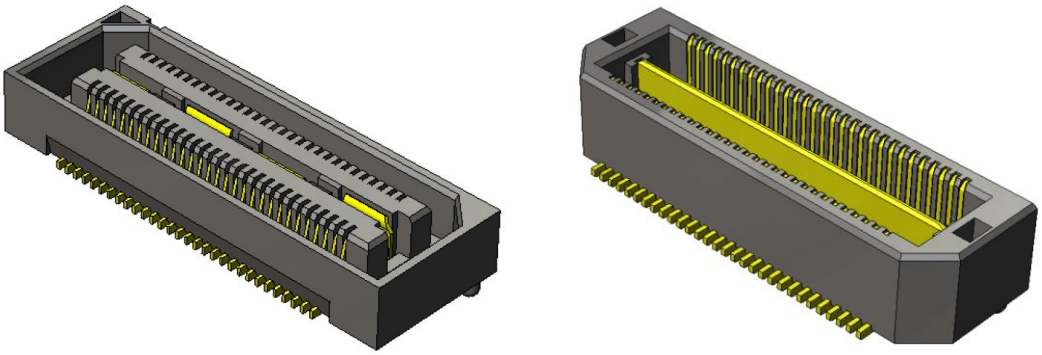


6 Connector pin assignments

There is 1 carrier board connector available on the Miami Zynq LITE SoM. The Samtec high-speed mezzanine connector is used for carrier board interfacing. All signal I/Os are exchanged via this connector, including power supplies and debugging resources.

6.1 X1: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm



Remark: Ground reference is available on the integrated ground bar as reference to any pin on the connector

SOM INTERFACE		MIAMI-LITE			
SoM pin	SoM pin	BOARD SIGNAL NAME	FPGA PIN	REMARKS	MIO PIN
X1.001	X1.A01	+3V3			
X1.002	X1.A02	+3V3			
X1.003	X1.A03	+3V3			
X1.004	X1.A04	+3V3			
X1.005	X1.A05	IO_D_AD_VCC1_21_N	G20		
X1.006	X1.A06	Vbat			
X1.007	X1.A07	IO_D_AD_VCC1_21_P	G19		
X1.008	X1.A08	GND			
X1.009	X1.A09	IO_D_VCC1_22_N	G18		
X1.010	X1.A10	SOM_RST_N			
X1.011	X1.A11	IO_D_VCC1_22_P	G17		
X1.012	X1.A12	IO_D_AD_VCC1_0_P	C20	LED_GREEN	
X1.013	X1.A13	IO_D_CC_VCC1_23_N	H17		
X1.014	X1.A14	IO_D_AD_VCC1_0_N	B20	LED_RED	
X1.015	X1.A15	IO_D_CC_VCC1_23_P	H16		
X1.016	X1.A16	IO_D_VCC1_16_P	D19		
X1.017	X1.A17	IO_D_AD_VCC1_11_N	M20		
X1.018	X1.A18	IO_D_VCC1_16_N	D20		
X1.019	X1.A19	IO_D_AD_VCC1_11_P	M19		
X1.020	X1.A20	IO_D_AD_CC_VCC1_1_P	J18		
X1.021	X1.A21	IO_D_AD_VCC1_12_N	M18		
X1.022	X1.A22	IO_D_AD_CC_VCC1_1_N	H18		
X1.023	X1.A23	IO_D_AD_VCC1_12_P	M17		
X1.024	X1.A24	IO_D_CC_VCC1_17_N	L17		
X1.025	X1.A25	IO_D_AD_VCC1_13_N	L20		
X1.026	X1.A26	IO_D_CC_VCC1_17_P	L16		
X1.027	X1.A27	IO_D_AD_VCC1_13_P	L19		
X1.028	X1.A28	IO_D_CC_VCC1_18_N	K18		
X1.029	X1.A29	IO_D_AD_VCC1_14_N	J19		
X1.030	X1.A30	IO_D_CC_VCC1_18_P	K17		
X1.031	X1.A31	IO_D_AD_VCC1_14_P	K19		
X1.032	X1.A32	IO_D_AD_VCC1_2_N	A20		
X1.033	X1.A33	IO_D_AD_VCC1_15_P	F19		
X1.034	X1.A34	IO_D_AD_VCC1_2_P	B19	LED_BLUE	
X1.035	X1.A35	IO_D_AD_VCC1_15_N	F20		
X1.036	X1.A36	IO_D_AD_VCC1_3_N	D18		
X1.037	X1.A37	GND			
X1.038	X1.A38	IO_D_AD_VCC1_3_P	E17		
X1.039	X1.A39				
X1.040	X1.A40	IO_D_AD_VCC1_4_N	E19		
X1.041	X1.A41	IO_S_VCC4_1	C10	USB_HUB_RESET	MIO52
X1.042	X1.A42	IO_D_AD_VCC1_4_P	E18		
X1.043	X1.A43				
X1.044	X1.A44	V_PRESENT			
X1.045	X1.A45	IO_S_VCC4_3	C11	GENERIC_SWITCH	MIO53
X1.046	X1.A46	IO_S_VCC4_4	F13	SDIO_uSD_DQ2	MIO44
X1.047	X1.A47	IO_S_VCC4_5	B13		MIO50
X1.048	X1.A48	IO_S_VCC4_6	D14	SDIO_uSD_CLK	MIO40
X1.049	X1.A49	IO_S_VCC4_7	B9		MIO51
X1.050	X1.A50	IO_S_VCC4_8	A9	SDIO_uSD_DQ1	MIO43
X1.051	X1.A51	SCL_1V8	B12	SCL	MIO48
X1.052	X1.A52	IO_S_VCC4_9	B15	SDIO_uSD_DQ3	MIO45
X1.053	X1.A53	SDA_1V8	C12	SDA	MIO49
X1.054	X1.A54	IO_S_VCC4_10	C17	SDIO_uSD_CMD	MIO41
X1.055	X1.A55	GND			
X1.056	X1.A56	IO_S_VCC4_11	B14	SDIO_DETECT	MIO47
X1.057	X1.A57	+1V8			
X1.058	X1.A58	IO_S_VCC4_12	E12	SDIO_uSD_DQ0	MIO42
X1.059	X1.A59	+1V8			
X1.060	X1.A60	IO_S_VCC4_13	D16		MIO46

SOM INTERFACE		MIAMI-LITE			
SoM pin	SoM pin	BOARD SIGNAL NAME	FPGA PIN	REMARKS	MIO PIN
X1.061	X1.B01	IO_S_VCC4_14	C8	UART1_RXD_TO_USB_UART	MIO15
X1.062	X1.B02	IO_D_VCC2_18_P	H15		
X1.063	X1.B03	IO_S_VCC4_15	C5	UART1_TXD_FROM_USB_UART	MIO14
X1.064	X1.B04	IO_D_VCC2_18_N	G15		
X1.065	X1.B05	SW_RST_N			
X1.066	X1.B06	IO_D_AD_VCC2_19_P	K14		
X1.067	X1.B07	IO_S_VCC4_16	F12	USB_DQ3	MIO35
X1.068	X1.B08	IO_D_AD_VCC2_19_N	J14		
X1.069	X1.B09	IO_S_VCC4_17	A10	USB_DQ5	MIO37
X1.070	X1.B10	IO_D_AD_VCC2_20_P	N15		
X1.071	X1.B11	IO_S_VCC4_18	C18	USB_DQ7	MIO39
X1.072	X1.B12	IO_D_AD_VCC2_20_N	N16		
X1.073	X1.B13	IO_S_VCC4_19	C16	USB_DQ4	MIO28
X1.074	X1.B14	IO_D_AD_VCC2_21_P	L14		
X1.075	X1.B15	IO_S_VCC4_20	A12	USB_DQ2	MIO34
X1.076	X1.B16	IO_D_AD_VCC2_21_N	L15		
X1.077	X1.B17	IO_S_VCC4_21	E13	USB_DQ6	MIO38
X1.078	X1.B18	IO_D_VCC2_22_P	M14		
X1.079	X1.B19	IO_S_VCC4_22	D15	USB_DQ1	MIO33
X1.080	X1.B20	IO_D_VCC2_22_N	M15		
X1.081	X1.B21	IO_S_VCC4_23	C15	USB_STP	MIO30
X1.082	X1.B22	IO_S_VCC2_0	G14		
X1.083	X1.B23	IO_S_VCC4_24	A11	USB_CLK	MIO36
X1.084	X1.B24	+1.25A			
X1.085	X1.B25	IO_S_VCC4_25	E16	USB_NXT	MIO31
X1.086	X1.B26	GND_XADC			
X1.087	X1.B27	IO_S_VCC4_26	C13	USB_DIR	MIO29
X1.088	X1.B28	IO_S_VCC0_0	R19	ETH_TX_EN	
X1.089	X1.B29	IO_S_VCC4_27	A14	USB_DQ0	MIO32
X1.090	X1.B30	IO_D_VCC0_16_P	T11	ETH_RESET_N	
X1.091	X1.B31	USB_RESET			
X1.092	X1.B32	IO_D_VCC0_16_N	T10	ETH_INT_N	
X1.093	X1.B33	GND			
X1.094	X1.B34	IO_D_VCC0_17_P	T12	ETH_MDIO	
X1.095	X1.B35	VCCO0			
X1.096	X1.B36	IO_D_VCC0_17_N	U12	ETH_MDC	
X1.097	X1.B37	VCCO1			
X1.098	X1.B38	IO_D_CC_VCC0_18_P	N18	ETH_RX_CLK	
X1.099	X1.B39	VCCO2			
X1.100	X1.B40	IO_D_CC_VCC0_18_N	P19	ETH_RX_EN	
X1.101	X1.B41	GND_XADC			
X1.102	X1.B42	IO_D_VCC0_19_P	V12	ETH_RX_D0	
X1.103	X1.B43	XADC_VP	K9		
X1.104	X1.B44	IO_D_VCC0_19_N	W13	ETH_RX_D1	
X1.105	X1.B45	XADC_VN	L10		
X1.106	X1.B46	IO_D_VCC0_20_N	T15	ETH_RX_D2	
X1.107	X1.B47	XADC_DXP	M9		
X1.108	X1.B48	IO_D_VCC0_20_P	T14	ETH_RX_D3	
X1.109	X1.B49	XADC_DXN	M10		
X1.110	X1.B50	IO_D_VCC0_21_P	P14	ETH_CLK125	
X1.111	X1.B51	PL_JTAG_RSTN			
X1.112	X1.B52	IO_D_VCC0_21_N	R14	ETH_TX_CLK	
X1.113	X1.B53	PL_JTAG_TDI	G6		
X1.114	X1.B54	IO_D_VCC0_22_N	Y17	ETH_TX_D3	
X1.115	X1.B55	PL_JTAG_TMS	J6		
X1.116	X1.B56	IO_D_VCC0_22_P	Y16	ETH_TX_D2	
X1.117	X1.B57	PL_JTAG_TCK	F9		
X1.118	X1.B58	IO_D_VCC0_23_N	Y14	ETH_TX_D1	
X1.119	X1.B59	PL_JTAG_TDO	F6		
X1.120	X1.B60	IO_D_VCC0_23_P	W14	ETH_TX_D0	

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7 Electrical characteristics

7.1 Electrical specifications

Supply voltage	3.3 [V], +/-5%
Current consumption	1.5 [A] typically (XC7Z010) , 1.75 [A] typically (XC7Z020)

7.2 Environment specifications

Extended operating temperature	-40 … +85[°C]
Storage temperature	-40 … +85[°C]
Relative humidity	0 … 95%, non-condensing

7.3 Mechanical specifications

Weight	approximately 15 [gram]
Board	glass epoxy FR-4, UL-listed, 12 layers, 1.6 [mm]
Dimensions	68.4 [mm] x 40.0 [mm] x 10.0 [mm] (length x width x height)

7.4 Regulatory conformation

CE (EMC, EMI)	Tested according to EN 55032 and EN 55035. Report available on request
Temperature and humidity	Tested according to EN 60068. Report available on request.
Shock and vibration	Tested according to EN 60068. Report available on request.
RoHS / REACH	All applied components, printed circuit board material, production of the printed circuit board as well as the assembly of the boards are conducted in compliance with the RoHS and REACH legislation. A declaration of compliance is available on request.