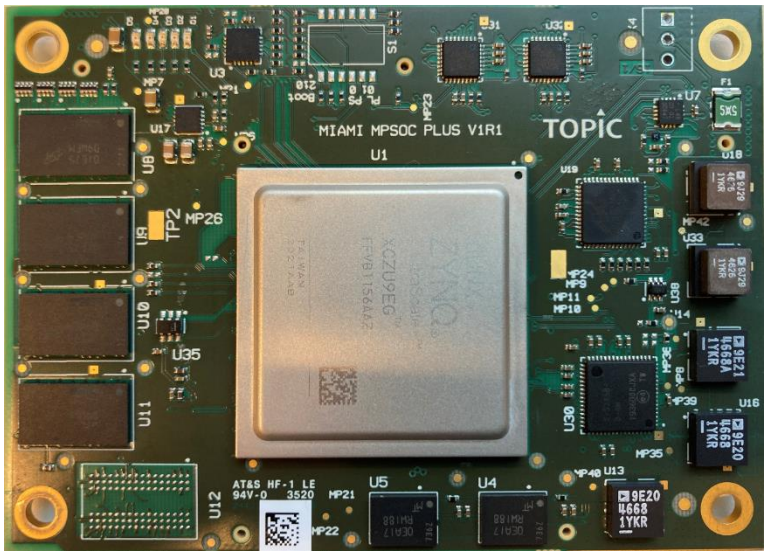
MIAMI MPSOC Plus SOM
(XCZU6 / XCZU9 / XCZU15)

Product Guide

V1R8 / 21-Mar-2021



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[5] Miami MPSOC Plus SOM schematic (Topic download website)
[6] Xilinx UG1085
[7] Topic Github: https://github.com/topic-embedded-products/meta-topic
[8] Topic downloads website: http://downloads.topic.nl
[9] Topic support: support@topicproducts.com

Abbreviations

Abbreviation	Description
BSP	Board Support Package
DFU	Device Upgrade Protocol
EMIO	Extended Multiplexed Input /Output
FPGA	Field Programmable Gate Array
I/O	Input / Output
MIO	Multiplexed Input /Output
MPSOC	Multi-Processor System On Chip
PS	Processor System
PL	Programmable Logic
SDK	Software Development Kit
SOM	System On Module
TLD	Topic Linux Distribution
TDK	Topic Development Kit

1 Introduction

The Miami MPSOC Plus System-on-Module (SOM) is a 95.0mmx68.5mm sized CPU board based on the Xilinx Zynq Ultrascale+ XCZU6, XCZU9 or XCZU15 System-on-Chip (SOC). Zynq MPSoC devices, depending on their configuration, can carry a quad core ARM Cortex A53 processor, a dual core ARM Cortex-R5, a GPU with an ARM Mali 400MP and large amount of Ultrascale+ FPGA fabric. This adds a significant amount of programmable logic and high-performance computing capabilities to the processor platform to implement even deep-learning capabilities to the edge. The Ultrascale+ FPGA provides flexible I/O technology, DSP capabilities and lots of on-chip RAM, using the UltraRAM blocks.

The processor cores can run up to 1.5GHz (speed grade 2 and above) and include a variety of functions required for multimedia, medical and industrial applications. These include data encryption, video encoding, processing accelerators, as well as display-, camera-, LVDS- and audio interfaces. But also general purpose inputs and outputs needed for system level integration.

When placing a production order, the modules can be assembled with different sizes of flash memory, DDR memory and several other configuration options. The Miami SOM can support for a wide range of physical interfaces such as Ethernet, USB 3.0 host/peripheral, USB 2.0 OTG, SDIO, PCI-Express and HDMI/DisplayPort. Remind that the physical interfaces and connectors have to be realized on the carrier board.

All interfaces are accessible through two 120-pin and one 180-pin high-performance Samtec mezzanine connectors. These connectors include power supply, CPU and FPGA I/O, along with signals for debugging, programming and configuration.

The maximum power consumption of the board is rated at 50 W for all the Miami MPSOC Plus versions. Passive and active cooling precautions can be put in place to support thermal conduction measures suitable for the target application.

2 Installation

The Miami MPSOC Plus SOMs are delivered with a pre-installed, limited functionality Linux distribution, executed from the NOR flash memory. Mounting the SOM on a carrier board and providing power to it, enables a console available via UART, USB or Ethernet with a command line prompt. By default, the pre-installed image does not require a password to login and gives you root privileges.

2.1 Hardware installation

2.1.1 Heatsink assembly

The Miami MPSOC Plus SOM is a high-performance computing platform, dissipating typically 15 W of heat and maximally 50 W. An applicable heatsink is dependent on the ambient conditions and enclosure of the target application. Dissipation is dominated by the utilization and clock frequency of the FPGA fabric. Please refer to chapter 9 for suggested heatsink solutions. If the Miami MPSOC Plus is ordered in an evaluation/development configuration, it comes with a standard heatsink solution for office ambient conditions. Also refer to chapter 9 for instructions on the installation of the heatsink on the board, the connection of the fan and the usage conditions. This chapter also reflects to other dissipation related aspects to be respected when integrating in your enclosure.

Although the Zynq Ultrascale+ devices are thermally protected when the junction temperature exceeds a threshold and performs a reset, it is highly recommended not to operate without a heatsink attached to the device.

2.1.2 Carrier board assembly

The Miami MPSOC plus module connects to a carrier board using 3 Samtec connectors (2x QSH-060-01-L-D-A and QSH-090-01-L-D-A) and 4 standoffs (5mm, M2.5, brass, female-female, e.g. Wuerth Electronics). The connectors can mate in one direction only. The required force to insert the SOM on the carrier board is significant. Please place the carrier board on a firm surface, such that it does not bend during assembly. Alignment of the connectors of the carrier board and SOM is very important. When designing your own carrier board, please make sure that the exact dimensions as specified in chapter 4.3 are respected. A mechanical drawing in DXF format is available for validating proper alignment of connectors and mounting holes[1].

Although the applied Samtec carrier board connectors are of high quality, a maximum of 200 mating cycles are guaranteed. Please consider this wearing when experimenting with the SOM in combination with a carrier board.

2.1.3 Boot mode selection

The Miami MPSOC Plus SOM supports most of the boot mode resources available on the Zynq Ultrascale+. Boot modes can be set using the (optional) boot mode switches on the board. Paragraph 5.1.2 gives a detailed overview of the possible settings for a boot mode. When delivered from the factory, the module boots from the QSPI connected NOR flash memory by default, containing a minimal Linux based image. Booting this image successfully will prompt with a console interface as described in paragraph 5.2.4. Successful powering and booting of the Miami SOM from the NOR flash memory is also visualized by means of the status LEDs, as described in paragraph 5.2.1.

The boot mode switch settings can be overruled by configuration settings on the carrier board. In this case, make sure that the switches on the Miami MPSOC Plus are the PS-JTAG boot state to avoid interference.

2.2 Topic Development Kit (TDK) installation

To explore the capabilities of the Miami MPSOC Plus SOM, it can be ordered in combination with a Florida Plus carrier board and accessories, forming a development/evaluation kit. The development kit comes with an accessories bag, containing a 12Vdc mains power adapter, miscellaneous cables, SDcard, M.2 NVMe SSD, etc. More details on the functionality of the Topic Development Kit can be found in the TDKZU9P user guide [2]. The offered physical interfaces on the Florida Plus carrier board are:

- 1 Gbit/sec RJ45 Ethernet connection
- 2x USB-C
- 1x micro-USB (virtual COM port) for console
- 1x JTAG
- 1x NVMe SSD M2 interface
- 2x PMOD generic GPIO interface
- 2x (HPC) FMC ports
- User LEDs and switches

2.3 BSP configuration

The Miami MPSOC Plus SOM is supported by a Linux distribution (TLD), actively maintained by Topic. which can be downloaded from [7]. There are two flavours of the TLD:

- The Miami MPSOC Plus is delivered with a basic Linux image, called “my-image”. This binary version is integrated in the NOR flash memory of the board. Via Github, the sources of this image are available. This is a minimal Linux configuration, supporting all the on-board peripherals on the SOM.
- A more complete reference design is formed by the combination Miami MPSOC Plus and the Florida Plus. This board exposes physical interfaces, providing means to evaluate the functionality of the board. Apart from the peripheral support, additional functionality of the board is provided:
    - Remote software update webserver
    - XFCE window manager and desktop functionality
    - Support for additional peripherals, such as:
        - Keyboard/mice
        - Flash memory storage via USB-C and M2-PCIe-NVMe
        - Wifi/Bluetooth functionality via USB
        - Specific Ethernet-over-USB dongles USB webcams
    - No driver support is automatically added for:
        - PMOD extension modules
        - FMC extension modules
        - Dedicated USB peripherals, such as docking stations, video-over-USB
    - Contact support@topicproducts.com for support on custom Linux drivers

For build instructions of this image, please refer to https://github.com/topic-embedded-products/topic-platform or the TLD manual [2]. These resources form an easy starting point for developing your own Linux based applications. When accessing the Github website, you are guided through the steps to download, install and start using the software by instructions as well as installation scripts. It is highly recommended to use a Linux based development PC running e.g. an Ubuntu LTS distribution. Please refer to the Xilinx installation manuals for supported Linux development platforms. The Linux distribution contains, amongst others:

- Linux configuration and development tools (OpenEmbedded, Yocto)
- Device tree configuration files
- Cross compiler for the Zynq/Cortex-A53 processor
- BSP with drivers for all peripherals on the Miami SOM
- Uboot bootloader
- Root file system
- Generation of the SDK for the configured platform

The TDK depends also on an FPGA image as specific board functionality to connected via the FPGA fabric with the processing system. The build of the FPGA bitstream is not part of the TDK BSP build script. When building the BSP, the binary bitstream is automatically downloaded from the Topic download area http://downloads.topic.nl.

The source code for the FPGA reference design TDPZU of the development kit can also be found on the Topic download area at http://downloads.topic.nl/trd.html. The Vivado design files can downloaded as TCL scripts with accompanied IP blocks as part of a ZIP file. The readme file in the downloaded ZIP container gives instructions on the reconstruction of the applicable Vivado project. Please check on the used Vivido tool versions and compatibility. The build script is intended to create the Vivado project from scratch and build the binary image automatically. The reference design consists information on:

- Vivado block diagram design
- Constraints file for pinout and timing
- All involved IP blocks

2.4 SD-Card programming

After downloading the standard build image or successfully completing the previous build steps, you can download the binary image on the development kit using the remote software update server, your own update strategy or using an SD-card. As the SD-card cannot be a standard FAT file system, there are some prerequisites in place to create a bootable SD-card. To program the downloaded file on an SD-card (recommended is an 8Gbyte version as a minimum), insert the card in a PC and execute the following commands:

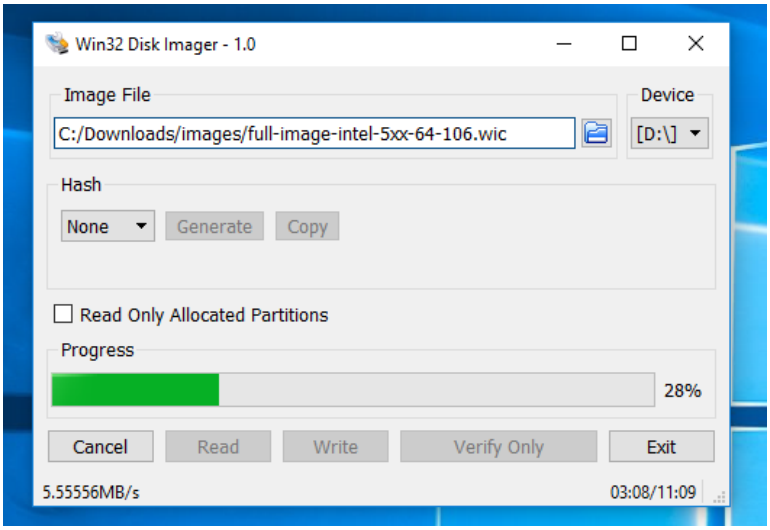
For Linux:

Insert the SD card, unmount it if it already contained a filesystem.
From a shell command line prompt type:

- wget https://downloads.topic.nl/wic/tdkzu9p/tdkzu9p.wic.gz
- umount /dev/sdX* (replace sdX with the actual SD card name, usually "sdb")
- gunzip < tdkzu9p.wic.gz | sudo dd of=/dev/sdX bs=1M

For Windows:

- *(taken from https://software.intel.com/en-us/node/721476)*
- Download the installer for Win32 Disk Imager:
  - *https://sourceforge.net/projects/win32diskimager/files/latest/download.*
- Right-click the installer file, then select Run as Administrator.
- Follow the onscreen prompts to install and open Win32 Disk Imager.
- Click the blue folder icon, then browse to the location of the SDcard image.
- Select *.* as the file type, then select the .wic image.



- From the Device drop-down list, select the drive of your device.
- *Warning: Be sure to select the correct drive. Selecting the wrong drive to write to could result in data loss. Check the name of your device in File Explorer if you're not sure which is correct.*
- Once you have the correct drive selected, click Write.
- When prompted, select Yes to start writing the image to your device.
- This process can take up to 5 minutes for a USB 3.0 drive or microSD card.
- When finished, disconnect the device from your computer.

Insert the created SD-card in the appropriate slot on the development kit, set the boot switches on the Miami MPSOC Plus to the SD-card boot state and power the board. This will load the SD-card image and start executing the content.

2.5 Software installation and application development

When developing embedded applications using the Miami MPSOC Plus SOM in combination with a carrier board, you can choose to adopt one of the two BSP configurations, described in the previous chapters and develop your software application using BitBake to manage application dependencies.

An alternative approach to application software development is to use the Topic development kit software development kit (SDK), generated from the TDPZU BSP. Instructions on the usage of the SDK can be found on the Topic download area http://downloads.topic.nl/sdk.html. The rich set of functionality covered by this SDK provides you with the ability to start implementing a custom application using the SDK of choice. Topic supports the following SDK environments:

- Xilinx Vivado SDK / Vitis
- Qt Creator

Other SDKs, like Eclipse, can also be used. However, these are not tested by the Topic support team.

It is highly recommended to use a Linux workstation to develop embedded Linux applications for the Miami MPSOC Plus module. The TDK BSP is intended to supply a rich set of functionality to develop applications. However, the Miami MPSOC Plus SOM remains an embedded platform with limited resources. If you would like to add functionality to the TDK BSP for specific application development, please contact Topic support at [9], to discuss the possibilities. With the TDK SDK you will be able to start developing applications directly when receiving the evaluation board.

2.6 Secure boot infrastructure

The Miami MPSOC Plus SOM supports all the features required to apply the secure boot infrastructure provided by the Zynq Ultrascale+ SOC. However, no active support on the implementation is provided. Please refer to Xilinx user guide UG1228, chapter 8 for an application specific security implementation approach.

2.7 Open source software

Open source software makes the software development process more efficient, cost effective and gives access to a large pool of engineers, working on the same subject. The Miami MPSOC Plus SOM with its TDPZU BSP and TLD depend heavily on open source Linux. Not all applied software is of open source origin: the proprietary software cannot be disclosed, but can be licensed. This relates to the use of e.g. Dyplo® as the application software as well as miscellaneous IP blocks in the FPGA. The latter are licensed to Xilinx and Analog Devices. However, the core operation of the Miami MPSOC Plus SOM is not dependent on these licensed IP blocks.

The use of open source software depends on its license conditions and can typically have the following implications:

- The use of open source software must be published in the final product manual.
- A party can request the open source software and on request must be delivered (only the open software software).

2.7.1 Open source statement

Topic Embedded Products (Topic) recognizes the importance of the use of open source, and is dedicated to contributing back to the open source community. Topic uses Open Source software in its products. Any code made available by Topic is for reference and informational purposes only and is distributed “as is” with no support and/or warranty of any kind intended, implied, or provided.

Important: *Topic accepts no licensing liability when modifying the BSP or using the BSP outside the context specified in the open source statement.*

Applied source code is published on GitHub (https://github.com/topic-embedded-products).

3 Miami MPSOC Plus SOM features

	SOM-MIAMI-XCZU6EG	SOM-MIAMI-XCZU9EG	SOM-MIAMI-XCZU15EG
PROCESSOR SYSTEM			
Application Processor [1]	XCZU6-EG-1FFVB1156I	XCZU9-EG-1FFVB1156I	XCZU15-EG-1FFVB1156I
CPU Architecture	ARM Cortex-A53 (quad core)		
CPU Performance [2]	Up to 1.2 GHz		
Real Time Processor	ARM Cortex R5 (dual core)		
Graphics Processor	ARM Mali™-400 MP2		
MEMORY			
Cache (Application processor)	L1: 32KB I / D per core, L2: 1MB, on chip memory 256 KByte		
Cache (Real time processor)	L1: 32KB I / D per core, tightly coupled memory 128 KByte per core		
Cache (Graphics processor)	64 KByte		
SDRAM [1]	2, ***4*** or 8 GByte DDR4 with/without ECC (assembly option 32, 64 or ***72*** bits wide)		
NOR [1]	Quad-speed SPI, (***64 MByte***, 128 MByte, 256 MByte)		
eMMC [1]	0, ***8***, 16, 32 or 64 GByte pseudo-SLC or ***MLC***		
EEPROM	32 Kbit I2C EEPROM storage		
FPGA			
Technology	Ultrascale+®		
Logic cells	469K	600K	747K
LUTs	215K	274K	341K
Flip Flops	429K	548K	682K
BRAM	25.1Mbit	32.1Mbit	26.2Mbit
UltraRAM	-	-	31.5Mbit
DSP slices	1973	2520	3528
PS transceivers	3x (6 Gbit/s each)	3x (6.0 Gbit/s each)	3x (6.0 Gbit/s each)
GTH transceivers [2]	16x (12.5 Gbit/s each)	16x (12.5 Gbit/s each)	16x (12.5 Gbit/s each)
2x120 + 1x180 pins available on SOM connector with programmable interfaces			
LAN	10/100/1000Mbps Ethernet, (PHY included), IEEE 1588 and SyncE support 10G/40G/50 G support (external PHY needed)		
Serial	UART, I2C, SPI, I2S, CAN (user configurable/selectable)		
Video	FPD link, SDI, TFT, HDMI (PL), DisplayPort (PS)		
USB	2x USB 3.0, including on-board ULPI media		
Debug	Debug UART, console, PS JTAG, PL JTAG		
PS connected I/O	PS connected 1.8V GPIO, multiplexed peripherals (MIO)		
PL connected I/O	HP and HD GPIO, 100 Ohm impedance controlled		
PS connected transceivers	3x, Display port, SATA, PCIe, USB 3.0 with integrated MAC support		
PL connected transceivers	16 lanes, 4 banks, 1 programmable clock per bank, 1 clock externally available, length matched within quads		
Power supply			
Input	5.0 – 16.0 Vdc via carrier board connector, 55 W absolute maximum power rating On-board voltage regulation and power distribution		
Output	Selectable I/O standards and voltages for HD GPIO banks		
Software			
Bootloader / BSP	U-Boot / Linux		
Boot options	JTAG, QSPI-NOR, eMMC, SD-Card, USB		
Operating System	Topic Linux distribution on GitHub		
Dyplo® compatible platform	Yes		
Mechanical and environmental			
Dimensions	95mm x 68.5mm		
Connectors	2x 120 + 1x 180 pin Samtec high performance mezzanine carrier board connectors		
Temperature	Industrial grade		

1) Configuration options possible at higher volumes, default configuration in bold italics.
2) Higher speed grade as configuration option: CPU performance up to 1.5GHz, 16Gbps transceivers

4 Miami MPSOC Plus architecture

The Miami MPSOC Plus SOM integrates various peripherals to bring up a fully functional processing system. The SOM connects to a carrier board using three high performance connectors. The following paragraphs give an overview of peripherals and devices which determine the functionality of the board. The board is designed to facilitate the use of one of the following Xilinx devices: XCZU[*6/9/15*][*C/E*]G-[*1/2*]FFVB1156[*I/E*]. The default assembled type is the XCZU9EG-1FFVB1156I.

4.1 Miami MPSOC Plus SOM board appearance

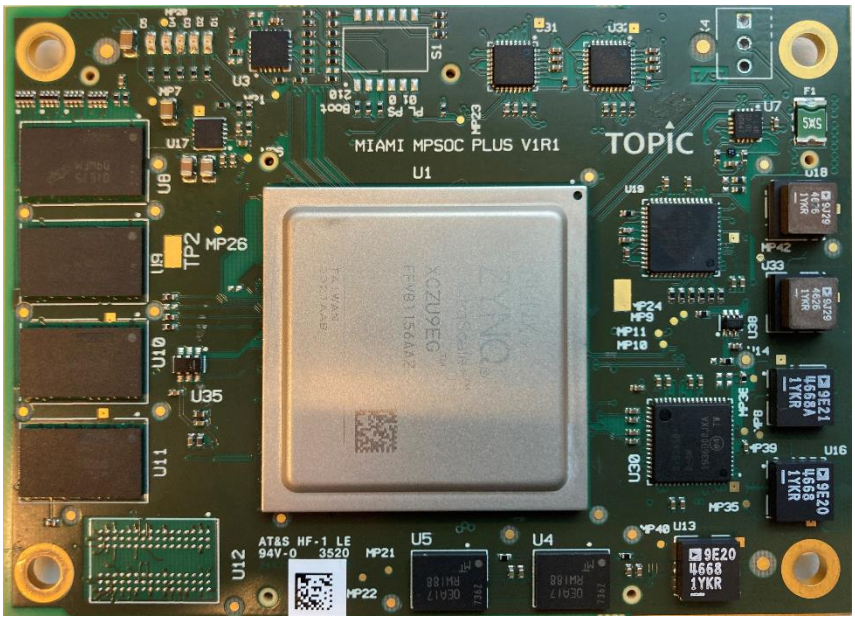


Figure 4.1: Miami MPSOC Plus board top view

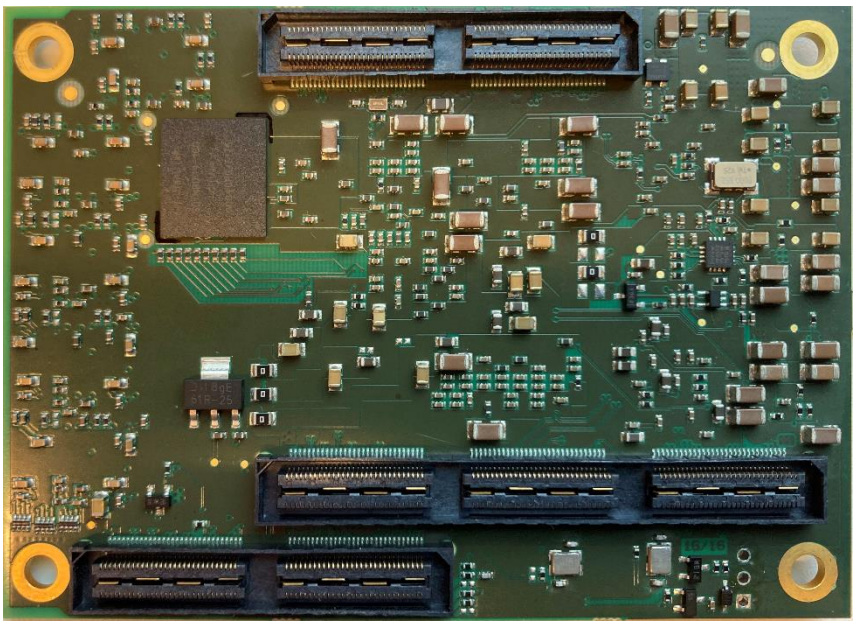


Figure 4.2: Miami MPSOC Plus board bottom view

4.2 Block diagram

The block diagram in Figure 4.3 illustrates the general functionality of the board, divided by FPGA and processor bound functionality. It is clear that the processor connected functionality is more dedicated than the free-programmable functionality of the FPGA fabric.

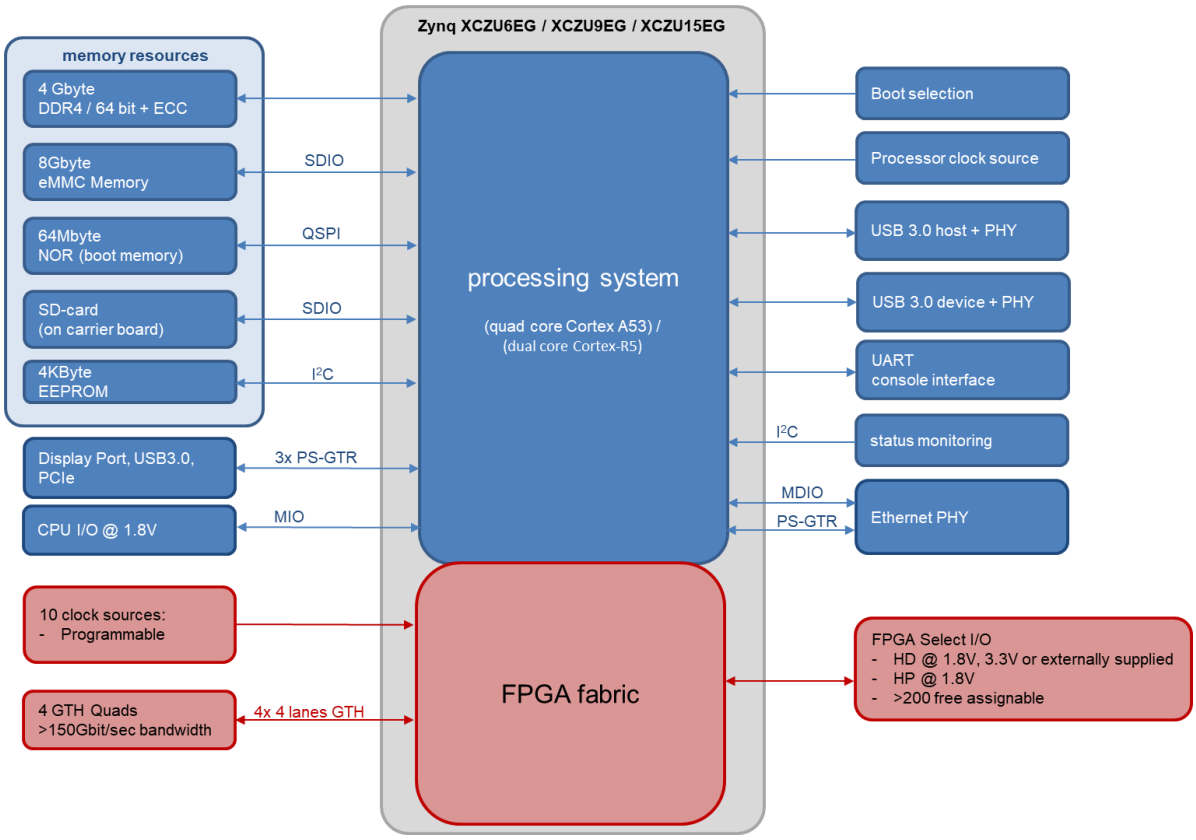


Figure 4.3: Block diagram of the Miami MPSOC Plus SOM

4.3 Mechanical description

The Miami MPSOC Plus SOM should be fitted on a carrier board using three mating connectors:

Part type (carrier board)	2x Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x 60 pins banks), stacking height 5mm
Part type (carrier board)	1x Samtec, QTH-090-01-L-D-A, High Speed ground plane socket, 180 pins (3x 60 pins banks), stacking height 5mm

The exact relative placement details of the connectors, the guide holes for the connectors and the standoff holes are described in figure 4.4. The exact measurement details can be downloaded from the support website as a DXF object [1] to match the Miami SOM footprint exactly on your carrier board layout floor plan. An optional IDF/STEP 3D file [3] is also available, to validate how the Miami MPSOC SOM module fits within your enclosure. Please respect the production tolerances as specified in the Samtec datasheets.

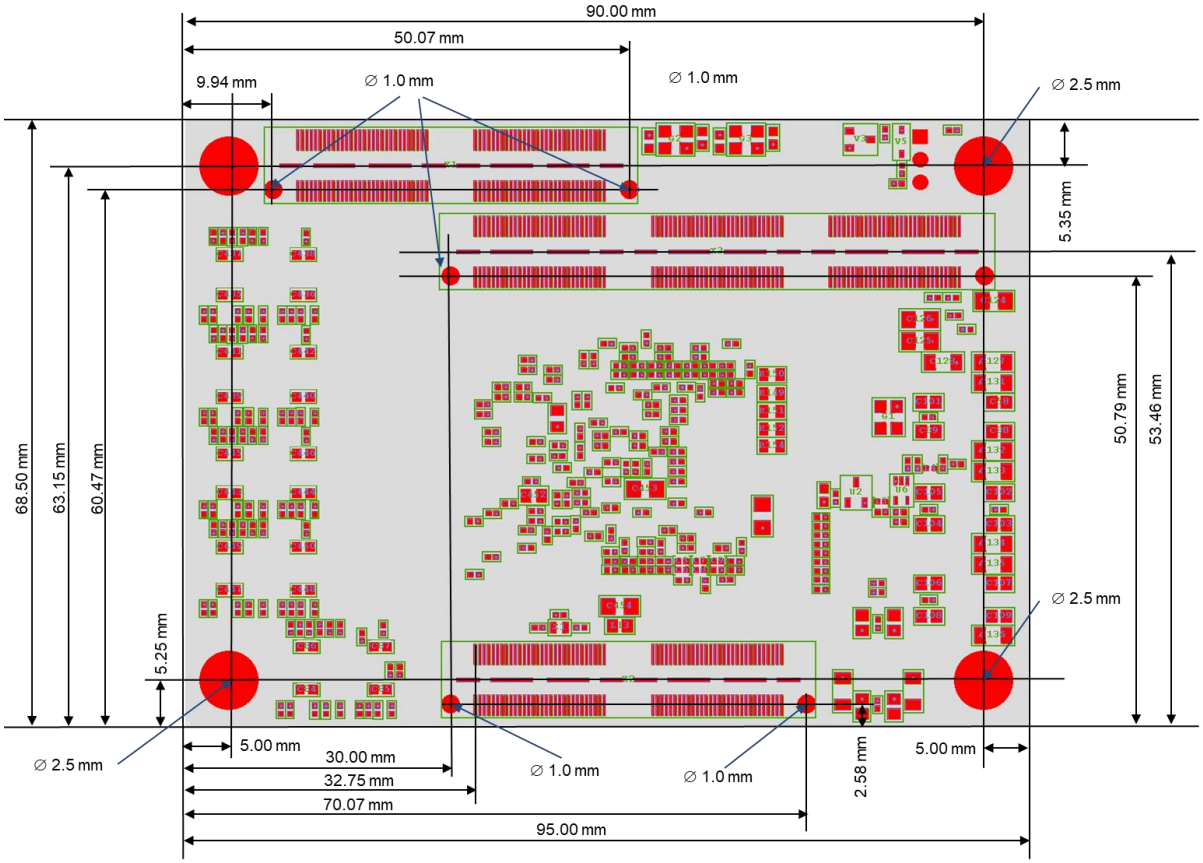


Figure 4.4:Mechanical dimensions Miami MPSOC Plus

Special attention must be given for mounting and removing the SOM from the carrier board. Samtec recommends lifting the connectors in a straight vertical movement. This requires specific tooling which is not standard available. Alternatively, careful alternating twisting with small force in the length direction removes the module from the carrier board. Due to the limited mating cycles of the connectors, this should be performed as little as possible. A maximum of 200 mating cycles is specified by Samtec.

5 Miami MPSOC Plus board functions

The functionality of the SOM module can be divided in different function groups:

- Configuration and debug interfaces
- Memory resources
- Communication interfaces
- Miscellaneous functionality

5.1 Default/recommended PS MIO pin mapping

In Table 5.1 a mapping of functionality within the Zynq PS is shown. This mapping is targetting the Topic Reference Design (TRD) configuration. The original source table can be found at [4]. This table also provides options for alternative interfaces, and the implications for using these.

Peripheral	MIO																				GT Lanes			
	0-12	13-23	24	25	26	27	28-29	30-31	32-33	34-35	36	37	38	39-41	42-43	44	45-51	52-63	64-75	76-77	GT_0	GT_1	GT_2	GT_3
Default Selections																								
QSPI	■																							
eMMC (SD_0)		■																						
SD_1																■	■							
I2C_0										■														
I2C_1							■																	
UART_0								■																
GPIO									■		■	■	■											
GEM 2 (With MDIO)																				■			■	
USB_0 (USB3-GT lane 2)																		■				■		
USB_1 (USB3-GT lane 3)																			■					■
IRQ of CLOCK GEN					■																			
SWITCH PS0			■																					
pin LED2/INT of ETH PHY						■																		
PCIe													■								■			
Alternative Options																								
SD_0		■	■	■																				
Kernel alive				■																				
PJTAG/SPI													■	■	■									
Display port										■	■	■										■		
IRQ						■																		

Table 5.1: Zynq MIO mapping

Notes:

- *Dedicated USB reset pins are controlled using I2C programmed distributed GPIO*
- *Although MIO_26 is a viable option to use for the ETH_FB clock, this pin is not available for implementation. The FB clock must be routed through EMIO if it is to be used.*
- *For SD_1 the following additional mapping applies:*
  - *CD – MIO_45*
  - *WP – MIO_44 assigned*

In the following paragraphs the functions are explained from a user perspective to help understand the context to use and program the functionality.

5.2 Configuration and debug interfaces

In the figures 5.2.a and 5.2.b the configuration and debug interfaces of the Miami MPSOC Plus are illustrated. The figures illustrate clearly that most signals required for this are accessible via the SOM connector and have to be disclosed via the carrier board. All Topic Florida carrier boards allow access to these interfaces.

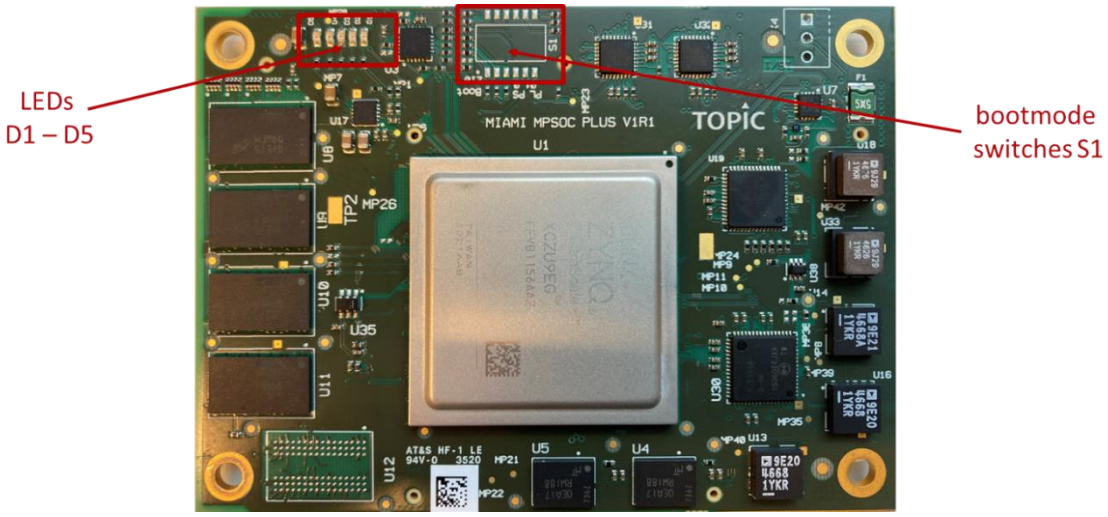


Figure 5.2.a: Configuration and debug interfaces top

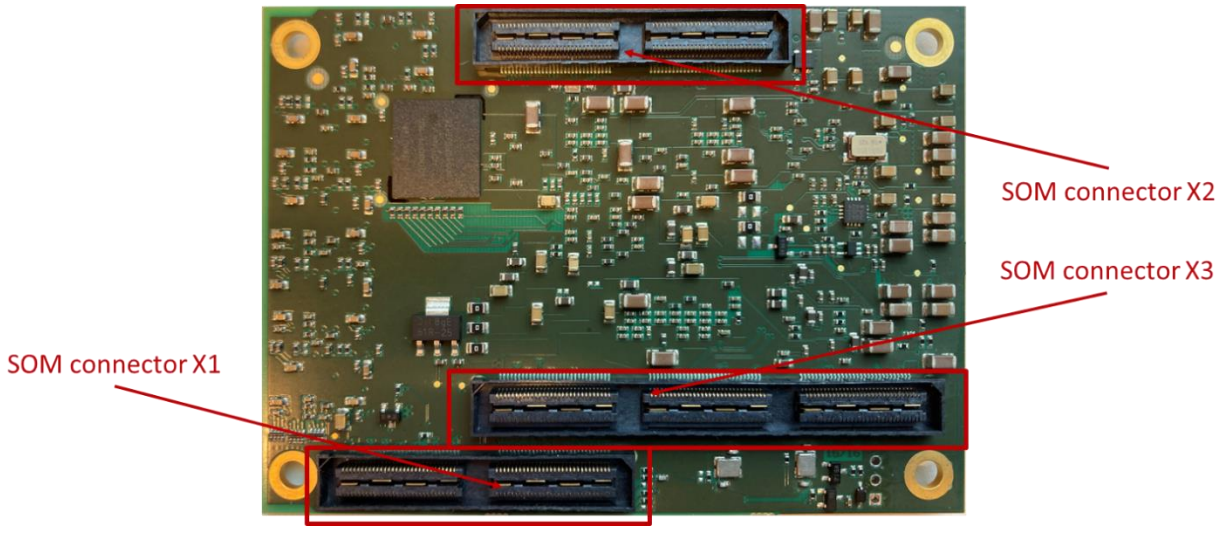


Figure 5.2.b: Configuration and debug interfaces bottom

5.2.1 Status LEDs

There are 5 status LEDs provided on the Miami MPSOC Plus boards. These indicate the operational status of the board from a system and user perspective.

LED reference	FPGA pin	Description
D1	AL12 (IO_L6N_HDGC_AD6N_44) (LVCMOS33)	FPGA user LED. By default this LED will be off. When booting a standard Topic image, this LED will blink to indicate a fully operational FPGA image. However, the LED is available for the user to give it any function.
D4	W21	FPGA image not ready. When active (illuminated), the FPGA part of the Zynq Ultrascale+ is not loaded yet or properly configured. When programmed with a valid bit stream, the LED will be turned off.
D2	n.a.	User LED2. This LED is controlled by the I2C GPIO expander. By default this LED will be off. However, the LED is available for the user to give it a different function.
D3	n.a.	Power-good LED. When active, the primary power supplies on the board are up and within operational limits. When the Miami board is powered by the main power rail, this must be the case.
D5	AE19 (PS_MIO25)	CPU alive LED. This LED is controlled by the processor system. By default a kernel controlled heartbeat signal is applied to the LED to indicate proper operation of the software. However, the LED is available for the user to give it a different function.

Table 5.3: LED descriptions

5.2.2 Boot mode selection switches

The first stage boot loader of the processor loads the initial boot code from a selectable source: JTAG, NOR memory, NAND memory (eMMC or SD-card) or via USB. This boot mode strapping is configurable using 3 positions of the 6 positions dipswitch S1, via a configurable resistor bank or via the SOM connector. The last two options are available as customization option.

S1.x = switch reference

S1.1 = boot mode selection bit 0
S1.2 = boot mode selection bit 1
S1.3 = boot mode selection bit 2
S1.4 = PS user signal (MIO24)
S1.5 = PL user signal (IO_l9N_AD3N_44)
S1.6 = PL user signal (IO_l9P_AD3P_44)

= on state = '1'
= off state = '0'

Table 5.4: Boot switch physical location and assignment

Switch S1 *S1.3 – S1.2 – S1.1*	Position	Boot source	PS boot role
0 0 0		PS JTAG	Slave
0 0 1		QSPI 24 bit addressing (not recommended)	Master
0 1 0		QSPI 32 bit addressing	Master
0 1 1		SD0 SD-card 2.0 FAT 16/32 flash memory	Master
1 0 0		NAND flash (not supported)	Master
1 0 1		SD1 SD-card 2.0 FAT 16/32 flash memory	Master
1 1 0		eMMC1.8V	Master
1 1 1		USB0 (2.0) via DFU protocol	Slave

Table 5.4: Boot switch settings descriptions

For more details on the boot mode selection and implications, please refer to Xilinx user guide UG1085 chapter 11 [6]. Note that booting is a critical process. The most reliable memory resource to boot from is the QSPI NOR flash. NAND flash memory is less reliable in terms of data retention and durability. Therefore, Topic highly recommends initiating booting (e.g. Uboot) from the NOR flash and continue booting (e.g. Linux kernel) from the eMMC. Please contact Topic to discuss implementation details for reliability considerations.

If it is not desirable to implement a mechanical switch on the board, switch S1 can be omitted as an assembly option. Configuring the right boot mode can be done in two alternative manners:

- Assembly of the optional configuration resistors with the right settings to select the boot mode. By default, the mode pins are pulled high. Using a 0 Ohm resistor soldering option to ground, the mode signal can be tied to ground.
- Selection of the boot mode by controlling the applicable SOM connector pins. By default, the mode pins are pulled high. On the carrier board the signal should be pulled to ground to enforce a logic low value. Otherwise, it should be high impedance.

SOM Signal	SOM pin	FPGA pin	Electrical
PS_MODE0	X1.A8	T22 (PS_MODE0)	1V8 open drain input
PS_MODE1	X1.A37	R22 (PS_MODE1)	1V8 open drain input
PS_MODE2	X1.A55	T23 (PS_MODE2)	1V8 open drain input
-	-	R23 (PS_MODE3)	Tied to GND (possible to tie to 1V8)

Table 5.2: Mode pins connections

5.2.3 JTAG interfaces

The Xilinx Zynq Ultrascale Plus has a dedicated and an optional JTAG port assigned via the SOM connector:

- PL_JTAG. This is the default JTAG port, connected to the dedicated JTAG pins on the Zynq Ultrascale+ device. It uses 1.8V signal levels. The applicable pull-up resistors are integrated on the Miami MPSOC Plus SOM. Using the PL-JTAG port you can:
  - Program the FPGA fabric
  - Use the ILA (Integrated Logic Analyzer) to debug the programmed FPGA logic
  - Boundary scan for production verification
  - Debug the processor software using the ARM CoreSight Debug Access Port (DAP)

PL_JTAG signals	FPGA pin	SOM pin	Description
PL_TDI	U25 (PS_JTAG_TDI)	X1.B53	Dedicated package pin
PL_TDO	T25 (PS_JTAG_TDO)	X1.B59	Dedicated package pin
PL_TCK	R25 (PS_JTAG_TCK)	X1.B57	Dedicated package pin
PL_TMS	R24 (PS_JTAG_TMS)	X1.B55	Dedicated package pin
PL_JTAG_RSTN	n.a.	X1.B51	Available for the software debugger to enforce a soft reset to the processor system.
JTAG_VREF	n.a.	X1.A44	Reference voltage for JTAG programmer. (1V8)

Table 5.3: JTAG pin connections

- PS_JTAG. This is a secondary JTAG port and multiplexed with PS MIO pins. The benefit of this port is that you can simultaneously debug the PS and PL functionality, without compromising bandwidth on the JTAG link and reducing problems where applications share the a JTAG probe. Making use of this feature requires:
  - Reprogramming of the MIO port pin assignments
  - Provisions on the applied carrier board to instrument a JTAG probe on these pins

PS_JTAG signals	FPGA pin	SOM Signal name	SOM pin	Description
PS_TDI	N23 (PS_MIO_39)	IO_S_VCC4_18	X1.B33	Dedicated package pin
PS_TDO	M23 (PS_MIO_40)	IO_S_VCC4_19	X2.B31	Dedicated package pin
PS_TCK	L23 (PS_MIO_38)	IO_S_VCC4_1	X1.A41	Dedicated package pin
PS_TMS	J24 (PS_MIO_41)	IO_S_VCC4_3	X1.A45	Dedicated package pin

Table 5.4: PS_JTAG pin connections

5.2.4 Console interfaces

A primary software development interface is the console connection to the processing system, available via the SOM connector. The Miami SOM provides a fixed console connection directly on the MIO port of the processing system.

Console signals	FPGA pin	SOM Signal name	SOM pin	Description
UART_RXD	L21 (PS_MIO_30)	IO_S_VCC4_15	X1.B3	Serial data from other device to processor. Can be used for other functionality if needed.
UART_TXD	J22 (PS_MIO_31)	IO_S_VCC4_14	X1.B1	Serial data from processor to other device. Can be used for other functionality if needed.

Table 5.5: UART pin connections

The console signals are available on the carrier board connector X1. The signals are 1.8V CMOS logic levels compatible. The console interface default settings are

- 115200 baud rate,
- 8 data bits,
- 1 stop bit and
- no parity or flow control.

5.2.5 Resetting the Miami MPSOC Plus SOM

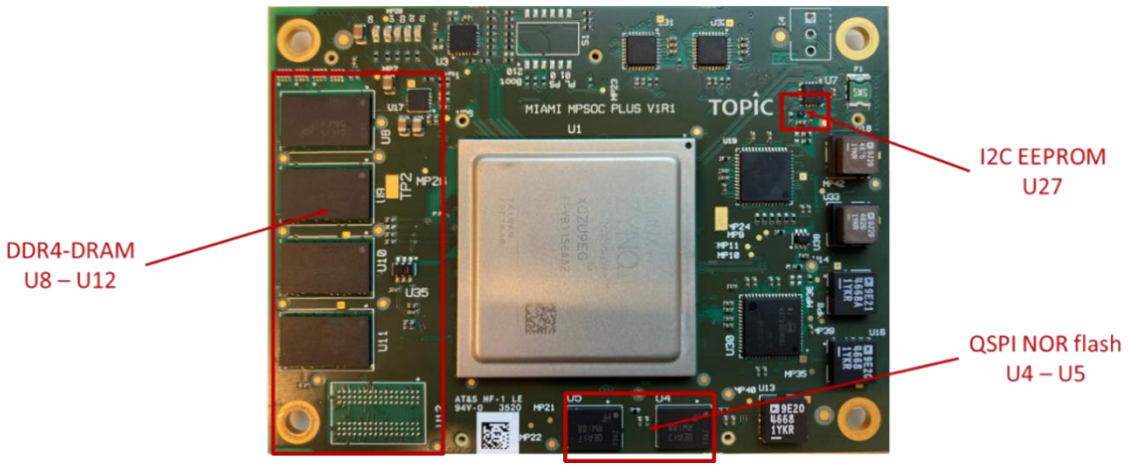
The Miami SOM facilitates different reset options (all signals are active low). See the table below.

SOM signal name	Connector pin	Description
SOM_RST_N	X1.A10	Hardware reset signal of the SOM, this pin activates the System Reset (PS_PROG_B, PS_POR_B FPGA pins) of the FPGA.
SW_RST_N	X1.B5	An active signal on these pins activates the System Reset (debug mode) (PS_SRST_B FPGA pin) of the FPGA.
PL_JTAG_RST_N	X1.B51	
USB0_RESET_N (BOOT_EXT_1)	X1.A37	Reset signal intended for resetting USB devices. If not used, this signal can be used for I/O purposes. This signal is accessible through the I2C GPIO expander.

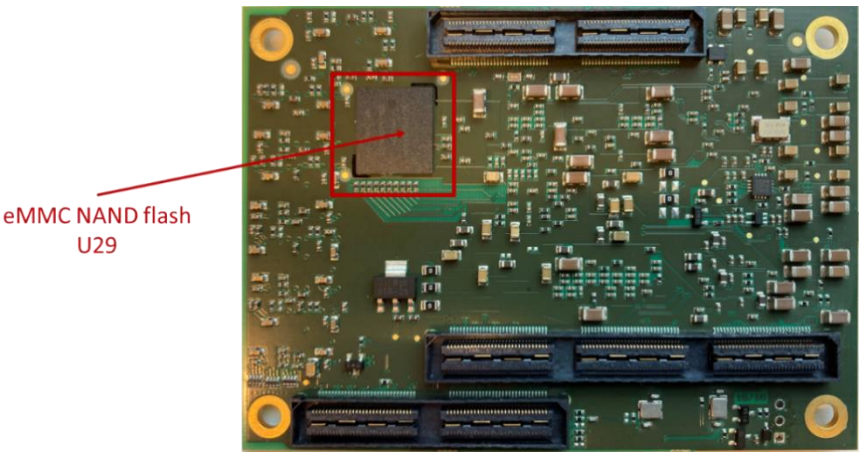
Table 5.6: Reset pin connections

Refer to Xilinx document UG1085 (Zynq UltraScale+ MPSoC technical reference guide) chapter 38 for more details on resetting sources.

5.3 Memory resources



(a)



(b)

Figure 5.1: Miami MPSOC Plus SOM Memory resources (a) top, (b) bottom

5.3.1 DDR4 SDRAM memory (MT40A512M16)

A 72 bit wide DDR4 SDRAM memory solution is provided as the main system memory, providing ECC protected 64 bit wide bus at 2.4 GT/s. This gives more than 100 Gbit/s effective bandwidth on the DDR memory. The DDR clock frequency is configured by the software configuration using PLL1 clock output 2, which is the standard DDR clock output. The size of the DDR4 SDRAM memory is 2GB, 4GB or 8GB, where 4GB is the standard assembled option.

The solution is built using 16-bit wide DDR4 SDRAM memory chips. The devices are connected to the dedicated DDR memory controller interface on the Zynq Ultrascale+, allowing both the PL and the PS access to the memory with high data bandwidth.

The Miami MPSoC Plus can be assembled with the following memory configuration:

Applied DDR4 device	32 bit option	64 bit option	72 bit option
MT40A256M16	---	2 GByte	2 GByte with ECC
MT40A512M16	2 GByte	4 GByte	**4 GByte with ECC(default)**
MT40A1G16	4 GByte	8 GByte	8 GByte with ECC

Table 5.7: DDR assembly options

5.3.2 Serial quad SPI NOR flash memory (MT25QU256)

The on-board quad SPI NOR flash memory offers a reliable boot memory source with sufficient storage capacity to hold a moderate embedded Linux distribution(32MB) as well as a bitstream image. The table below illustrates the size of an uncompressed bitstream for the supported devices.

Device	Bitstream size (bits, uncompressed)
XCZU6	212.086.240
XCZU9	212.086.240
XCZU15	229.605.952

Table 5.8: Device configuration file sizes

The Miami MPSoC Plus can be assembled with the following quad-SPI NOR flash devices.

Assembled device	NOR flash storage size
MT25QU256	**64 MByte (default assembly option)**
MT25QU512	128 MByte
MT25QU01	256 MByte
MT25QU02	512 MByte

Table 5.9: QSPI assembly options

The Miami MPSoC Plus assigns the NOR flash to fixed processing system MIO pins. The following table describes which pins are being used by the quad SPI controller.

SPI NOR flash signal name	FPGA pin	FPGA pin label
QSPI1_DQ0	AH16	PS_MIO_4
QSPI1_DQ1	AJ16	PS_MIO_1
QSPI1_DQ2	AD16	PS_MIO_2
QSPI1_DQ3	AG16	PS_MIO_3
QSPI1_CLK	AF16	PS_MIO_0
QSPI1_CS_N	AM15	PS_MIO_5
QSPI2_DQ0	AE17	PS_MIO_8
QSPI2_DQ1	AP15	PS_MIO_9
QSPI2_DQ2	AH17	PS_MIO_10
QSPI2_DQ3	AF17	PS_MIO_11
QSPI2_CLK	AJ17	PS_MIO_12
QSPI2_CS_N	AD17	PS_MIO_7
Feedback Clk	AL15	PS_MIO_6

Table 5.10: QSPI pin connections

5.3.3 eMMC memory (SDINBDG4-8G-XI)

The Miami MPSOC Plus integrates eMMC memory connected to the MIO SDIO interface as external storage device or as a boot source. The eMMC memory is an assembly option. The following assembly configurations are offered:

Capacity	Type number
8 Gbyte	**SDINBDG4-8G-XI (default assembly option)**
16 GByte	SDINBDG4-16G-XI
32 GByte	SDINBDG4-32G-XI
64 GByte	SDINBDG4-64G-XI

Table 5.11: eMMC assembly options

The selected eMMC are from the SanDisk® iNAND® 7250 Industrial Embedded Flash Drives family devices. This is MLC NAND flash technology. For high-reliability purposes, eMMC MLC NAND flash can have limitations:

- The storage temperature of -51ºC is not offered from qualified sources. When using the eMMC flash memory in an application that requires storage temperatures of less than -40ºC, an alternative device must be selected and assembled.
- The applied NAND flash is MLC. A limitation of MLC is the number of write cycles. When using double the size of the needed memory space of the application, this drawback can be mitigated.

Both options are alternative assembly options. Please contact Topic Product sales support to discuss the possibilities. Also take note that it is recommended that for high-reliability operation the QSPI connected NOR flash memory is available. This way, the system can be booted reliably from NOR flash and the eMMC NAND flash data can be used in a controlled way, including the use of the file system error correction capabilities.

5.3.4 SD-card memory interface (via carrier board)

Optionally, the Miami MPSOC Plus can be booted from an SD-card, mounted on the carrier board if implemented. The pins available for the SD-card are part of the MIO peripheral multiplexer. This means that on this Miami, a total of 2 SD-card interfaces are available as media interfaces. Apart from using the interfaces for NAND flash memory solutions, it is also possible to use this for WiFi/BlueTooth modules for example.

The SDIO interface is operated at 1.8V. This may require the use of a level converter on the carrier board to properly interface with the SDIO controller.

The following table addresses the involved signals for carrier board implementation and software control.

Signal name	SOM Signal name	SoM pin	FPGA pin	FPGA pin label
uSD_CLK	IO_S_VCC4_6	X1.A48	N25	PS_MIO_51
uSD_CMD	IO_S_VCC4_10	X1.A54	P25	PS_MIO_50
uSD_DQ0	IO_S_VCC4_12	X1.A58	J25	PS_MIO_46
uSD_DQ1	IO_S_VCC4_8	X1.A50	L25	PS_MIO_47
uSD_DQ2	IO_S_VCC4_4	X1.A46	M25	PS_MIO_48
uSD_DQ3	IO_S_VCC4_9	X1.A52	K25	PS_MIO_49
uSD_DETECT	IO_S_VCC4_11	X1.A56	P24	PS_MIO_45
uSD_WP	IO_S_VCC4_13	X1.A60	N24	PS_MIO_44

Table 5.12: SD-card connection pins

5.3.5 EEPROM memory (M24C32)

The SOM provides a 32Kbit I²C connected M24C32 EEPROM device for storing parameters and other configuration and user settings. This device is connected to the Miami system I²C bus, accessible via the following MIO pins of the processor system. *Refer to the datasheet of the M24C32 regarding information how to use this device. Be aware that 16 highest address words available are reserved by the system for the serial number and administrative parameters. Take care not to overwrite this data.*

I2C bus signal name	SOM Signal name	SOM pin	FPGA pin	FPGA pin label
SCL_1V8	IO_S_VCC4_5	X1.A47	L22	PS_MIO34
SDA_1V8	IO_S_VCC4_7	X1.A49	P22	PS_MIO35

Table 5.13: EEPROM (I2C) connection pins

I²C address EEPROM memory	0x51 / 0x59

5.4 Communication interfaces

5.4.1 Gigabit Ethernet

The Zynq MPSoC implements a 10/100/1000Mb Ethernet PHY on the SOM, connected via a GTR transceiver (MGT2) of the processing system (PS). This enables the use of the Ethernet port by software without the need to program the FPGA fabric. The applied PHY is a Marvell 88E1512P, supporting synchronous Ethernet and IEEE1588. For selection of a recommended media transformer on the carrier board, please refer to the Marvell datasheets of the 88E1512P. The SOM is delivered with a Topic specific MAC address, flashed into the EEPROM. Specific MAC address ranges can be requested.

More Ethernet connections cannot be implemented on the processor side because of available MIO signals and other assigned peripherals.

Additional Ethernet connections can be established using the FPGA connected I/O pins. Using the Select I/O pins, RGMII interfaces are recommended to be used when implementing 10/100/1000 Mb Ethernet connectivity. In case of 10Gb Ethernet or higher, gigabit transceiver-based implementations are required. Using a quad of transceivers, Ethernet connections of 50 Gb/s are possible. The use of SFP+ or QSFP copper and optical solutions are recommended.

Ethernet connectivity is supported by several IP blocks from the Vivado IP catalog. *For more information on this subject, contact support@TopicEmbeddedProducts.com. Regarding the high-end performance capabilities of the Gigabit Ethernet Controller (GEM) refer to Xilinx document UG1085 (Zynq UltraScale+ MPSoC TRM technical reference guide) chapter 34.*

5.4.2 USB 3.0

The Miami MPSOC Plus SOM supports 2 USB PHYs (ULPI) on the board itself. Both ports can be used as host or as device. Usage of the USB connection as an OTG compliant port is dependent on the software drivers applied. Using the ULPI devices, the port is USB 2.0 OTG compliant. The USB PHYs are connected directly to the MIO pins of the processing system. These MIO pins are not available for implementing other peripheral functionality. The FPGA fabric is available for this, using EMIO bridges or connecting softcore peripheral IP in the programmable logic.

By adding the one or two of the GTR transceiver pairs to the USB pinout, a USB 3.1 or 3.0 connection can be established with a maximum data throughput rate of 5Gbit/sec. Combining the PHY signals with the gigabit transceivers on the carrier board will give a compliant USB port.

The following signals of the Zynq Ultrascale+ are assigned to implement the USB functionality:

Signal name	SoM signal name	SoM pin	FPGA pin	FPGA pin label
USB_CLK	-	-	F22	PS_MIO52
USB_DIR	-	-	E23	PS_MIO53
USB_STP	-	-	G23	PS_MIO58
USB_NXT	-	-	B23	PS_MIO55
USB_DQ0	-	-	C23	PS_MIO56
USB_DQ1	-	-	A23	PS_MIO57
USB_DQ2	-	-	F23	PS_MIO54
USB_DQ3	-	-	B24	PS_MIO59
USB_DQ4	-	-	E24	PS_MIO60
USB_DQ5	-	-	C24	PS_MIO61
USB_DQ6	-	-	G24	PS_MIO62
USB_DQ7	-	-	D24	PS_MIO63
USB_RESET	-	-	n.a.	Connected to the processor system using an I^2C I/O expander

Table 5.14 (a): USB0 FPGA pin connections

Signal name	SoM signal name	SoM pin	FPGA pin	FPGA pin label
USB_CLK	-	-	A25	PS_MIO64
USB_DIR	-	-	A26	PS_MIO65
USB_STP	-	-	C26	PS_MIO70
USB_NXT	-	-	B25	PS_MIO67
USB_DQ0	-	-	B26	PS_MIO68
USB_DQ1	-	-	B27	PS_MIO69
USB_DQ2	-	-	A27	PS_MIO66
USB_DQ3	-	-	C27	PS_MIO71
USB_DQ4	-	-	E25	PS_MIO72
USB_DQ5	-	-	H24	PS_MIO73
USB_DQ6	-	-	G25	PS_MIO74
USB_DQ7	-	-	D25	PS_MIO75
USB_RESET	-	-	n.a.	Connected to the processor system using an I^2C I/O expander

Table 5.15 (b): USB1 FPGA pin connections

Pin label	Connector pin	FPGA pin	Description
USB0_OTG_DP	X3.B51		
USB0_OTG_DM	X3.B53		
USB0_ID	X3.B55		
USB0_5V	X3.B57		
PS_MGT_D_RX_1P	X2.B22	AA31	High-speed lines used for USB3.0 implementation
PS_MGT_D_RX_1N	X2.B24	AA32	High-speed lines used for USB3.0 implementation
PS_MGT_D_TX_1P	X2.B3	Y29	High-speed lines used for USB3.0 implementation
PS_MGT_D_TX_1N	X2.B5	Y30	High-speed lines used for USB3.0 implementation
USB1_OTG_DP	X3.B52		
USB1_OTG_DM	X3.B54		
USB1_ID	X3.B56		
USB1_5V	X3.B58		
PS_MGT_D_RX_3P	X2.B10	V33	High-speed lines used for USB3.0 implementation
PS_MGT_D_RX_3N	X2.B12	V34	High-speed lines used for USB3.0 implementation
PS_MGT_D_TX_3P	X2.B9	V29	High-speed lines used for USB3.0 implementation
PS_MGT_D_TX_3N	X2.B11	V30	High-speed lines used for USB3.0 implementation

Table 5.16: USB phy connections and pins

Note: Only USB0 possible for boot

5.4.3 SDIO

The Zynq MPSoC contains 2 embedded SDIO controllers. One controller is used by the on-board eMMC flash memory device. The second controller, through MIO pins, is exposed to the carrier board and can be used for a bootable SD-card or e.g. WiFi/BlueTooth module. With a different pin multiplexer configuration other functionality can also be assigned to these pins. When it is not required to boot from an SDIO connected SD-card image/eMMC memory, both SDIO controllers can be accessed via the MIO processor pins or via the FPGA fabric. Be aware that the use of an SDIO interface via FPGA fabric requires specific design constraints for proper operation. IP blocks covering this functionality are available via our webshop. *For more information on this subject, contact [9]. Regarding the usage of the SDIO controller refer to Xilinx document UG1085 (Zynq UltraScale+ MPSoC technical reference guide) chapter 26.*

5.4.4 PS based transceiver pairs

The Miami MPSoC Plus provides 3 GTR transceiver links from the processing system. The fourth pair is used for connecting the on-board Ethernet PHY.

The PS connected transceivers can be used for USB, Ethernet, PCIe, SATA or DisplayPort connectivity. They are connected with direct PS controlled MAC peripherals. Controlling these interfaces do not need FPGA fabric.

The available options for connections is indicated in the table below

Connection label	Connector pins (RX)	Connector pins (TX)	Primary mapping	Alternative mapping
PS_MGT_D_0	X2.B16/B18	X2.B15/17	PCIe	Custom
PS_MGT_D_1	X2.B22/B24	X2.B3/B5	USB0 (boot)	Display port / custom
PS_MGT_D_2	--	--	Ethernet	Not available
PS_MGT_D_3	X2.B10/B12	X2.B9/B11	USB1	Custom

Table 5.17: USB mapping

5.4.5 PL based transceiver lanes

The Miami MPSoC Plus provides four quads of differential GTH transceiver lanes from the FPGA fabric to the connectors. Every quad of transceivers is accompanied with a differential clock signal input for external synchronization purposes from the carrier board. On the Miami MPSOC Plus, a clock synthesis chip is integrated that is connected to the second clock input of each quad. This allows for a high flexibility on clock resources, where every quad can be operated from different clock sources.

The PL connected GTH transceivers can be assigned to any differential communication protocol. This can be at individual transceiver pair level or per quad. This leads to a theoretical communication bandwidth of at least 150 Gbit/s for both transmit and receive. For the full functionality of the transceivers see UG1085 Zynq UltraScale+ MPSoC technical reference guide.

Software IP to make the transceivers work at the PS side require driver support from the applied operating system, e.g. Linux. IP integrated in the Xilinx MPSoC may require puchased licenses in addition to drivers for software integration with the PS.

The following table gives an overview of the transciever connector assignments.

SoM signal name	SoM pin	FPGA pin	FPGA pin label
MGT_D_REFCLK_0_P	--	L8	MGTREFCLK0P_228
MGT_D_REFCLK_0_N	--	L7	MGTREFCLK0N_228
MGT_D_REFCLK_1_P	X3.A27	J8	MGTREFCLK1P_228
MGT_D_REFCLK_1_N	X3.A29	J7	MGTREFCLK1N_228
MGT_D_REFCLK_2_P	--	G8	MGTREFCLK0P_229
MGT_D_REFCLK_2_N	--	G7	MGTREFCLK0N_229
MGT_D_REFCLK_3_P	X3.A52	E8	MGTREFCLK1P_229
MGT_D_REFCLK_3_N	X3.A54	E7	MGTREFCLK1N_229
MGT_D_REFCLK_4_P	--	C8	MGTREFCLK0P_230
MGT_D_REFCLK_4_N	--	C7	MGTREFCLK0N_230
MGT_D_REFCLK_5_P	X3.B21	B10	MGTREFCLK1P_230
MGT_D_REFCLK_5_N	X3.B23	B9	MGTREFCLK1N_230
MGT_D_REFCLK_6_P	--	G27	MGTREFCLK0P_130
MGT_D_REFCLK_6_N	--	G28	MGTREFCLK0N_130
MGT_D_REFCLK_7_P	X3.B46	E27	MGTREFCLK1P_130
MGT_D_REFCLK_7_N	X3.B48	E28	MGTREFCLK1N_130
			Bank 228
MGT_D_RX_0_P	X3.A3	T2	MGTHRXP0_228
MGT_D_RX_0_N	X3.A5	T1	MGTHRXN0_228
MGT_D_TX_0_P	X3.A15	R4	MGTHTXP0_228

MGT_D_TX_0_N	X3.A17	R3	MGTHTXN0_228
MGT_D_RX_1_P	X3.A4	P2	MGTHRXP1_228
MGT_D_RX_1_N	X3.A6	P1	MGTHRXN1_228
MGT_D_TX_1_P	X3.A16	P6	MGTHTXP1_228
MGT_D_TX_1_N	X3.A18	P5	MGTHTXN1_228
MGT_D_RX_2_P	X3.A9	M2	MGTHRXP2_228
MGT_D_RX_2_N	X3.A11	M1	MGTHRXN2_228
MGT_D_TX_2_P	X3.A21	N4	MGTHTXP2_228
MGT_D_TX_2_N	X3.A23	N3	MGTHTXN2_228
MGT_D_RX_3_P	X3.A10	L4	MGTHRXP3_228
MGT_D_RX_3_N	X3.A12	L3	MGTHRXN3_228
MGT_D_TX_3_P	X3.A22	M6	MGTHTXP3_228
MGT_D_TX_3_N	X3.A24	M5	MGTHTXN3_228
			Bank 229
MGT_D_RX_4_P	X3.A28	K2	MGTHRXP0_229
MGT_D_RX_4_N	X3.A30	K1	MGTHRXN0_229
MGT_D_TX_4_P	X3.A40	K6	MGTHTXP0_229
MGT_D_TX_4_N	X3.A42	K5	MGTHTXN0_229
MGT_D_RX_5_P	X3.A33	J4	MGTHRXP1_229
MGT_D_RX_5_N	X3.A35	J3	MGTHRXN1_229
MGT_D_TX_5_P	X3.A45	H6	MGTHTXP1_229
MGT_D_TX_5_N	X3.A47	H5	MGTHTXN1_229
MGT_D_RX_6_P	X3.A34	H2	MGTHRXP2_229
MGT_D_RX_6_N	X3.A36	H1	MGTHRXN2_229
MGT_D_TX_6_P	X3.A46	G4	MGTHTXP2_229
MGT_D_TX_6_N	X3.A48	G3	MGTHTXN2_229
MGT_D_RX_7_P	X3.A39	F2	MGTHRXP3_229
MGT_D_RX_7_N	X3.A41	F1	MGTHRXN3_229
MGT_D_TX_7_P	X3.A51	F6	MGTHTXP3_229
MGT_D_TX_7_N	X3.A53	F5	MGTHTXN3_229
			Bank 230
MGT_D_RX_8_P	X3.B9	D2	MGTHRXP0_230
MGT_D_RX_8_N	B3.B11	D1	MGTHRXN0_230
MGT_D_TX_8_P	X3.A57	E4	MGTHTXP0_230
MGT_D_TX_8_N	X3.A59	E3	MGTHTXN0_230
MGT_D_RX_9_P	X3.B10	C4	MGTHRXP1_230
MGT_D_RX_9_N	X3.B12	C3	MGTHRXN1_230
MGT_D_TX_9_P	X3.A58	D6	MGTHTXP1_230
MGT_D_TX_9_N	X3.A60	D5	MGTHTXN1_230
MGT_D_RX_10_P	X3.B15	B2	MGTHRXP2_230
MGT_D_RX_10_N	X3.B17	B1	MGTHRXN2_230
MGT_D_TX_10_P	X3.B3	B6	MGTHTXP2_230
MGT_D_TX_10_N	X3.B5	B5	MGTHTXN2_230
MGT_D_RX_11_P	X3.B16	A4	MGTHRXP3_230
MGT_D_RX_11_N	X3.B18	A3	MGTHRXN3_230
MGT_D_TX_11_P	X3.B4	A8	MGTHTXP3_230
MGT_D_TX_11_N	X3.B6	A7	MGTHTXN3_230
			Bank 130
MGT_D_RX_12_P	X3.B22	E31	MGTHRXP0_130
MGT_D_RX_12_N	X3.B24	E32	MGTHRXN0_130
MGT_D_TX_12_P	X3.B34	F29	MGTHTXP0_130
MGT_D_TX_12_N	X3.B36	F30	MGTHTXN0_130
MGT_D_RX_13_P	X3.B27	D33	MGTHRXP1_130
MGT_D_RX_13_N	X3.B29	D34	MGTHRXN1_130
MGT_D_TX_13_P	X3.B39	D29	MGTHTXP1_130

MGT_D_TX_13_N	X3.B41	D30	MGTHTXN1_130
MGT_D_RX_14_P	X3.B287	C31	MGTHRXP2_130
MGT_D_RX_14_N	X3.B30	C32	MGTHRXN2_130
MGT_D_TX_14_P	X3.B40	B29	MGTHTXP2_130
MGT_D_TX_14_N	X3.B42	B30	MGTHTXN2_130
MGT_D_RX_15_P	X3.B33	B33	MGTHRXP3_130
MGT_D_RX_15_N	X3.B35	B34	MGTHRXN3_130
MGT_D_TX_15_P	X3.B45	A31	MGTHTXP3_130
MGT_D_TX_15_N	X3.B47	A32	MGTHTXN3_130

Table 5.18: PL Transceiver connections

Important: *The transmitter lines are AC coupled with a 100nF capacitors. You have to take care that the carrier board implements a coupling capacitor on the transmitter side of the return signal. The signals are routed differentially with a controlled impedance of 100 Ohm.*

5.5 Miscellaneous resources

5.5.1 Clocking resources

The Miami MPSOC Plus SOM integrates various programmable clock sources:

Clock signal name	Comp pin	FPGA pin	SOM pin	Comp pin name	Description
PS_CLOCK_33MHZ	--	U24	--	PS_REF_CLK	33.333 MHz, 20 ppm
REFCLK_0_P	U30.63	--	X2.B4	IN0+	Programmable clock input (+)
REFCLK_0_N	U30.64	--	X32.B6	IN0-	Programmable clock input (-)
REFCLK_1_P	U30.1	--	X3.C1	IN1+	Programmable clock input (+)
REFCLK_1_N	U30.2	--	X3.C3	IN1-	Programmable clock input (-)
MGT_D_REFCLK_0_P	U30.24	L8	--	OUT0+	MGT Bank 228 Clock 0 (+)
MGT_D_REFCLK_0_N	U30.23	L7	--	OUT0-	MGT Bank 228 Clock 0 (-)
MGT_D_REFCLK_1_P	--	J8	X3.A27	--	MGT Bank 228 Clock 1 (+)
MGT_D_REFCLK_1_N	--	J7	X3.A29	--	MGT Bank 228 Clock 1 (-)
MGT_D_REFCLK_2_P	U30.28	G8	--	OUT1+	MGT Bank 229 Clock 0 (+)
MGT_D_REFCLK_2_N	U30.27	G7	--	OUT1-	MGT Bank 229 Clock 0 (-)
MGT_D_REFCLK_3_P	--	E8	X3.A52	--	MGT Bank 229 Clock 1 (+)
MGT_D_REFCLK_3_N	--	E7	X3.A54	--	MGT Bank 229 Clock 1 (-)
MGT_D_REFCLK_4_P	U30.45	C8	--	OUT6+	MGT Bank 230 Clock 0 (+)
MGT_D_REFCLK_4_N	U30.44	C7	--	OUT6-	MGT Bank 230 Clock 0 (-)
MGT_D_REFCLK_5_P	--	B10	X3.B21	--	MGT Bank 230 Clock 1 (+)
MGT_D_REFCLK_5_N	--	B9	X3.B23	--	MGT Bank 230 Clock 1 (-)
MGT_D_REFCLK_6_P	U30.38	G27	--	OUT4+	MGT Bank 130 Clock 0 (+)
MGT_D_REFCLK_6_N	U30.37	G28	--	OUT4-	MGT Bank 130 Clock 0 (-)
MGT_D_REFCLK_7_P	--	E27	X3.B46	--	MGT Bank 130 Clock 21 (+)
MGT_D_REFCLK_7_N	--	E28	X3.B48	--	MGT Bank 130 Clock 21 (-)
PS_MGT_D_REFCLK_0_P	U30.35	AA27		OUT3+	PS MGT Clock 0 (+)
PS_MGT_D_REFCLK_0_N	U30.34	AA28		OUT3-	PS MGT Clock 0 (-)
PS_MGT_D_REFCLK_1_P	U30.31	W27		OUT2+	PS MGT Clock 1 (+)
PS_MGT_D_REFCLK_1_N	U30.30	W28		OUT2-	PS MGT Clock 1 (-)
PS_MGT_D_REFCLK_3_P	U30.54	U31		OUT8+	PS MGT Clock 3 (+)
PS_MGT_D_REFCLK_3_N	U30.53	U32		OUT8-	PS MGT Clock 3 (-)
Ext_PHY_CLK (ETH)	U39.2	--	X2.B21		External ETH Sync clock
Int_PHY_CLK (ETH)	U30.42 – U39.6	--			25 MHz ETH clock from Clock generator (U30)
ETH_PHY_CLK	U39.12 – U19.34				Ethernet Phy Clock in (Sync clock if needed)
ETH_125MHz_CLK_OUT	U19.9	H13			Ethernet sync clock to logic
CLOCK_FPGA0_P	U30.51	AE7			PL Clock 0 (+)
CLOCK_FPGA0_N	U30.50	AF7			PL Clock 0 (-)
CLOCK_FPGA1_P	U30.59	AL6			PL Clock 1 (+)
CLOCK_FPGA1_N	U30.58	AL5			PL Clock 1 (-)

Table 5.19: Clock mapping

Clock generator (U30) I2C Addess

I^2C address SI5345B (U30)	0x74

5.5.2 I2C connected support peripherals

Table 5.20 gives an overview of the first I2C bus on the Zynq MPSoC. This bus is used to control the I²C peripherals on the SOM itself and can be expanded with peripherals on the carrier board. Care must be taken that loading this I²C bus with other peripherals may affect the devices present on the SOM (e.g. length of the signal traces, unique addresses, additional termination. The second I²C bus is especially intended for user controlled chains on the carrier boards. However, the I²C controller is also accessible via the EMIO ports via the programmable logic pins. This allows the user to use the involved pins on the MIO for other purposes.

I2C bus signal name	SoM pin	FPGA pin	FPGA pin label
SCL_1 (SCL_1V8)	X1.A51	N21	PS_MIO28
SDA_1 (SDA_1V8)	X1.A53	K22	PS_MIO29
SCL_0 (IO_S_VCC4_5)	X1.A47	L22	PS_MIO34
SDA_0 (IO_S_VCC4_7)	X1.A49	P22	PS_MIO35

Table 5.20: SOM I2C bus connections

Reference Designator	Component	Description	I2C bus	I2C Address
U35	TMP101NA/3K	Temperature Sensor	Dedicated / I2C core in FPGA	0x1001010 (0x4A)
U7	PCA9554	IO Expander	I2C_1	0x010000 (0x20)
U27	M24C32	EEPROM	I2C_1	0x1010001 (0x51) and 0x1011001 (0x59)
U30	Si5345B	Clock Generator	I2C_1	0x1101000 (0x68)

Table 5.21: SOM I2C address map

The following diagram shows the implementation of the I2C nets

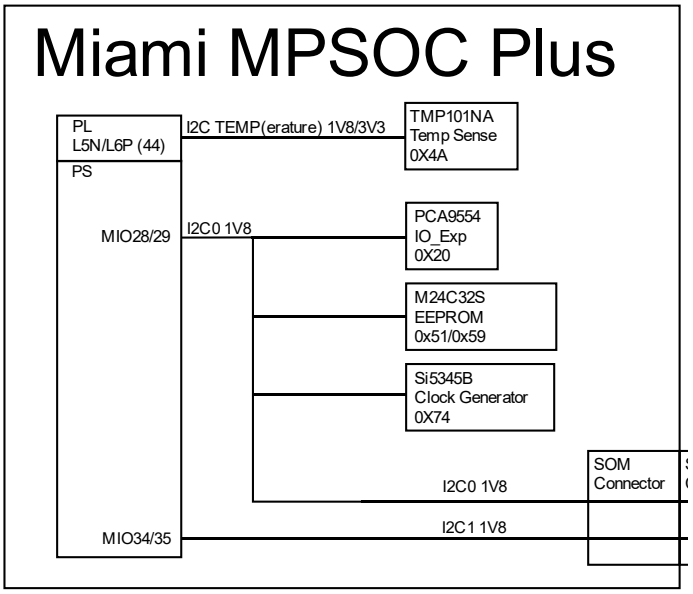


Figure 5.2: Miami MPSOC Plus SOM I2C mapping

5.5.3 Real Time Clock

The Miami SOM integrated Zynq MPSoC device incorporates a Real Time Clock that maintains the real time, even when the device is off. When the device is off, the RTC is switched to the battery power supply (Vbat). The RTC uses a 32.768 KHz 20 ppm crystal.

Refer to Xilinx document UG1085 (Zynq UltraScale+ MPSoC technical reference guide) chapter 7 for more details on the Real Time Clock.

5.5.4 Fan controller

The power dissipation of the board is dominated by the Xilinx MPSoC. However, other devices on the board also contributes to the power dissipation (power supplies, Ethernet PHY, etc.). In the case of an active cooling solution, a fan controller is needed. This can be implemented on the carrier board, utilizing PL or PS connected signals. The Miami MPSOC Plus implements circuitry to drive a fan and read back the tacho signal for speed control. Connector X4 (assembly option) allows for connecting a fan on top of the heatsink and implement a temperature-controlled control loop.

Signal name	FPGA pin	FPGA pin label	Description
FAN_PWM	AN12	IO_L3P_AD9P_44	PWM output to fan driver
FAN_TACHO	AP12	IO_L3N_AD9N_44	Tacho input for RPM measurement

Table 5.22: Fan controller mapping

6 Power supplies

For powering the Miami MPSOC Plus SOM a single 12Vdc power supply is recommended. A 9-16 Vdc power supply is acceptable. The maximum current drawn by the module depends upon:

- Type of the Zynq Ultrascale+ device (ZU6, ZU9 or ZU15)
- Speed grade qualification of the device and related operational frequencies
- Load, execution profile and clock speed of the FPGA logic
- Type of I/O interfaces in use (particularly the GTR/GTH transceivers)
- Powering of the I/O banks from the module or from an external source

6.1 Power supply rating

The maximum power rating of the module is dynamic, depending on the utilization and application of the board. The following power supplies are implemented on the board with their rated power limitations.

Description	Nominal supply	Tolerance or range	Current (A)	Max. power (W)
Input power supply	12 V	5 – 16 V	3.4 – 7.2 *)	55
Core supply	0.85	±1.5%	24	20.4
Generic 1.8V power rail	1.8	±1.5%	2.4	4.3
MGT termination power rail	1.2	±1.5%	2.4	2.9
Generic 3.3V power rail	3.3	±1.5%	2.4	7.9
MGT supply power rail	0.9	±1.5%	2.4	2.2
DDR supply	1.2	±1.5%	4.8	5.8
DDR reference voltage	1.2	±20 mV	-	-
DDR termination voltage	1.2	±4 mV	3.0	3.6
ADC I/O supply FPGA	1.8	±3 mV	0.15	0.3
ADC signal supply FPGA	1.25	±0.2%	0.15	0.2
Total supply capability				**47.8**
*) The 6 pins of the SOM connector, supplying the power to the SOM, have a maximum rated current of 1.2A per pin.				

Table 6.1: On-board power supply overview

Please refer to the relevant component data sheets for efficiency curves.

6.2 Power distribution connectors

The Miami MPSOC Plus SOM is powered from the carrier board using connector X3. All required supplies on the board are derived from this supply. The Samtec connectors have a conductive strip in the middle, acting as ground reference. Apart from this a number of signals on the connector are also connected to ground to achieve a controlled return path. In addition, the I/O bank voltage for banks 44, 47, 48 and 49 are exposed to the connector, although the I/O bank voltages can be supplied (default) by the SOM. This is a configuration item for the module. In the next tables, the available supply related voltages are summarized.

Carrier board connector X1			
Signal name	**Connector pin**	**Direction**	**Description**
Vbat	X1.A6	In	Battery back-up supply from carrier board
GND		Ref	Supply ground reference
GND		Ref	Supply ground reference
GND		Ref	Supply ground reference
+1V8	X1.A57	Out	Supply for logic level matching PS I/O bank 500 and 501 (recommended max .100mA)
+1V8	X1.A59	Out	Supply for logic level matching PS I/O bank 500 and 501 (recommended max .100mA)
+1V25A	X1.B39	Out	Analogue power supply for on-board XADC
AGND	X1.B41	Ref	Ground reference for on-board XADC
+VCC0	X1.B35	Out	3.3V logic supply for logic level matching FPGA I/O bank 10 (recommended max.100mA)
GND	X1 ground strip	Ref	Supply ground reference

Table 6.2: Connector X1 power supply terminals overview

Carrier board connector X2			
Signal name	**Connector pin**	**Direction**	**Description**
GND	X2.A17	Ref	Supply ground reference
GND	X2.A18	Ref	Supply ground reference
GND	X2.A55	Ref	Supply ground reference
GND	X2.A56	Ref	Supply ground reference
GND	X2.B1	Ref	Supply ground reference for GTH transceivers
GND	X2.B2	Ref	Supply ground reference for GTH transceivers
GND	X2.B7	Ref	Supply ground reference for GTH transceivers
GND	X2.B8	Ref	Supply ground reference for GTH transceivers
GND	X2.B13	Ref	Supply ground reference for GTH transceivers
GND	X2.B14	Ref	Supply ground reference for GTH transceivers
GND	X2.B19	Ref	Supply ground reference for GTH transceivers
GND	X2.B20	Ref	Supply ground reference for GTH transceivers
GND	X2.B25	Ref	Supply ground reference for GTH transceivers
GND	X2.B26	Ref	Supply ground reference for GTH transceivers
GND	X2 ground strip	Ref	Supply ground reference

Table 6.3: Connector 2 power supply terminals overview

Carrier board connector X3			
Signal name	**Connector pin**	**Direction**	**Description**
GND	X3.A1	Ref	Supply ground reference for GTH transceivers
GND	X3.A2	Ref	Supply ground reference for GTH transceivers
GND	X3.A7	Ref	Supply ground reference for GTH transceivers
GND	X3.A8	Ref	Supply ground reference for GTH transceivers
GND	X3.A13	Ref	Supply ground reference for GTH transceivers
GND	X3.A14	Ref	Supply ground reference for GTH transceivers
GND	X3.A19	Ref	Supply ground reference for GTH transceivers
GND	X3.A20	Ref	Supply ground reference for GTH transceivers
GND	X3.A25	Ref	Supply ground reference for GTH transceivers
GND	X3.A26	Ref	Supply ground reference for GTH transceivers
GND	X3.A31	Ref	Supply ground reference for GTH transceivers
GND	X3.A32	Ref	Supply ground reference for GTH transceivers
GND	X3.A37	Ref	Supply ground reference for GTH transceivers
GND	X3.A38	Ref	Supply ground reference for GTH transceivers
GND	X3.A43	Ref	Supply ground reference for GTH transceivers
GND	X3.A44	Ref	Supply ground reference for GTH transceivers
GND	X3.A49	Ref	Supply ground reference for GTH transceivers
GND	X3.A50	Ref	Supply ground reference for GTH transceivers
GND	X3.A55	Ref	Supply ground reference for GTH transceivers
GND	X3.A56	Ref	Supply ground reference for GTH transceivers
GND	X3.B1	Ref	Supply ground reference for GTH transceivers
GND	X3.B2	Ref	Supply ground reference for GTH transceivers
GND	X3.B7	Ref	Supply ground reference for GTH transceivers
GND	X3.B8	Ref	Supply ground reference for GTH transceivers
GND	X3.B13	Ref	Supply ground reference for GTH transceivers
GND	X3.B14	Ref	Supply ground reference for GTH transceivers
GND	X3.B19	Ref	Supply ground reference for GTH transceivers
GND	X3.B20	Ref	Supply ground reference for GTH transceivers
GND	X3.B25	Ref	Supply ground reference for GTH transceivers
GND	X3.B26	Ref	Supply ground reference for GTH transceivers
GND	X3.B31	Ref	Supply ground reference for GTH transceivers
GND	X3.B32	Ref	Supply ground reference for GTH transceivers
GND	X3.B37	Ref	Supply ground reference for GTH transceivers
GND	X3.B38	Ref	Supply ground reference for GTH transceivers
GND	X3.B43	Ref	Supply ground reference for GTH transceivers
GND	X3.B44	Ref	Supply ground reference for GTH transceivers
GND	X3.B49	Ref	Supply ground reference for GTH transceivers
GND	X3.B50	Ref	Supply ground reference for GTH transceivers
GND	X3.C2	Ref	Supply ground reference
+VCC3	X3.C5	Out	1.8V logic supply for logic level matching FPGA I/O bank 12 (recommended max.100mA)
+12V	X3.C55	In	Supply input from carrier board (max. 1.2A per pin)
+12V	X3.C56	In	Supply input from carrier board (max. 1.2A per pin)
+12V	X3.C57	In	Supply input from carrier board (max. 1.2A per pin)
+12V	X3.C58	In	Supply input from carrier board (max. 1.2A per pin)
+12V	X3.C59	In	Supply input from carrier board (max. 1.2A per pin)
+12V	X3.C60	In	Supply input from carrier board (max. 1.2A per pin)
GND	X3 ground strip	Ref	Supply ground reference

Table 6.4: Connector 3 power supply terminals overview

6.2.1 Battery backup supply

The FPGA facilitates a battery-backup supply pin for holding specific functions (real-time clock, AES encryption key) active during power-down of the device. By supplying this pin, the functionality behind this is guaranteed. *Refer to Xilinx user guide for more information on this functionality.*

6.2.2 I/O reference supplies

As denoted in **Table 6.1** several supplies are derived on the Miami SOM to supply different power rails. The I/O banks of the FPGA can be powered using different sources.

- The MIO pins of the processor are always powered at 1.8V
- The HD I/O bank pins of the FPGA can be selectively powered by 1.8V, 3.3V or supplied by the carrier board. This is an assembly option, executed by the customer or on request by Topic. Default is 3.3V.

Supply name	I/O bank reference	Voltages
+1V8	500, 501, 502, 503	1.8V only
+1V25A	503	1.25V only
VCC0	44, 47, 48	1.8V, 3.3V (default), carrier board supplied (HD bank) - R149 assembled and R342 not assembled → 3.3V - R342 assembled and R149 not assembled → 1.8V - R149 and R342 not assembled → carrier board supplied
VCC3	49	1.8V, 3.3V (default), carrier board supplied (HD bank) - R152 assembled and R154 not assembled → 3.3V - R152 not assembled and R154 assembled → 1.8V - R152 and R154 not assembled → carrier board supplied

Table 6.5: I/O power configuration

To facilitate proper level conversion or limited logic supply loading, the supply of each I/O bank is made available. It is recommended not to exceed 100mA loading per supply pin presented on the connector.

6.2.3 Analogue supply

The +1.25A analogue supply is provided as reference for the FPGA integrated XADC. It is not intended for supplying devices with relative high loads.

6.2.4 Configuration of the IO bank voltage

Table 6.5 gives an overview of the I/O voltage configuration options for the FPGA I/O banks. **Error! Reference source not found.** indicates where to locate the referenced resistors to configure the voltages. This is a soldering option, to be executed on request by Topic or the customer self. Use for configuration purposes only 0603 SMT resistors of 0 Ohm. Other values will lead to a voltage drop of the voltage on the banks.

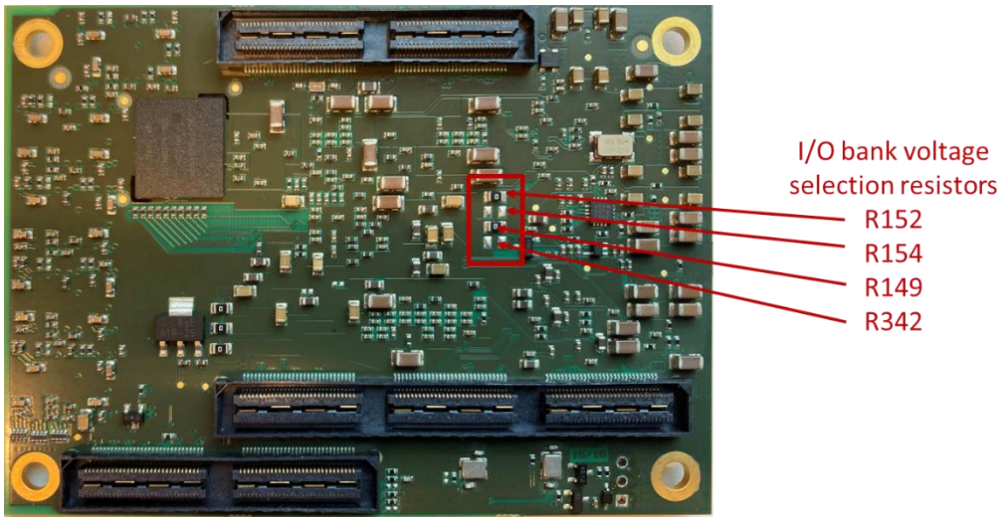


Figure 6.1: I/O power configuration resistor location (bottom view)

7 SOM connector pinout

7.1 X1: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm

PIN	Name	FPGA pin	PIN	Name	FPGA pin
A1	Reserved		A2	Reserved	
A3	Reserved		A4	Reserved	
A5	IO_D_VCC1_21_N	AK12	A6	VBAT	
A7	IO_D_VCC1_21_P	AJ12	A8	BOOT_EXT_0	
A9	IO_D_VCC1_22_N	AK1	A10	SOM_RST_N	
A11	IO_D_VCC1_22_P	AL1	A12	IO_D_AD_VCC1_0_P	AN8
A13	IO_D_CC_VCC1_23_N	AM5	A14	IO_D_AD_VCC1_0_N	AP8
A15	IO_D_CC_VCC1_23_P	AM6	A16	O_D_VCC1_16_P	AN9
A17	IO_D_AD_VCC1_11_N	AP4	A18	IO_D_VCC1_16_N	AP9
A19	IO_D_AD_VCC1_11_P	AP5	A20	IO_D_AD_CC_VCC1_1_P	AN6
A21	IO_D_AD_VCC1_12_N	AP3	A22	IO_D_AD_CC_VCC1_1_N	AP6
A23	IO_D_AD_VCC1_12_P	AN3	A24	IO_D_CC_VCC1_17_N	AL7
A25	IO_D_AD_VCC1_13_N	AN1	A26	IO_D_CC_VCC1_17_P	AL8
A27	IO_D_AD_VCC1_13_P	AM1	A28	IO_D_CC_VCC1_18_N	AK7
A29	IO_D_AD_VCC1_14_N	AL2	A30	IO_D_CC_VCC1_18_P	AK8
A31	IO_D_AD_VCC1_14_P	AL3	A32	IO_D_AD_VCC1_2_N	AK4
A33	IO_D_AD_VCC1_15_P	AK3	A34	IO_D_AD_VCC1_2_P	AK5
A35	IO_D_AD_VCC1_15_N	AK2	A36	IO_D_AD_VCC1_3_N	AP2
A37	BOOT_EXT_1		A38	IO_D_AD_VCC1_3_P	AN2
A39	IO_S_VCC4_0	K24	A40	IO_D_AD_VCC1_4_N	AN4
A41	IO_S_VCC4_1	L23	A42	IO_D_AD_VCC1_4_P	AM4
A43	IO_S_VCC4_2	M24	A44	JTAG_VREF	
A45	IO_S_VCC4_3	J24	A46	IO_S_VCC4_4	M25
A47	IO_S_VCC4_5	L22	A48	IO_S_VCC4_6	N25
A49	IO_S_VCC4_7	P22	A50	IO_S_VCC4_8	L25
A51	SCL_1V8	N21	A52	IO_S_VCC4_9	K25
A53	SDA_1V8	K22	A54	IO_S_VCC4_10	P25
A55	BOOT_EXT_2		A56	IO_S_VCC4_11	P24
A57	+1V8		A58	IO_S_VCC4_12	J25
A59	+1V8		A60	IO_S_VCC4_13	N24

PIN	Name	FPGA pin	PIN	Name	FPGA pin
B1	IO_S_VCC4_14	J22	B2	IO_D_VCC2_18_P	AH1
B3	IO_S_VCC4_15	L21	B4	IO_D_VCC2_18_N	AJ1
B5	SOM_SW_RST_N		B6	IO_D_VCC2_19_P	AF2
B7	MDIP0		B8	IO_D_VCC2_19_N	AF1
B9	MDIN0		B10	IO_D_VCC2_20_P	AE2
B11	MDIN1		B12	IO_D_VCC2_20_N	AE1
B13	MDIP1		B14	IO_D_VCC2_21_P	AD2
B15	MDIP2		B16	IO_D_VCC2_21_N	AD1
B17	MDIN2		B18	IO_D_VCC2_22_P	AH7
B19	MDIP3		B20	IO_D_VCC2_22_N	AH6
B21	MDIN3		B22	IO_S_VCC1_0	AM3
B23	LED0		B24	IO_S_VCC1_1	AP1
B25	LED1		B26	IO_S_VCC1_2	AN11
B27	LED2		B28	IO_S_VCC1_3	AJ7
B29	IO_S_VCC4_16	H23	B30	IO_S_VCC2_0	AG1
B31	IO_S_VCC4_17	H22	B32	IO_S_VCC2_1	AH9
B33	IO_S_VCC4_18	N23	B34	IO_S_VCC2_2	AD5
B35	VCC_0		B36	IO_S_VCC2_3	AD9
B37	IO_S_VCC4_21	N22	B38	IO_D_VCC5_0_P	T7
B39	+1V25A		B40	IO_D_VCC5_0_N	T6
B41	AGND		B42	IO_D_VCC5_1_P	W12
B43	XADC_VP	U18	B44	IO_D_VCC5_1_N	W11
B45	XADC_VN	V17	B46	IO_D_VCC5_2_N	V11
B47	XADC_DXP	W18	B48	IO_D_VCC5_2_P	V12
B49	XADC_DXN	W17	B50	IO_D_VCC5_3_P	U9
B51	PL_JTAG_RSTN		B52	IO_D_VCC5_3_N	U8
B53	PL_JTAG_TDI	U25	B54	IO_D_VCC5_4_N	U6
B55	PL_JTAG_TMS	R24	B56	IO_D_VCC5_4_P	V6
B57	PL_JTAG_TCK	R25	B58	IO_D_VCC5_5_N	V7
B59	PL_JTAG_TDO	T25	B60	IO_D_VCC5_5_P	V8

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

7.2 X2: Carrier board connector pinning

Part type	Samtec, QSH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-060-01-L-D-A, High Speed ground plane socket, 120 pins (2x60), stacking height 5mm

PIN	Name	FPGA pin	PIN	Name	FPGA pin
A1	IO_D_AD_VCC1_5_N	AM11	A2	IO_D_AD_VCC1_6_P	AM9
A3	IO_D_AD_VCC1_5_P	AL11	A4	IO_D_AD_VCC1_6_N	AM8
A5	IO_D_AD_VCC1_7_P	AN7	A6	IO_D_VCC5_6_P	U10
A7	IO_D_AD_VCC1_7_N	AP7	A8	IO_D_VCC5_6_N	T10
A9	IO_D_AD_VCC1_8_N	AK10	A10	IO_D_AD_VCC1_9_P	AL10
A11	IO_D_AD_VCC1_8_P	AJ10	A12	IO_D_AD_VCC1_9_N	AM10
A13	IO_D_VCC1_20_P	AJ9	A14	IO_D_AD_VCC1_10_N	AP10
A15	IO_D_VCC1_20_N	AK9	A16	IO_D_AD_VCC1_10_P	AP11
A17	GND		A18	GND	
A19	IO_D_VCC2_0_P	AH5	A20	IO_D_VCC2_1_P	AH12
A21	IO_D_VCC2_0_N	AJ4	A22	IO_D_VCC2_1_N	AH11
A23	IO_D_VCC2_2_P	AG10	A24	IO_D_VCC2_3_P	AE12
A25	IO_D_VCC2_2_N	AG9	A26	IO_D_VCC2_3_N	AF12
A27	IO_D_CC_VCC2_4_P	AJ6	A28	IO_D_VCC2_5_P	AH2
A29	IO_D_CC_VCC2_4_N	AJ5	A30	IO_D_VCC2_5_N	AJ2
A31	IO_D_VCC2_6_P	AG8	A32	IO_D_VCC2_7_P	AG3
A33	IO_D_VCC2_6_N	AH8	A34	IO_D_VCC2_7_N	AH3
A35	IO_D_VCC2_8_P	AD10	A36	IO_D_VCC2_9_P	AE3
A37	IO_D_VCC2_8_N	AE9	A38	IO_D_VCC2_9_N	AF3
A39	IO_D_VCC2_10_P	AE8	A40	IO_D_VCC2_11_P	AF11
A41	IO_D_VCC2_10_N	AF8	A42	IO_D_VCC2_11_N	AG11
A43	IO_D_VCC2_12_P	AE10	A44	IO_D_CC_VCC2_13_P	AF6
A45	IO_D_VCC2_12_N	AF10	A46	IO_D_CC_VCC2_13_N	AG6
A47	IO_D_VCC2_14_P	AD7	A48	IO_D_VCC2_15_P	AG5
A49	IO_D_VCC2_14_N	AD6	A50	IO_D_VCC2_15_N	AG4
A51	IO_D_VCC2_16_P	AD4	A52	IO_D_CC_VCC2_17_P	AE5
A53	IO_D_VCC2_16_N	AE4	A54	IO_D_CC_VCC2_17_N	AF5
A55	GND		A56	GND	
A57	IO_D_VCC0_0_P	L18	A58	IO_D_VCC0_1_P	L17
A59	IO_D_VCC0_0_N	K18	A60	IO_D_VCC0_1_N	K17

PIN	Name	FPGA pin	PIN	Name	FPGA pin
B1	GND		B2	GND	
B3	PS_MGT_D_TX_1_P	Y29	B4	REFCLK_0_P	
B5	PS_MGT_D_TX_1_N	Y30	B6	REFCLK_0_N	
B7	GND		B8	GND	
B9	PS_MGT_D_TX_3_P	V29	B10	PS_MGT_D_RX_3_P	V33
B11	PS_MGT_D_TX_3_N	V30	B12	PS_MGT_D_RX_3_N	V34
B13	GND		B14	GND	
B15	PS_MGT_D_TX_0_P	AB29	B16	PS_MGT_D_RX_0_P	AB33
B17	PS_MGT_D_TX_0_N	AB30	B18	PS_MGT_D_RX_0_N	AB34
B19	GND		B20	GND	
B21	EXT_PHY_CLK		B22	PS_MGT_D_RX_1_P	AA31
B23	n.c.		B24	PS_MGT_D_RX_1_N	AA32
B25	GND		B26	GND	
B27	IO_D_VCC5_7_P	T13	B28	IO_D_VCC5_8_P	U11
B29	IO_D_VCC5_7_N	R13	B30	IO_D_VCC5_8_N	T11
B31	IO_S_VCC4_19	M23	B32	IO_S_VCC4_20	K23
B33	IO_D_VCC0_2_P	G18	B34	IO_D_VCC0_3_P	J17
B35	IO_D_VCC0_2_N	G19	B36	IO_D_VCC0_3_N	H17
B37	IO_D_CC_VCC0_4_P	G21	B38	IO_D_VCC0_5_P	H18
B39	IO_D_CC_VCC0_4_N	F21	B40	IO_D_VCC0_5_N	H19
B41	IO_D_CC_VCC0_6_P	G20	B42	IO_D_VCC0_7_P	C21
B43	IO_D_CC_VCC0_6_N	F20	B44	IO_D_VCC0_7_N	B21
B45	IO_D_VCC0_8_P	E22	B46	IO_D_VCC0_9_P	C18
B47	IO_D_VCC0_8_N	D22	B48	IO_D_VCC0_9_N	C19
B49	IO_D_CC_VCC0_10_P	F17	B50	IO_D_VCC0_11_P	D17
B51	IO_D_CC_VCC0_10_N	F18	B52	IO_D_VCC0_11_N	C17
B53	IO_D_VCC0_12_P	E17	B54	IO_D_VCC0_13_P	A17
B55	IO_D_VCC0_12_N	E18	B56	IO_D_VCC0_13_N	A18
B57	IO_D_CC_VCC0_14_P	E19	B58	IO_D_VCC0_15_P	B18
B59	IO_D_CC_VCC0_14_N	D19	B60	IO_D_VCC0_15_N	B19

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

7.3 X3: Carrier board connector pinning

Part type (SOM)	Samtec, QSH-090-01-L-D-A, High Speed ground plane socket, 180 pins (3x60), stacking height 5mm
Mating part type (carrier board)	Samtec, QTH-090-01-L-D-A, High Speed ground plane socket, 180 pins (3x60), stacking height 5mm

PIN	Name	FPGA pin	PIN	Name	FPGA pin
A1	GND		A2	GND	
A3	MGT_D_RX_0_P	T2	A4	MGT_D_RX_1_P	P2
A5	MGT_D_RX_0_N	T1	A6	MGT_D_RX_1_N	P1
A7	GND		A8	GND	
A9	MGT_D_RX_2_P	M2	A10	MGT_D_RX_3_P	L4
A11	MGT_D_RX_2_N	M1	A12	MGT_D_RX_3_N	L3
A13	GND		A14	GND	
A15	MGT_D_TX_0_P	R4	A16	MGT_D_TX_1_P	P6
A17	MGT_D_TX_0_N	R3	A18	MGT_D_TX_1_N	P5
A19	GND		A20	GND	
A21	MGT_D_TX_2_P	N4	A22	MGT_D_TX_3_P	M6
A23	MGT_D_TX_2_N	N3	A24	MGT_D_TX_3_N	M5
A25	GND		A26	GND	
A27	MGT_D_REFCLK_1_P	J8	A28	MGT_D_RX_4_P	K2
A29	MGT_D_REFCLK_1_N	J7	A30	MGT_D_RX_4_N	K1
A31	GND		A32	GND	
A33	MGT_D_RX_5_P	J4	A34	MGT_D_RX_6_P	H2
A35	MGT_D_RX_5_N	J3	A36	MGT_D_RX_6_N	H1
A37	GND		A38	GND	
A39	MGT_D_RX_7_P	F2	A40	MGT_D_TX_4_P	K6
A41	MGT_D_RX_7_N	F1	A42	MGT_D_TX_4_N	K5
A43	GND		A44	GND	
A45	MGT_D_TX_5_P	H6	A46	MGT_D_TX_6_P	G4
A47	MGT_D_TX_5_N	H5	A48	MGT_D_TX_6_N	G3
A49	GND		A50	GND	
A51	MGT_D_TX_7_P	F6	A52	MGT_D_REFCLK_3_P	E8
A53	MGT_D_TX_7_N	F5	A54	MGT_D_REFCLK_3_N	E7
A55	GND		A56	GND	
A57	MGT_D_TX_8_P	E4	A58	MGT_D_TX_9_P	D6
A59	MGT_D_TX_8_N	E3	A60	MGT_D_TX_9_N	D5

PIN	Name	FPGA pin	PIN	Name	FPGA pin
B1	GND		B2	GND	
B3	MGT_D_TX_10_P	B6	B4	MGT_D_TX_11_P	A8
B5	MGT_D_TX_10_N	B5	B6	MGT_D_TX_11_N	A7
B7	GND		B8	GND	
B9	MGT_D_RX_8_P	D2	B10	MGT_D_RX_9_P	C4
B11	MGT_D_RX_8_N	D1	B12	MGT_D_RX_9_N	C3
B13	GND		B14	GND	
B15	MGT_D_RX_10_P	B2	B16	MGT_D_RX_11_P	A4
B17	MGT_D_RX_10_N	B1	B18	MGT_D_RX_11_N	A3
B19	GND		B20	GND	
B21	MGT_D_REFCLK_5_P	B10	B22	MGT_D_RX_12_P	E31
B23	MGT_D_REFCLK_5_N	B9	B24	MGT_D_RX_12_N	E32
B25	GND		B26	GND	
B27	MGT_D_RX_13_P	D33	B28	MGT_D_RX_14_P	C31
B29	MGT_D_RX_13_N	D34	B30	MGT_D_RX_14_N	C32
B31	GND		B32	GND	
B33	MGT_D_RX_15_P	B33	B34	MGT_D_TX_12_P	F29
B35	MGT_D_RX_15_N	B34	B36	MGT_D_TX_12_N	F30
B37	GND		B38	GND	
B39	MGT_D_TX_13_P	D29	B40	MGT_D_TX_14_P	B29
B41	MGT_D_TX_13_N	D30	B42	MGT_D_TX_14_N	B30
B43	GND		B44	GND	
B45	MGT_D_TX_15_P	B30	B46	MGT_D_REFCLK_7_P	E27
B47	MGT_D_TX_15_N	B31	B48	MGT_D_REFCLK_7_N	E28
B49	GND		B50	GND	
B51	USB0_OTG_DP		B52	USB1_OTG_DP	
B53	USB0_OTG_DM		B54	USB1_OTG_DM	
B55	USB0_ID		B56	USB1_ID	
B57	USB0_5V		B58	USB1_5V	
B59	GND		B60	GND	

PIN	Name	FPGA pin	PIN	Name	FPGA pin
C1	REFCLK_1_P		C2	GND	
C3	REFCLK_1_N		C4	IO_S_VCC5_1	P10
C5	VCC3		C6	IO_S_VCC5_0	P9
C7	IO_D_CC_VCC5_9_P	N9	C8	IO_D_CC_VCC5_10_P	T12
C9	IO_D_CC_VCC5_9_N	N8	C10	IO_D_CC_VCC5_10_N	R12
C11	IO_D_CC_VCC5_11_P	R10	C12	IO_D_CC_VCC5_12_P	N13
C13	IO_D_CC_VCC5_11_N	R9	C14	IO_D_CC_VCC5_12_N	M13
C15	IO_D_VCC5_13_P	M10	C16	IO_D_VCC5_14_P	M11
C17	IO_D_VCC5_13_N	L10	C18	IO_D_VCC5_14_N	L11
C19	IO_D_VCC5_15_P	T8	C20	IO_D_VCC5_16_P	M15
C21	IO_D_VCC5_15_N	R8	C22	IO_D_VCC5_16_N	M14
C23	IO_D_VCC5_17_P	P12	C24	IO_D_VCC5_18_P	P11
C25	IO_D_VCC5_17_N	N12	C26	IO_D_VCC5_18_N	N11
C27	IO_D_VCC5_19_P	L12	C28	IO_D_VCC5_20_P	L16
C29	IO_D_VCC5_19_N	K12	C30	IO_D_VCC5_20_N	K16
C31	IO_D_CC_VCC3_12_P	E14	C32	IO_D_CC_VCC3_13_P	C14
C33	IO_D_CC_VCC3_12_N	D14	C34	IO_D_CC_VCC3_13_N	B14
C35	IO_D_CC_VCC3_14_P	C13	C36	IO_D_CC_VCC3_15_P	E15
C37	IO_D_CC_VCC3_14_N	B13	C38	IO_D_CC_VCC3_15_N	D15
C39	IO_D_VCC3_16_P	B16	C40	IO_D_VCC5_21_P	L13
C41	IO_D_VCC3_16_N	A16	C42	IO_D_VCC5_21_N	K13
C43	IO_S_VCC5_2	K10	C44	IO_D_VCC3_19_P	L12
C45	IO_S_VCC5_3	K14	C46	IO_D_VCC3_19_N	K12
C47	IO_D_VCC3_20_P	C12	C48	IO_S_VCC5_4	W10
C49	IO_D_VCC3_20_N	B12	C50	IO_S_VCC5_5	V9
C51	IO_D_VCC3_22_P	A13	C52	IO_D_VCC5_22_P	L15
C53	IO_D_VCC3_22_N	A12	C54	IO_D_VCC5_22_N	K15
C55	V_IN		C56	V_IN	
C57	V_IN		C58	V_IN	
C59	V_IN		C60	V_IN	

Remark: Ground reference is available on the integrated ground socket as reference to any pin on the connector.

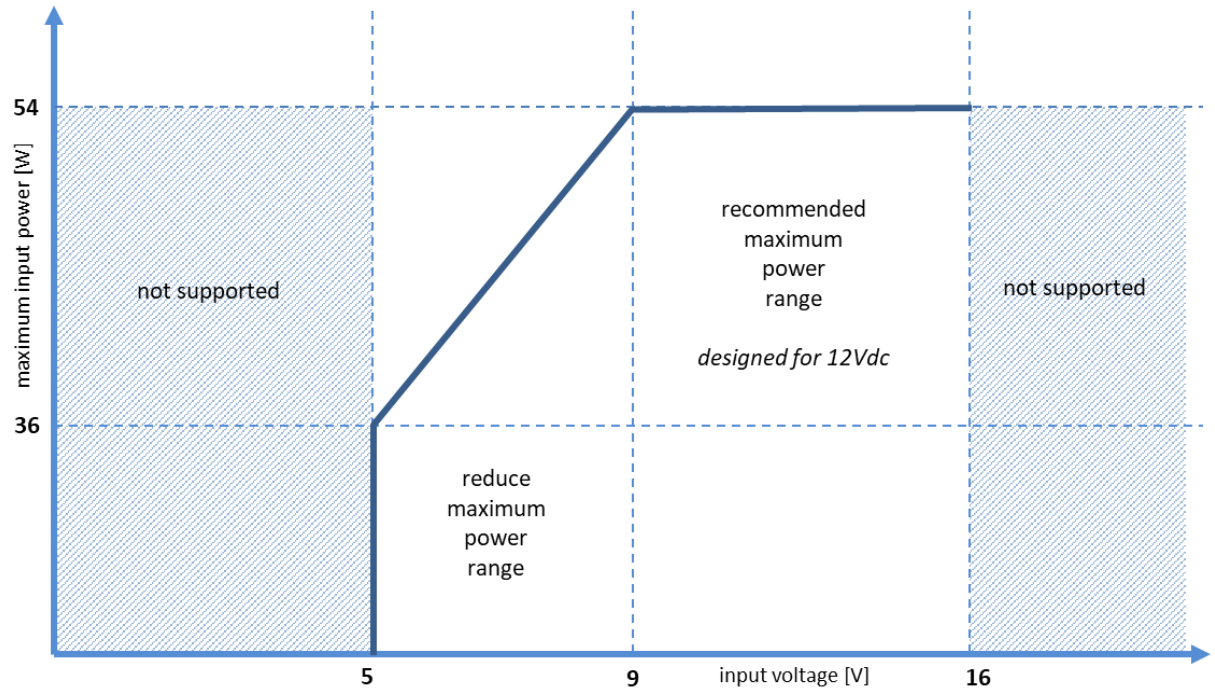
8 Electrical characteristics

8.1 Electrical specifications

Supply voltage	5.0 – 16.0 Vdc *)
Power consumption	55 W (maximum) **)
Load step	5 W (minimum) ***)

*) *Power is supplied to the module using 6 pins of the SOM connector. The maximum current rating of the connector pins as well as the related PCB power traces limit the currents flowing to the SOM. At lower voltages, higher currents are required to deliver the same power. The SOM power train is designed to provide maximum 55[W], including efficiency losses by the on-board power supplies. For reliable operation, the following supply profile is recommended.*

$$MaxPower(W) = 4.5 \times InputVoltage(V) + 13.5 \rightarrow \ where\ InputVoltage: [5,9]V$$



**) *Power consumption is dominated by the use of the FPGA fabric of the Zynq Ultrascale+ SOC. For an accurate estimation of the power consumption, use the Xilinx Power Estimator (XPE). The latest version can be downloaded via the Xilinx website.*

***) *The FPGA fabric of the Xilinx SOC is powered from the 0.85V core power supply rail. It is possible to program logic in the FPGA with a high dynamic current switching profile, exceeding the capabilities of the power supply. The minimum load step is guaranteed by design. This must be taken into account when programming FPGA logic. Excessive load steps may result in corrupted logic operation or invocation of a system reset.*

8.2 Environment specifications

Extended operating temperature	-40 … +85°C
Storage temperature	-51 … +90°C
Relative humidity	0 … 95%, non-condensing

8.3 Mechanical specifications

Weight	approximately 35 grams
Board	glass epoxy Megtron6, UL-listed, 16 layers, 1.80 mm thick
Dimensions	Length and width: 95.0 mm x 68.5 mm Bottom side component heigh : <=2.0 mm Top side component height: <=3.8 mm PCB thickness: 1.80 mm Default connector stacking height: 5 mm

8.4 Regulatory conformation

CE (EMC, EMI)	Tested according to EN 55032 and EN 55035. Report available on request
Temperature and humidity	Tested according to EN 60068. Report available on request.
Shock and vibration	Tested according to EN 60068. Report available on request.
Altitude compliance	TBD
RoHS / REACH	All applied components, printed circuit board material, production of the printed circuit board as well as the assembly of the boards are conducted in compliance with the RoHS and REACH legislation. A declaration of compliance is available on request.

8.5 Reliability

Failure rate calculation method	IEC 61709
Failure rate (FIT)	3198
MTBF	312.697 (hour), 35 (year)
Conditions	40°C ambient temperature, continuous operation (8760 hours per year), non-mobile operation, ground benign
Remark	Be aware that the failure rate calculation is a statistical method, built on experience figures. The specified failure rate is highly depending on the ambient temperature. As a rule of thumb: the MTBF is halved every 10°C ambient temperature increase. The maximum supported operational ambient temperature is 85°C. Topic does not warrant against board malfunction related to accelerated board aging as a result of increased ambient temperature conditions and/or insufficient heat management precautions leading to a shorter product life time. E.g.: at an ambient temperature of 85°C, the MTBF figure is only 1.6 years when operated continuously. Report available on request.
Warrantee	The Miami MPSOC Plus standard warrantee period is only applicable when operated in an ambient temperature of maximum 50°C. Please consult with Topic for details.

9 Ordering information

9.1 System-on-Module configuration

The Miami MPSOC Plus can be ordered in different configurations. These options are expressed in the order number.

Option	Values
Basic order number	**Miami MPSOC Plus**
FPGA type	6, **9**, 15
CPU cores	C, **G**
Speed grade	**1**, 2
Ethernet PHY	No, **Yes**
USB0 PHY0	No, **Yes**
USB1 PHY1	No, **Yes**
eMMC	0, 8, **16**, 32, 64 GByte
DDR4 width	32, 64, **72** bit
DDR4 capacity	2, **4**, 8 GByte
NOR	64, 128, **256**, 512 Mbyte
Boot mode switches	No, **Yes**
Fan connector	No, **Yes**

Bold items indicate the default configuration

9.2 Heatsink recommendation

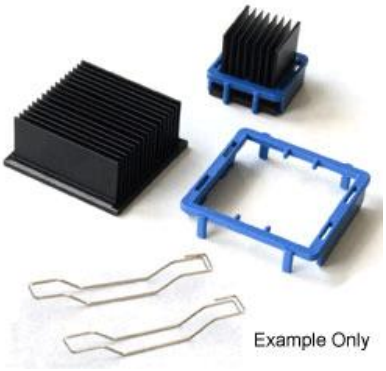
The Miami MPSOC Plus power consumption is dominated by the Zynq Ultrascale+ MPSoC. However, there are other heat sources that need consideration:

- Power supplies
- PHY devices (Ethernet)
- DDR4 memory devices

9.2.1 Standard thermal Xilinx Ultrascale Plus solution

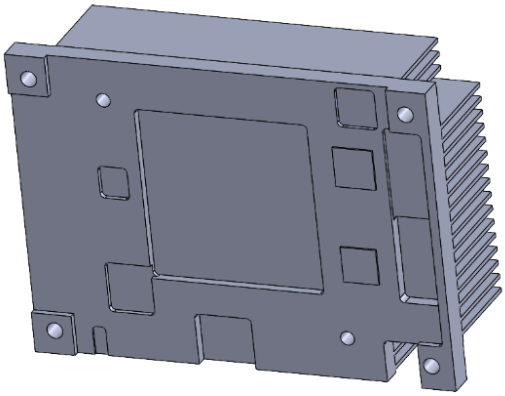
When operating the Miami MPSOC Plus in a stand-alone configuration during development, evaluation or prototyping with an ambient temperature limited to 35°C, Topic recommends to apply the following heatsink for the Xilinx Ultrascale+:

- AAVID EA-350-H245-T710. Passive cooling only.
- Add-on cooling fan 35mm diameter, 12 Vdc with tacho readback.



It is recommended to apply a form of forced airflow over the heatsink. The Zynq Ultrascale+ devices are protected against overheating past the maximum junction temperature, when this feature is enabled. The Topic Linux distribution enables this (by default disabled) function.

9.2.2 Custom thermal board solution



Topic highly recommends applying the (optional) specially designed heatsink for the Miami MPSOC Plus. This will not only sink heat from the Xilinx SOC, but also from the power supplies, Ethernet and USB PHYs as well as the clocking source. It is designed for a nominal ambient temperature of 50°C, operate at full load of 50W and stay safely below the junction temperature limits of all board components.

Please inquire for the heatsink design document for all thermal design details. Ordering information from Topic:

- miap-zu-50w (50W Miami MPSOC Plus heatsink)