

MXXEVP Hardware Manual

Version: 1.0

Created on: May 19, 2022

Created by: Diana Korchmar

© ARIES Embedded GmbH. The information contained in this document is strictly confidential. This document may not be copied, reproduced, translated, changed or distributed without the written approval of ARIES Embedded GmbH

CONTENTS:

1	About this manual	4
1.1	Imprint	4
1.2	Disclaimer	4
1.3	Copyright	5
1.4	Registered Trademarks	5
1.5	Care and Maintenance	5
1.6	Change Log	5
2	Overview	6
2.1	Block Diagram	7
2.2	Feature Set	7
2.3	Dimensions	8
2.4	Handling Recommendations	9
3	Resources	10
3.1	Ethernet	10
3.1.1	HPS Gigabit Ethernet Phy 0 (U500)	10
3.1.2	HPS Gigabit Ethernet Phy 1 (U600)	11
3.2	Boot Select	11
3.3	IDT Clock-Buffer	11
3.3.1	Connector P9	11
3.3.2	DIP Switch S1	12
3.4	MicroSD card	13
3.5	JTAG	13
3.5.1	Connector P8	13
3.6	Reset Button	14
3.7	UART	14
3.8	CAN	14
3.8.1	CAN1 (P23)	15
3.8.2	CAN2 (P24)	15
3.9	USB-OTG	15
3.10	LCD Interface	16
3.10.1	LCD	16
3.11	Touch Controller	17
3.12	PMOD Module Connectors	17
3.12.1	Connector J4:	18
3.12.2	Connector J5:	18
3.12.3	Connector J6:	18
3.13	Pin Header	19
3.13.1	Connector P3	19

- 3.14 FMC connector 19
 - 3.14.1 Connector J2A: 20
 - 3.14.2 Connector J2B: 20
 - 3.14.3 Connector J2C: 21
 - 3.14.4 Connector J2D: 21
 - 3.14.5 Connector J2F: 22
 - 3.14.6 Connector J2G: 22
 - 3.14.7 Connector J2H: 23
 - 3.14.8 Connector J2J: 23
- 3.15 miniPCIe and PCIe 24
- 3.16 Samtec Connector 24
 - 3.16.1 Connector P1 24
 - 3.16.2 Connector P2 28

ABOUT THIS MANUAL

1.1 Imprint

Address:

ARIES Embedded GmbH
Schöngesinger Str. 84
D-82256 Fürstenfedbruck
Germany

Phone:

+49 (0) 8141/36 367-0

Fax:

+49 (0) 8141/36 367-67

1.2 Disclaimer

ARIES Embedded does not guarantee that the information in this document is up-to-date, correct, complete or of good quality. Liability claims against ARIES Embedded, referring to material or non-material related damages caused, due to usage or non-usage of the information given in this document, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of ARIES Embedded. ARIES Embedded explicitly reserves the rights to change or add to the contents of this Preliminary User's Manual or parts of it without notification.

1.3 Copyright

This document may not be copied, reproduced, translated, changed or distributed, completely or partially in any form without the written approval of ARIES Embedded GmbH.

1.4 Registered Trademarks

The contents of this document may be subject of intellectual property rights (including but not limited to copyright, trademark, or patent rights). Any such rights that are not expressly licensed or already owned by a third party are reserved by ARIES Embedded GmbH.

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

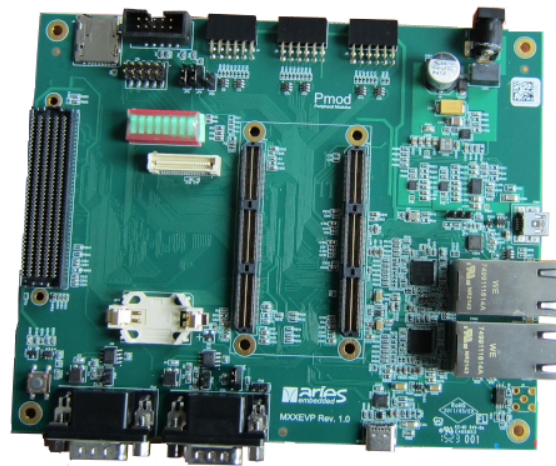
Revision	Date	Revised	Comment
1.0	11.11.2022	dk	Initial creation
1.1	13.09.2023	wa	Updated the new version features

CHAPTER

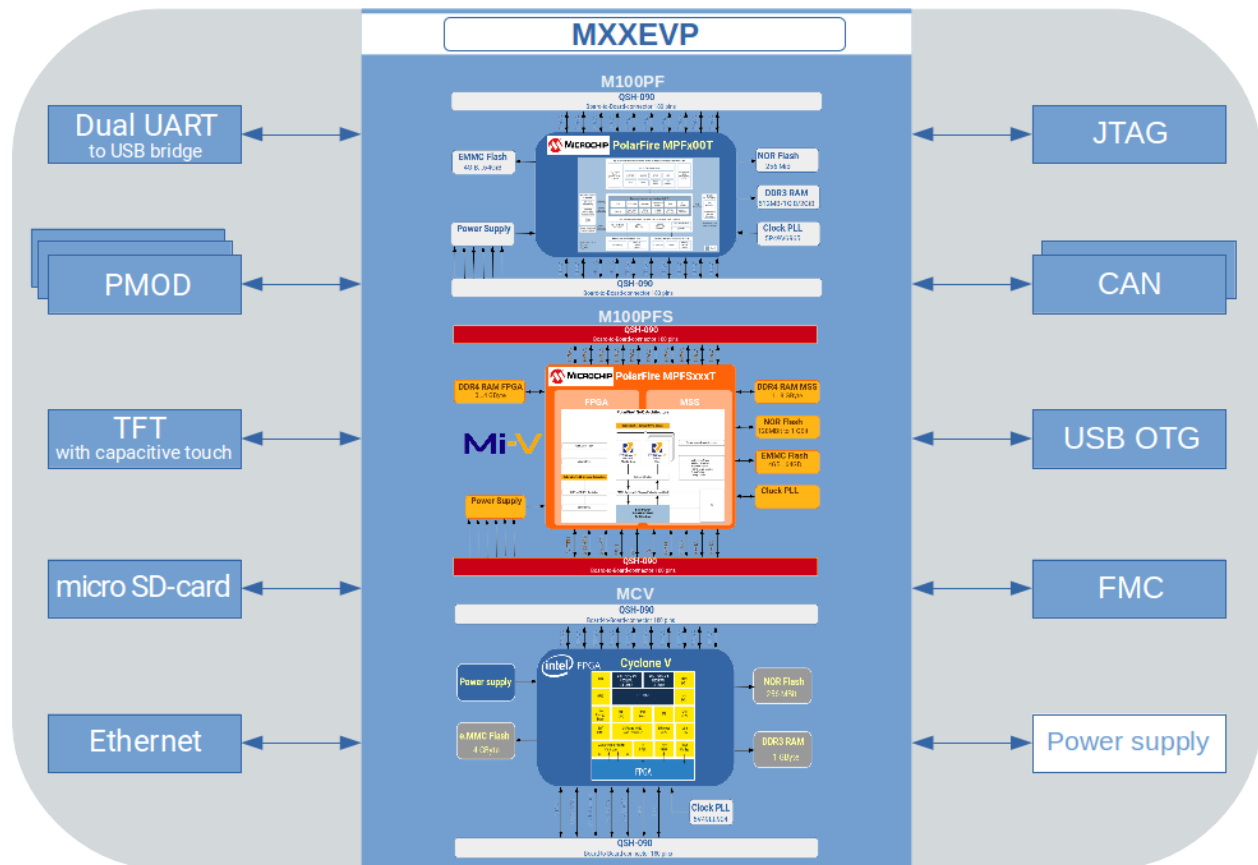
TWO

OVERVIEW

MXxEVP represents the flexible Evaluation Platform for working with the MCV, M100PF and M100PFS Systems-on-Module. The system helps developers to have a smooth start with the MCV, M100PF and M100PFS SoMs, it can be used for developing software as well as implementing prototypes.



2.1 Block Diagram

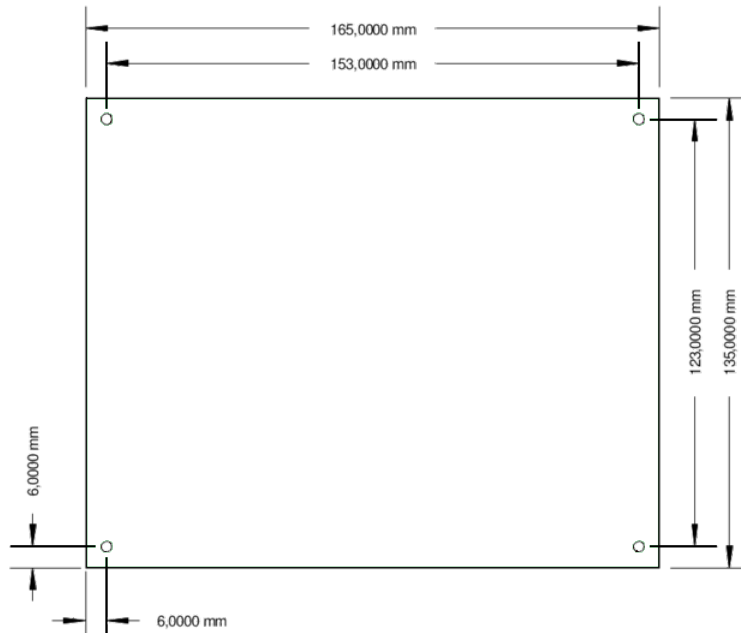


2.2 Feature Set

For supporting development projects and fast prototyping in the best possible way MXXEVP supplies

- 2x HPS Gigabit Ethernet on a RJ45 connector
- HPS USB on a mini-USB connector
- 2x UART on a CP2105 USB to dual UART Bridge
- 2x CAN on a DSUB-9 connector each
- TFT with Touch
- FMC extension connector
- 3x PMOD extension connectors
- microSD-card slot
- boot mode selection for FPGA-/eMMC-boot-mode
- JTAG pin header
- flexible supply voltage 7V to 36V DC

2.3 Dimensions



2.4 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating base-board connectors. To avoid mechanical damage to the components populated on SoM it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:

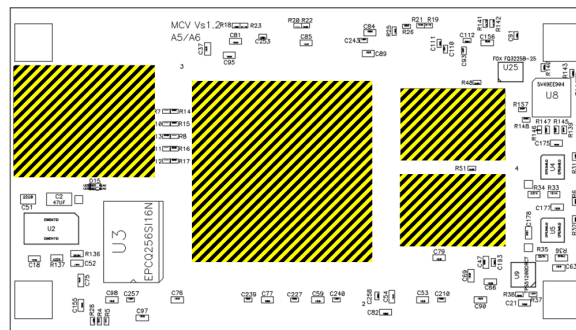


Fig. 1: MCV SoM Handling Recommendations

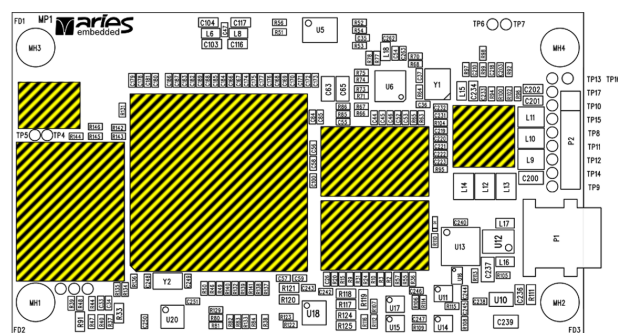


Fig. 2: M100PF SoM Handling Recommendations

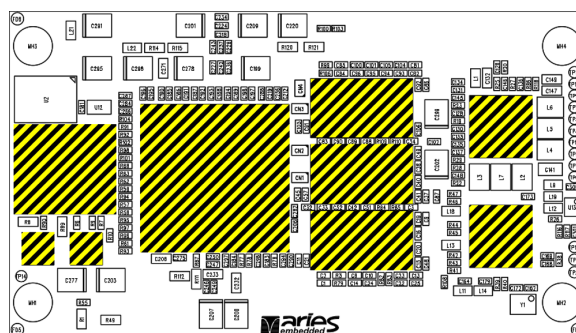


Fig. 3: M100PFS SoM Handling Recommendations

CHAPTER

THREE**RESOURCES****3.1 Ethernet**

MXXEVP offers the EMAC0 and EMAC1 Ethernet Ports in RGMII mode of the Cyclone V SoC-FPGA. These ports can be accessed via the RJ45 connectors P500 and P600 supported by Microchip KSZ9131RXN Ethernet physical-layer transceivers.

3.1.1 HPS Gigabit Ethernet Phy 0 (U500)

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
CLK25_PHY0	P2-174	CLKEXTE	–	CLK25_3	–	CLK25_O	–
RST_N	–	–	–	–	–	–	–
HPS_GPI3	P2-154	HPS_GPI3	R21	GPIO_G13	G13	MSS_IO34	B3
EMAC0_RX_CLK	P2-118	HPS_GPIO10	G4	ETH0_RXC	G14	ETH0_RXC	E15
EMAC0_RX_CTL	P2-117	HPS_GPIO8	F4	ETH0_RX_DV	E16	ETH0_RX_DV	B13
EMAC0_RXD0	P2-110	HPS_GPIO5	C8	ETH0_RXD0	G15	ETH0_RXD0	D22
EMAC0_RXD1	P2-116	HPS_GPIO11	C5	ETH0_RXD1	H15	ETH0_RXD1	C22
EMAC0_RXD2	P2-111	HPS_GPIO12	E5	ETH0_RXD2	D17	ETH0_RXD2	D14
EMAC0_RXD3	P2-109	HPS_GPIO13	D5	ETH0_RXD3	D16	ETH0_RXD3	D13
EMAC0_TX_CLK	P2-113	HPS_GPIO0	E4	ETH0_GTXCLK	B14	ETH0_GTXCLK	G17
EMAC0_TX_CTL	P2-114	HPS_GPIO9	C6	ETH0_TX_EN	C17	ETH0_TX_EN	A15
EMAC0_TXD0	P2-106	HPS_GPIO1	C10	ETH0_TXD0	C16	ETH0_TXD0	G14
EMAC0_TXD1	P2-107	HPS_GPIO2	F5	ETH0_TXD1	A16	ETH0_TXD1	F15
EMAC0_TXD2	P2-108	HPS_GPIO3	C9	ETH0_TXD2	A15	ETH0_TXD2	H15
EMAC0_TXD3	P2-105	HPS_GPIO4	C4	ETH0_TXD3	H13	ETH0_TXD3	G15
EMAC0_MDC	P2-112	HPS_GPIO7	C7	ETH0_MDC	B15	ETH0_MDC	B15
EMAC0_MDIO	P2-115	HPS_GPIO6	D4	ETH0_MDIO	A17	ETH0_MDIO	H17

3.1.2 HPS Gigabit Ethernet Phy 1 (U600)

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
CLK25_PHY1	P2-174	CLKEXTE	–	CLK25_3	–	CLK25_O	–
RST_N	–	–	–	–	–	–	–
HPS_GPI4	P2-148	HPS_GPI4	R28	–	–	–	–
EMAC1_RX_CLK	P1-110	IOB4A21	AA13	ETH1_RXC	R5	ETH1_RXC	C6
EMAC1_RX_CTL	P1-165	IOB5A12	AC24	ETH1_RX_DV	P8	ETH1_RX_DV	C4
EMAC1_RXD0	P1-169	IOB5A10	AA24	ETH1_RXD0	R8	ETH1_RXD0	A5
EMAC1_RXD1	P1-170	IOB5A2	V16	ETH1_RXD1	P9	ETH1_RXD1	A6
EMAC1_RXD2	P1-168	IOB5A3	V15	ETH1_RXD2	R6	ETH1_RXD2	B7
EMAC1_RXD3	P1-173	IOB5A8	Y16	ETH1_RXD3	P6	ETH1_RXD3	A7
EMAC1_TX_CLK	P1-159	IOB5A15	AE26	ETH1_GTXCLK	P4	ETH1_GTXCLK	D18
EMAC1_TX_CTL	P1-172	IOB5A1	AD26	ETH1_TX_EN	T3	ETH1_TX_EN	C5
EMAC1_TXD0	P1-174	IOB5A0	AE25	ETH1_TXD0	T2	ETH1_TXD0	D8
EMAC1_TXD1	P1-163	IOB5A13	AB23	ETH1_TXD1	P3	ETH1_TXD1	D9
EMAC1_TXD2	P1-171	IOB5A9	W15	ETH1_TXD2	N4	ETH1_TXD2	B8
EMAC1_TXD3	P1-166	IOB5A4	Y17	ETH1_TXD3	R4	ETH1_TXD3	A8
EMAC1_MDC	P1-161	IOB5A14	AF26	ETH1_MDC	N8	ETH1_MDC	B5
EMAC1_MDIO	P1-164	IOB5A5	Y18	ETH1_MDIO	P7	ETH1_MDIO	E18

3.2 Boot Select

Connector P32 offers the selection of the boot-media as follows:

closed	FPGA boot
open	eMMC boot

3.3 IDT Clock-Buffer

Pin header P9 on the MXXEVP provides the I2C programming interface for the IDT Clock buffer on the MCV, M100PF and M100PFS SoM:

3.3.1 Connector P9

Function	Pin	Pin	Function
GND	1	2	IDT_SEL0
GND	3	4	IDT_SEL1
GND	5	6	IDT_SEL2
IDT_SDAT	7	8	VCC33
IDT_SCLK	9	10	VCC18

3.3.2 DIP Switch S1

DIP Switch S1 can be used to configure the clock chip on MCV, M100PF and M100PFS change the JTAG scan chain. The clock chip can be programmed with an external I2C device or directly by the SoM while using the I2C0 interface. While configuring the clock chip directly with the SoM, care should be taken to use a valid configuration, since a wrong clock can render the board inoperable until it the clock chip is reconfigured with an **external** I2C device.

Switch one to three can be used to select one of six configurations stored in the IDT5V49EE904 clock generator. Switch 'on' represents a logic one and 'off' a logic zero.

Switch	Signal	Default
1	IDT_SEL0	off
2	IDT_SEL1	off
3	IDT_SEL2	off

Switch four and five connect the clock generator's I2C bus to the SoM's I2C0 bus and therefore enable it to program the clock generator directly with the SoM. These switches should always be set together.

Switch	Signal	Default
4	I2C0_SDA to IDT_SDAT	off
5	I2C0_SCL to IDT_SCL	off

Switch six to eight include/exclude the FMC connector into the JTAG scan chain. There are only two valid combinations. The first and default one is shown in the following table and directly connects the JTAG header P8 with the MCV board.

Switch	Signal	configuration 1 (default)
6	MCV_TDO	on
7	MCV_TDO	off
8	FMC_TDO	off

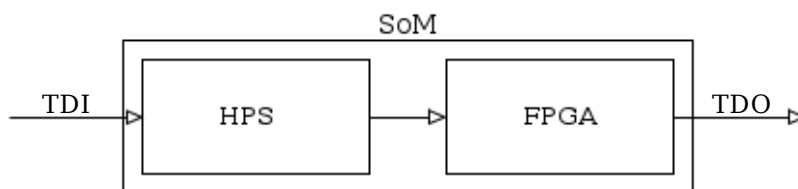


Fig. 1: JTAG scan chain in default configuration

The second valid combination is listed in the next table and includes the FMC connector into the JTAG scan chain.

Switch	Signal	configuration 2
6	MCV_TDO	off
7	MCV_TDO	on
8	HSMC_TDO	on

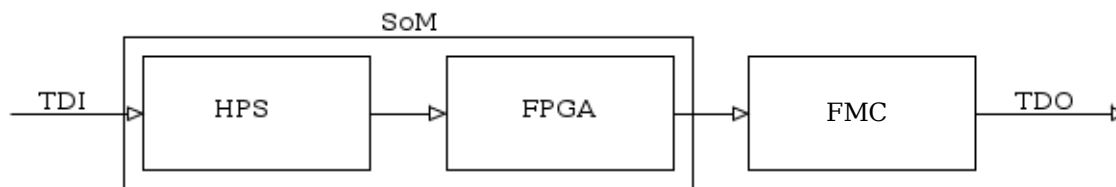


Fig. 2: JTAG scan chain with FMC in serial.

3.4 MicroSD card

MXXEVP offers a slot to hold a microSD card.

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
SD_DATA2	P1-27	IOB3A15	T8	SD_DATA2	C9	SD_DAT2	K4
SD_DATA3	P1-29	IOB3A14	U9	SD_DATA3	B10	SD_DAT3	J7
SD_CMD	P1-31	IOB3A13	V10	SD_CMD	B9	SD_CMD	K5
SD_CLK	P1-33	IOB3A12	U10	SD_CLK	A2	SD_CLK	J1
SD_DATA0	P1-35	IOB3A11	Y8	SD_DATA0	C12	SD_DAT0	H1
SD_DATA1	P1-37	IOB3A10	W8	SD_DATA1	C11	SD_DAT1	J4
SD_DETECT	P1-39	IOB3A9	Y4	SD_DETECT	C10	SD_PRS_N	–

3.5 JTAG

P8 provides the JTAG signals of the SoC FPGA to the outer world. The JTAG connector complies with the standard Altera pinout, the USB-Blaster or the new USB-Blaster II can be directly connected. The following signals are available:

3.5.1 Connector P8

Function	Pin	Pin	Function
TCK	1	2	GND
TDO	3	4	VCC33
TMS	5	6	VJTAG
HPS_RST_N	7	8	TRSTN
TDI	9	10	GND

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
TCK	P1-6	TCK	AB5	JTAG_TCK	F8	JTAG_TCK	E9
MCV_TDO	P1-4	TDO	Y9	JTAG_TDO	F6	JTAG_TDO	E8
TMS	P1-10	TMS	AC7	JTAG_TMS	F7	JTAG_TMS	F8
HPS_RST_N	P2-159	HPS_RST_N	A23	POR_N	–	POR_N	–
TDI	P1-8	TDI	D22	JTAG_TDI	G8	JTAG_TDI	G9
VJTAG	P1-12	VCCPD8A5B	–	JTAG_VIO	1.8V	JTAG_VIO	1.8V
TRSTN	P1-2	GND	–	JTAG_TRSTN	G7	JTAG_TRSTN	G8

3.6 Reset Button

Button P4 is connected to the HPS_RSTn signal of MCV, M100PF and M100PFS.

3.7 UART

Two UARTs are available on MXXEVP located at position U100. The CP2105 is a highly integrated USB-to-Dual-UART Bridge Controller providing a simple solution for updating RS-232 designs to USB using a minimum of components and PCB space.

The CP2105 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, one-time programmable ROM, and two asynchronous serial data buses (UART) with full modem control signals.

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
UART1_RX	P1-77	IOB3B16	AE12	UART1_RX	J7	GPIO_B14	B14
UART1_TX	P1-75	IOB3B17	AD12	UART1_TX	K6	GPIO_E14	E14
GND	–	–	–	–	–	–	–
UART0_RX	P2-138	HPS_GPIO49	A22	UART0_RX	J8	MSS_IO35	A3
UART0_TX	P2-132	HPS_GPIO50	B21	UART0_TX	K8	MSS_IO36	E3

3.8 CAN

Two CAN ports are available on MXXEVP. The signals on the DSUB connector can optionally be terminated by 120 Ohms. This is done by setting the jumpers at position P19 and P20.

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
CAN0_TX	P2-129	HPS_GPIO62	H17	CAN0_TX	F17	MSS_IO31	E4
CAN0_RX	P2-137	HPS_GPIO61	A17	CAN0_RX	G17	MSS_IO32	B2
CAN1_TX	P2-135	HPS_GPIO54	J18	CAN1_TX	F16	MSS_IO28	D3
CAN1_RX	P2-130	HPS_GPIO53	A20	CAN1_RX	F15	MSS_IO29	C2

3.8.1 CAN1 (P23)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.8.2 CAN2 (P24)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.9 USB-OTG

MXXEVP supports an USB-OTG port. The Microchip USB3320 USB-OTG Phy drives the physical connection, it is connected to the HPS of the SoC-FPGA by using the ULPI interface running at 1.8V. The respective connector on MXXEVP could be found at position P201.

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
USB_D0	P2-100	HPS_GPIO15	A16	–	–	MSS_IO18	F2
USB_D1	P2-87	HPS_GPIO16	J14	–	–	MSS_IO19	E1
USB_D2	P2-98	HPS_GPIO17	A15	–	–	MSS_IO20	G3
USB_D3	P2-99	HPS_GPIO18	D17	–	–	MSS_IO21	F5
USB_D4	P2-85	HPS_GPIO22	J13	–	–	MSS_IO22	D1
USB_D5	P2-86	HPS_GPIO23	A12	–	–	MSS_IO23	D2
USB_D6	P2-82	HPS_GPIO24	J12	–	–	MSS_IO24	F6
USB_D7	P2-84	HPS_GPIO25	A11	–	–	MSS_IO25	F3
USB_CLK	P2-83	HPS_GPIO29	A8	–	–	MSS_IO14	G2
USB_NXT	P2-88	HPS_GPIO32	J16	–	–	MSS_IO16	G5
USB_DIR	P2-81	HPS_GPIO31	A7	–	–	MSS_IO15	F1
USB_STP	P2-95	HPS_GPIO30	H16	–	–	MSS_IO17	G4

3.10 LCD Interface

Many applications in the world of applications based on ARN architecture require display support. MXXEVP offers a TFT display interface, the MCV, M100PF and M100PFS reference implementation offers a display controller IP. The TFT interface is implemented on the following signals:

Function	Pin	Pin	Function
	40	1	
GND	39	2	
LCD_CLK	38	3	
Touch YMI	37	4	Backlight
Touch XMI	36	5	Backlight
LCD_R0	35	6	Backlight
LCD_R1	34	7	VCC33
LCD_R2	33	8	
GND	32	9	LCD_DE
LCD_R3	31	10	Touch XP1
LCD_R4	30	11	Touch YP1
LCD_R5	29	12	LCD_DIM
GND	28	13	LCD_B5
LCD_G0	27	14	LCD_B4
LCD_G1	26	15	LCD_B3
LCD_G2	25	16	GND
GND	24	17	LCD_B2
LCD_G3	23	18	LCD_B1
LCD_G4	22	19	LCD_B0
LCD_G5	21	20	GND

3.10.1 LCD

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
LCD_R0	P1-30	IOB3A6	AA11	GPIO_A3	A3	GPIO_B12	B12
LCD_R1	P1-32	IOB3A5	AD5	GPIO_D3	D3	GPIO_D16	D16
LCD_R2	P1-34	IOB3A4	AE6	GPIO_E3	E3	GPIO_E16	E16
LCD_R3	P1-36	IOB3A3	AD4	GPIO_B3	B3	GPIO_F16	F16
LCD_R4	P1-38	IOB3A2	AC4	GPIO_B2	B2	GPIO_F17	F17
LCD_R5	P1-40	IOB3A1	AA4	GPIO_E5	E5	GPIO_D17	D17
LCD_R6	P1-42	IOB3A0	AB4	GPIO_F5	F5	GPIO_C16	C16
LCD_R7	P1-46	IOB3B15	AF9	GPIO_C4	C4	GPIO_A17	A17
LCD_G0	P1-48	IOB3B14	AE8	GPIO_D4	D4	GPIO_A16	A16
LCD_G1	P1-50	IOB3B13	AF8	GPIO_E4	E4	GPIO_D19	D19
LCD_G2	P1-52	IOB3B12	AE7	GPIO_F3	F3	GPIO_E19	E19
LCD_G3	P1-54	IOB3B11	AF4	GPIO_A5	A5	GPIO_C17	C17
LCD_G4	P1-56	IOB3B10	AE4	GPIO_B4	B4	GPIO_B17	B17
LCD_G5	P1-58	IOB3B9	AF6	GPIO_D6	D6	GPIO_D6	D6
LCD_G6	P1-60	IOB3B8	AF5	GPIO_E6	E6	GPIO_D7	D7
LCD_G7	P1-64	IOB3B7	W11	GPIO_G2	G2	GPIO_B9	B9

continues on next page

Table 1 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
LCD_B0	P1-66	IOB3B6	V11	GPIO_H2	H2	GPIO_B10	B10
LCD_B1	P1-68	IOB3B5	U11	GPIO_J2	J2	GPIO_B18	B18
LCD_B2	P1-70	IOB3B4	T11	GPIO_L2	L2	GPIO_A18	A18
LCD_B3	P1-72	IOB3B3	W12	GPIO_M2	M2	GPIO_F10	F10
LCD_B4	P1-45	IOB3B31	AH2	GPIO_E8	E8	GPIO_C9	C9
LCD_B5	P1-47	IOB3B30	AH3	GPIO_B5	B5	GPIO_C10	C10
LCD_B6	P1-49	IOB3B29	AH4	GPIO_C5	C5	GPIO_A11	A11
LCD_B7	P1-51	IOB3B28	AG5	GPIO_C6	C6	GPIO_A10	A10
LCD_T_RESET	P1-41	IOB3A8	Y5	GPIO_A12	A12	GPIO_C7	C7
LCD_T_INT	P2-124	HPS_GPIO57	A18	–	–	GPIO_B21	B21
I2C0_SDA	P2-126	HPS_GPIO55	A19	I2C1_SDA	H6	MSS_IO27	B1
I2C0_SCL	P2-139	HPS_GPIO56	C18	I2C1_SCL	H5	MSS_IO26	C1
LCD_DIM	P1-53	IOB3B27	AH5	GPIO_C7	C7	GPIO_D11	D11
LCD_CLK	P1-28	IOB3A7	Y11	GPIO_C2	C2	GPIO_C12	C12
LCD_DISP	P1-55	IOB3B26	AH6	GPIO_D7	D7	GPIO_C11	C11
LCD_HSYNK	P1-74	IOB3B2	V12	GPIO_H1	H1	GPIO_E10	E10
LCD_VSYNK	P1-76	IOB3B1	T13	GPIO_J1	J1	GPIO_F11	F11
LCD_DE	P1-78	IOB3B0	T12	GPIO_K1	K1	GPIO_F12	F12

3.11 Touch Controller

The touch controller (STMPE811) uses an I2C interface to connect to the FPGA. The interface is available on the following location:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
I2C_SDA	P2-126	HPS_GPIO55	A19	I2C1_SDA	H6	MSS_IO27	B1
I2C_SCL	P2-139	HPS_GPIO56	C18	I2C1_SCL	H5	MSS_IO26	C1
LCD_T_INT	P2-124	HPS_GPIO57	A18	–	–	GPIO_B21	B21

3.12 PMOD Module Connectors

Three 2x6 angled pin headers are available on the MXXEVP board which fit the requirements for Pmod modules. To support a wider range of possible modules, each connector has its own level shifter. A corresponding jumper allows the selection between 3.3V or 5V module voltage.

Connector J4				Connector J5				Connector J6			
Function	Pin	Pin	Function	Function	Pin	Pin	Function	Function	Pin	Pin	Function
IOB4A16	1	7	IOB4A17	HPS_GPIO48	7	HPS_GPIO63	HPS_GPIO26	1	7	HPS_GPIO58	
IOB4A44	2	8	IOB4A45	IOB5A6	2	8	HPS_GPIO64	HPS_GPIO27	2	8	HPS_GPIO59
IOB4A52	3	9	IOB4A53	IOB8A3	3	9	HPS_GPIO65	HPS_GPIO21	3	9	HPS_GPIO60
IOB3B0	4	10	IOB3B1	IOB8A2	4	10	HPS_GPIO66	HPS_GPIO20	4	10	HPS_GPIO19
GND	5	11	GND	GND	5	11	GND	GND	5	11	GND
VCC	6	12	VCC	VCC	6	12	VCC	VCC	6	12	VCC

3.12.1 Connector J4:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
IOB4A16	P1-120	IOB4A16	AF18	GPIO_R1	R1	GPIO_D12	D12
IOB4A17	P1-118	IOB4A17	AH12	GPIO_T1	T1	GPIO_E11	E11
IOB4A44	P1-133	IOB4A44	AG26	GPIO_N1	N1	GPIO_E13	E13
IOB4A45	P1-131	IOB4A45	AH26	GPIO_P1	P1	GPIO_F13	F13
IOB4A52	P1-115	IOB4A52	AG21	GPIO_R3	R3	GPIO_H12	H12
IOB4A53	P1-113	IOB4A53	AH21	GPIO_T5	T5	GPIO_G12	G12
HPS_GPIO37	P2-70	HPS_GPIO37	A5	GPIO_E11	E11	GPIO_B19	B19
HPS_GPIO44	P2-71	HPS_GPIO44	B12	GPIO_F11	F11	GPIO_B20	B20

3.12.2 Connector J5:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
HPS_GPIO48	P2-136	HPS_GPIO48	C21	GPIO_M8	M8	GPIO_C20	C20
HPS_GPIO63	P2-127	HPS_GPIO63	C19	GPIO_N6	N6	GPIO_C19	C19
IOB5A6	P1-162	IOB5A6	AA20	GPIO_T6	T6	GPIO_G13	G13
HPS_GPIO64	P2-121	HPS_GPIO64	B16	GPIO_N7	N7	GPIO_A21	A21
IOB8A3	P1-15	IOB8A3	D8	GPIO_A13	A13	LPRB_B	C15
HPS_GPIO65	P2-128	HPS_GPIO65	B19	GPIO_M9	M9	GPIO_B22	B22
IOB8A2	P1-17	IOB8A2	E8	GPIO_B17	B17	LPRB_A	C14
HPS_GPIO66	P2-123	HPS_GPIO66	C16	GPIO_N5	N5	GPIO_A20	A20

3.12.3 Connector J6:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
HPS_GPIO26	P2-93	HPS_GPIO26	C15	GPIO_K4	K4	–	–
HPS_GPIO58	P2-125	HPS_GPIO58	C17	GPIO_L3	L3	–	–
HPS_GPIO27	P2-80	HPS_GPIO27	A9	GPIO_L7	L7	–	–
HPS_GPIO59	P2-122	HPS_GPIO59	B18	GPIO_M4	M4	–	–
HPS_GPIO21	P2-90	HPS_GPIO21	A13	GPIO_M7	M7	–	–
HPS_GPIO60	P2-133	HPS_GPIO60	J17	GPIO_M5	M5	–	–
HPS_GPIO20	P2-97	HPS_GPIO20	E16	GPIO_K5	K5	–	–
HPS_GPIO19	P2-94	HPS_GPIO19	A14	GPIO_L6	L6	–	–

3.13 Pin Header

Pinheader P3 provides access to 27 IO Pins of MCV.

3.13.1 Connector P3

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
HPS_GPIO14	P2-89	HPS_GPIO14	J15	GPIO_C14	C14	–	–
HPS_GPIO33	P2-79	HPS_GPIO33	A6	GPIO_E14	E14	–	–
HPS_GPIO34	P2-92	HPS_GPIO34	C14	GPIO_D14	D14	–	–
HPS_GPI1	P2-144	HPS_GPI1	K27	GPIO_J3	J3	–	–
HPS_GPI2	P2-149	HPS_GPI2	R20	GPIO_D11	D11	–	–
HPS_GPI5	P2-146	HPS_GPI5	P26	GPIO_E10	E10	–	–
HPS_GPI6	P2-150	HPS_GPI6	T17	GPIO_K3	K3	–	–
HPS_GPI7	P2-147	HPS_GPI7	T16	GPIO_F12	F12	–	–
HPS_GPI8	P2-153	HPS_GPI8	Y28	GPIO_D12	D12	MSS_IO37	D4
HPS_GPI9	P2-155	HPS_GPI9	Y26	GPIO_F10	F10	MSS_IO30	E5
HPS_GPI10	P2-143	HPS_GPI10	U15	GPIO_E13	E13	–	–
HPS_GPI11	P2-145	HPS_GPI11	U16	GPIO_D13	D13	–	–
HPS_GPI12	P2-152	HPS_GPI12	AC27	GPIO_G12	G12	–	–
HPS_GPIO35	P2-96	HPS_GPIO35	B14	GPIO_C15	C15	–	–
IOB5A11	P1-167	IOB5A11	AA23	GPIO_L1	L1	GPIO_B4	B4
IOB4A20	P1-112	IOB4A20	Y13	GPIO_F1	F1	GPIO_A12	A12
IOB5A7	P1-142	IOB4A7	AE23	–	–	HSIO_U12	U12

3.14 FMC connector

MXXEVP houses a FPGA Mezzanine Card (FMC) connector. Its pinout is shown in the following table.

3.14.1 Connector J2A:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
GXB_RX_L1_P	P2-21	GXB_RX_L1_P	AB2	RX1_P	T22	RX1_P	K22
GXB_RX_L1_N	P2-23	GXB_RX_L1_N	AB1	RX1_N	T21	RX1_N	K21
GXB_RX_L2_P	P2-33	GXB_RX_L2_P	V2	RX2_P	W20	RX2_P	M22
GXB_RX_L2_N	P2-35	GXB_RX_L2_N	V1	RX2_N	W19	RX2_N	M21
GXB_RX_L3_P	P2-10	GXB_RX_L3_P	P2	RX4_P	A20	RX3_P	R20
GXB_RX_L3_N	P2-12	GXB_RX_L3_N	P1	RX4_N	A19	RX3_N	R19
GXB_RX_L4_P	P2-22	GXB_RX_L4_P	K2	RX5_P	C20	RX4_P	L5
GXB_RX_L4_N	P2-24	GXB_RX_L4_N	K1	RX5_N	C19	RX4_N	L6
GXB_RX_L5_P	P2-34	GXB_RX_L5_P	F2	RX6_P	F22	RX5_P	K6
GXB_RX_L5_N	P2-36	GXB_RX_L5_N	F1	RX6_N	F21	RX5_N	K7
GXB_TX_L1_P	P2-27	GXB_TX_L1_P	Y2	TX1_P	V22	TX1_P	H22
GXB_TX_L1_N	P2-29	GXB_TX_L1_N	Y1	TX1_N	V21	TX1_N	H21
GXB_TX_L2_P	P2-39	GXB_TX_L2_P	T2	TX2_P	Y22	TX2_P	P21
GXB_TX_L2_N	P2-41	GXB_TX_L2_N	T1	TX2_N	Y21	TX2_N	P22
GXB_TX_L3_P	P2-16	GXB_TX_L3_P	M2	TX4_P	B22	TX3_P	T22
GXB_TX_L3_N	P2-18	GXB_TX_L3_N	M1	TX4_N	B21	TX3_N	T21
GXB_TX_L4_P	P2-28	GXB_TX_L4_P	H2	TX5_P	D22	TX4_P	N6
GXB_TX_L4_N	P2-30	GXB_TX_L4_N	H1	TX5_N	D21	TX4_N	N7
GXB_TX_L5_P	P2-40	GXB_TX_L5_P	D2	TX6_P	H22	TX5_P	M7
GXB_TX_L5_N	P2-42	GXB_TX_L5_N	D1	TX6_N	H21	TX5_N	N8

3.14.2 Connector J2B:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
HPS_GPI13	P2-151	HPS_GPI13	V24	—	—	—	—

3.14.3 Connector J2C:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
GXB_TX_LO_P	P2-15	GXB_TX_LO_P	AD2	TX0_P	P22	TX0_P	F22
GXB_TX_LO_N	P2-17	GXB_TX_LO_N	AD1	TX0_N	P21	TX0_N	F21
GXB_RX_LO_P	P2-9	GXB_RX_LO_P	AF2	RX0_P	M22	RX0_P	G20
GXB_RX_LO_N	P2-11	GXB_RX_LO_N	AF1	RX0_N	M21	RX0_N	G19
IOB4A13	P1-128	IOB4A13	AF22	–	–	–	–
IOB4A12	P1-130	IOB4A12	AF21	–	–	–	–
IOB4A24	P1-102	IOB4A24	AD17	–	–	HSIO_AB14	AB14
IOB4A25	P1-100	IOB4A25	AE17	–	–	HSIO_AB13	AB13
IOB4A32	P1-84	IOB4A32	AG10	–	–	HSIO_AA16	AA16
IOB4A33	P1-82	IOB4A33	AH9	–	–	HSIO_AB17	AB17
IOB4A40	P1-143	IOB4A40	AF27	–	–	HSIO_Y19	Y19
IOB4A41	P1-141	IOB4A41	AF28	–	–	HSIO_W19	W19
IOB4A62	P1-93	IOB4A62	AG15	–	–	HSIO_U17	U17
IOB4A63	P1-91	IOB4A63	AH14	–	–	HSIO_T16	T16

3.14.4 Connector J2D:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
REFCLK0L_P	P2-3	REFCLK0L_P	V5	XCR0_REF _CLK_P	–	XCVR0_REF _CLK_P	L19
REFCLK0L_N	P2-5	REFCLK0L_N	V4	XCR0_RE F_CLK_N	–	XCVR0_REF _CLK_N	L20
IOB4A2	P1-152	IOB4A2	U14	–	–	HSIO_Y13	Y13
IOB4A3	P1-150	IOB4A3	U13	–	–	HSIO_AA12	AA12
IOB4A11	P1-132	IOB4A11	AF20	–	–	–	–
IOB4A10	P1-134	IOB4A10	AG20	–	–	HSIO_W12	W12
IOB4A22	P1-108	IOB4A22	W14	–	–	HSIO_AA15	AA15
IOB4A23	P1-106	IOB4A23	V13	–	–	HSIO_AB15	AB15
IOB4A30	P1-90	IOB4A30	AG9	–	–	HSIO_W16	W16
IOB4A31	P1-88	IOB4A31	AH8	–	–	HSIO_W17	W17
IOB4A38	P1-147	IOB4A38	AD23	–	–	CLK_60M	–
IOB4A39	P1-145	IOB4A39	AE22	–	–	GND	–
IOB4A54	P1-111	IOB4A54	AG19	–	–	HSIO_AA21	AA21
IOB4A55	P1-109	IOB4A55	AH19	–	–	HSIO_AB21	AB21
IOB4A60	P1-97	IOB4A60	AF17	–	–	HSIO_V16	V16
IOB4A61	P1-95	IOB4A61	AG16	–	–	HSIO_U18	U18

3.14.5 Connector J2F:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
CLKEXT_P	P2-160	CLKEXTA	–	OCLK_P	–	OCLK_P	–
CLKEXT_N	P2-162	CLKEXTB	–	OCLK_N	–	OCLK_N	–

3.14.6 Connector J2G:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
IOB4A0	P1-156	IOB4A0	Y15	–	–	–	–
IOB4A1	P1-154	IOB4A1	AA15	–	–	–	–
IOB4A6	P1-144	IOB4A6	AE24	–	–	HSIO_T13	T13
IOB4A7	P1-142	IOB4A7	AE23	–	–	HSIO_U12	U12
IOB4A18	P1-116	IOB4A18	AG13	–	–	–	–
IOB4A19	P1-114	IOB4A19	AF13	–	–	–	–
IOB4A28	P1-94	IOB4A28	AG8	–	–	HSIO_W14	W14
IOB4A29	P1-92	IOB4A29	AH7	–	–	HSIO_V12	V12
IOB4A36	P1-151	IOB4A36	AC22	–	–	–	–
IOB4A37	P1-149	IOB4A37	AC23	–	–	GND	–
IOB4A46	P1-129	IOB4A46	AF25	–	–	HSIO_U15	U15
IOB4A47	P1-127	IOB4A47	AG25	–	–	HSIO_T15	T15
IOB4A50	P1-119	IOB4A50	AH23	–	–	–	–
IOB4A51	P1-117	IOB4A51	AH22	–	–	–	–
IOB4A58	P1-101	IOB4A58	AH17	–	–	HSIO_AA18	AA18
IOB4A59	P1-99	IOB4A59	AH16	–	–	HSIO_V17	V17
IOB4A66	P1-83	IOB4A66	AG11	–	–	HSIO_T17	T17
IOB4A67	P1-81	IOB4A67	AH11	–	–	HSIO_V19	V19
IOB3B20	P1-69	IOB3B20	AF11	–	–	HSIO_V21	V21
IOB3B21	P1-67	IOB3B21	AF10	–	–	HSIO_Y20	Y20
IOB3B24	P1-59	IOB3B24	AF7	–	–	–	–
IOB3B25	P1-57	IOB3B25	AG6	–	–	–	–

3.14.7 Connector J2H:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
HPS_GPIO0	P2-156	HPS_GPIO0	M25	GPIO_L8	L8	MSS_IO33	A2
IOB4A4	P1-148	IOB4A4	AE20	–	–	HSIO_AB12	AB12
IOB4A5	P1-146	IOB4A5	AD20	–	–	HSIO_R12	R12
IOB4A9	P1-136	IOB4A9	AE19	–	–	HSIO_U13	U13
IOB4A8	P1-138	IOB4A8	AD19	–	–	HSIO_U14	U14
IOB4A15	P1-124	IOB4A15	AG23	–	–	–	–
IOB4A14	P1-126	IOB4A14	AF23	–	–	–	–
IOB4A26	P1-98	IOB4A26	AF15	–	–	HSIO_AA13	AA13
IOB4A27	P1-96	IOB4A27	AE15	–	–	HSIO_Y14	Y14
IOB4A34	P1-155	IOB4A34	AA19	–	–	–	–
IOB4A35	P1-153	IOB4A35	AA18	–	–	–	–
IOB4A42	P1-137	IOB4A42	AG28	–	–	HSIO_Y18	Y18
IOB4A43	P1-135	IOB4A43	AH27	–	–	HSIO_W18	W18
IOB4A48	P1-125	IOB4A48	AG24	–	–	HSIO_V15	V15
IOB4A49	P1-123	IOB4A49	AH24	–	–	HSIO_W13	W13
IOB4A56	P1-107	IOB4A56	AG18	–	–	HSIO_AA20	AA20
IOB4A57	P1-105	IOB4A57	AH18	–	–	HSIO_AB20	AB20
IOB4A64	P1-89	IOB4A64	AG14	–	–	HSIO_R14	R14
IOB4A65	P1-87	IOB4A65	AH13	–	–	HSIO_R15	R15
IOB3B19	P1-71	IOB3B19	AD11	–	–	HSIO_W21	W21
IOB3B18	P1-73	IOB3B18	AF11	–	–	HSIO_AA22	AA22
IOB3B22	P1-65	IOB3B22	AD10	–	–	HSIO_Y21	Y21
IOB3B23	P1-63	IOB3B23	AE9	–	–	HSIO_W22	W22

3.14.8 Connector J2J:

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
IOB8A0	P1-21	IOB8A0	E11	–	–	–	–
IOB8A1	P1-19	IOB8A1	D11	–	–	–	–
HPS_GPIO51	P2-134	HPS_GPIO51	A21	GPIO_M3	M3	GPIO_D20	D20
HPS_GPIO52	P2-131	HPS_GPIO52	K18	GPIO_F13	F13	GPIO_D21	D21
IOB5B0	P1-24	IOB5B0	Y24	–	–	–	–
IOB5B1	P1-22	IOB5B1	W24	–	–	–	–
IOB5B2	P1-20	IOB5B2	AB26	–	–	–	–
IOB5B3	P1-18	IOB5B3	AA26	–	–	–	–
IOB5B4	P1-16	IOB5B4	W21	–	–	ICLK_P	–
IOB5B5	P1-14	IOB5B5	W20	–	–	ICLK_N	–

3.15 miniPCIe and PCIe

Unlike the MCVEVP, the MXXEVP does not house a miniPCIe slot. Nevertheless we offer adapters for miniPCIe and PCIe x8 cards, which can be inserted into the FMC connectors.

3.16 Samtec Connector

The MCV, M100PF and M100PFS SoMS connect to the MXXEVP Baseboard using two Samtec QSH-090-01-F-D-A connectors.

3.16.1 Connector P1

MXXEVP		MCV		M100PF		M100PFS	
Function	Connector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
VCC33	P1-1	VCC33	–	–	–	V_3P3V	–
TRSTN	P1-2	GND	–	JTAG_TRSTN	G7	JTAG_TRSTN	G8
VCC33	P1-3	VCC33	–	–	–	V_3P3V	–
MCV_TDO	P1-4	TDO	Y9	JTAG_TDO	F6	JTAG_TDO	E8
VCC33	P1-5	VCC33	–	–	–	V_3P3V	–
TCK	P1-6	TCK	AB5	JTAG_TCK	F8	JTAG_TCK	E9
VCC33	P1-7	VCC33	–	–	–	V_3P3V	–
TDI	P1-8	TDI	D22	JTAG_TDI	G8	JTAG_TDI	G9
VCC33	P1-9	VCC33	–	–	–	V_3P3V	–
TMS	P1-10	TMS	AC7	JTAG_TMS	F7	JTAG_TMS	F8
VCC33	P1-11	VCC33	–	–	–	V_3P3V	–
VJTAG	P1-12	VCCPD8A5B	–	JTAG_VIO	1.8V	JTAG_VIO	1.8V
VCCIO8A	P1-13	VCCIO8A5B	–	–	–	–	–
IOB5B5	P1-14	IOB5B5	W20	–	–	ICLK_N	–
IOB8A3	P1-15	IOB8A3	D8	GPIO_A13	A13	LPRB_B	C15
IOB5B4	P1-16	IOB5B4	W21	–	–	ICLK_P	–
IOB8A2	P1-17	IOB8A2	E8	GPIO_B17	B17	LPRB_A	C14
IOB5B3	P1-18	IOB5B3	AA26	–	–	–	–
IOB8A1	P1-19	IOB8A1	D11	–	–	–	–
IOB5B2	P1-20	IOB5B2	AB26	–	–	–	–
IOB5B1	P1-22	IOB5B1	W24	–	–	–	–
IOB8A0	P1-21	IOB8A0	E11	–	–	–	–
VCCIO8A	P1-23	VCCIO8A5B	–	–	–	–	–
IOB5B0	P1-24	IOB5B0	Y24	–	–	–	–
VCC33	P1-25	VCC33	–	–	–	V_3P3V	–
VCCPD8A	P1-26	VCCIO8A5B	–	–	–	–	–
SD_DATA2	P1-27	IOB3A15	T8	SD_DATA2	C9	SD_DAT2	K4
LCD_CLK	P1-28	IOB3A7	Y11	GPIO_C2	C2	GPIO_C12	C12
SD_DATA3	P1-29	IOB3A14	U9	SD_DATA3	B10	SD_DAT3	J7
LCD_R0	P1-30	IOB3A6	AA11	GPIO_A3	A3	GPIO_B12	B12
SD_CMD	P1-31	IOB3A13	V10	SD_CMD	B9	SD_CMD	K5
LCD_R1	P1-32	IOB3A5	AD5	GPIO_D3	D3	GPIO_D16	D16
SD_CLK	P1-33	IOB3A12	U10	SD_CLK	A2	SD_CLK	J1

continues on next page

Table 2 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
LCD_R2	P1-34	IOB3A4	AE6	GPIO_E3	E3	GPIO_E16	E16
SD_DATA0	P1-35	IOB3A11	Y8	SD_DATA0	C12	SD_DAT0	H1
LCD_R3	P1-36	IOB3A3	AD4	GPIO_B3	B3	GPIO_F16	F16
SD_DATA1	P1-37	IOB3A10	W8	SD_DATA1	C11	SD_DAT1	J4
LCD_R4	P1-38	IOB3A2	AC4	GPIO_B2	B2	GPIO_F17	F17
SD_DETECT	P1-39	IOB3A9	Y4	SD_DETECT	C10	SD_PRS_N	–
LCD_R5	P1-40	IOB3A1	AA4	GPIO_E5	E5	GPIO_D17	D17
LCD_T_RESET	P1-41	IOB3A8	Y5	GPIO_A12	A12	GPIO_C7	C7
LCD_R6	P1-42	IOB3A0	AB4	GPIO_F5	F5	GPIO_C16	C16
VCCIO3B4A	P1-43	VCCIO3B	–	–	–	–	–
VCCIO3B4A	P1-44	VCCIO3B	–	–	–	–	–
LCD_B4	P1-45	IOB3B31	AH2	GPIO_E8	E8	GPIO_C9	C9
LCD_R7	P1-46	IOB3B15	AF9	GPIO_C4	C4	GPIO_A17	A17
LCD_B5	P1-47	IOB3B30	AH3	GPIO_B5	B5	GPIO_C10	C10
LCD_G0	P1-48	IOB3B14	AE8	GPIO_D4	D4	GPIO_A16	A16
LCD_B6	P1-49	IOB3B29	AH4	GPIO_C5	C5	GPIO_A11	A11
LCD_G1	P1-50	IOB3B13	AF8	GPIO_E4	E4	GPIO_D19	D19
LCD_B7	P1-51	IOB3B28	AG5	GPIO_C6	C6	GPIO_A10	A10
LCD_G2	P1-52	IOB3B12	AE7	GPIO_F3	F3	GPIO_E19	E19
LCD_DIM	P1-53	IOB3B27	AH5	GPIO_C7	C7	GPIO_D11	D11
LCD_G3	P1-54	IOB3B11	AF4	GPIO_A5	A5	GPIO_C17	C17
LCD_DISP	P1-55	IOB3B26	AH6	GPIO_D7	D7	GPIO_C11	C11
LCD_G4	P1-56	IOB3B10	AE4	GPIO_B4	B4	GPIO_B17	B17
IOB3B25	P1-57	IOB3B25	AG6	–	–	–	–
LCD_G5	P1-58	IOB3B9	AF6	GPIO_D6	D6	GPIO_D6	D6
IOB3B24	P1-59	IOB3B24	AF7	–	–	–	–
LCD_G6	P1-60	IOB3B8	AF5	GPIO_E6	E6	GPIO_D7	D7
VCCIO3B4A	P1-61	VCCIO3B	–	–	–	HSIO_V22	V22
VCCIO3B4A	P1-62	VCCPD3B4A	–	–	–	–	–
IOB3B23	P1-63	IOB3B23	AE9	–	–	HSIO_W22	W22
LCD_G7	P1-64	IOB3B7	W11	GPIO_G2	G2	GPIO_B9	B9
IOB3B22	P1-65	IOB3B22	AD10	–	–	HSIO_Y21	Y21
LCD_B0	P1-66	IOB3B6	V11	GPIO_H2	H2	GPIO_B10	B10
IOB3B21	P1-67	IOB3B21	AF10	–	–	HSIO_Y20	Y20
LCD_B1	P1-68	IOB3B5	U11	GPIO_J2	J2	GPIO_B18	B18
IOB3B20	P1-69	IOB3B20	AF11	–	–	HSIO_V21	V21
LCD_B2	P1-70	IOB3B4	T11	GPIO_L2	L2	GPIO_A18	A18
IOB3B19	P1-71	IOB3B19	AD11	–	–	HSIO_W21	W21
LCD_B3	P1-72	IOB3B3	W12	GPIO_M2	M2	GPIO_F10	F10
IOB3B18	P1-73	IOB3B18	AF11	–	–	HSIO_AA22	AA22
LCD_HSYNC	P1-74	IOB3B2	V12	GPIO_H1	H1	GPIO_E10	E10
UART1_TX	P1-75	IOB3B17	AD12	UART1_TX	K6	GPIO_E14	E14
LCD_VSYNC	P1-76	IOB3B1	T13	GPIO_J1	J1	GPIO_F11	F11
UART1_RX	P1-77	IOB3B16	AE12	UART1_RX	J7	GPIO_B14	B14
LCD_DE	P1-78	IOB3B0	T12	GPIO_K1	K1	GPIO_F12	F12
VCCIO3B4A	P1-79	VCCIO3B	–	–	–	HSIO_V20	V20
VCCIO3B4A	P1-80	VCCPD3B4A	–	–	–	HSIO_AA17	AA17

continues on next page

Table 2 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
IOB4A67	P1-81	IOB4A67	AH11	–	–	HSIO_V19	V19
IOB4A33	P1-82	IOB4A33	AH9	–	–	HSIO_AB17	AB17
IOB4A66	P1-83	IOB4A66	AG11	–	–	HSIO_T17	T17
IOB4A32	P1-84	IOB4A32	AG10	–	–	HSIO_AA16	AA16
VCCIO3B4A	P1-85	VCCIO4A	–	–	–	HSIO_R16	R16
VCCIO3B4A	P1-86	VCCPD3B4A	–	–	–	HSIO_Y16	Y16
IOB4A65	P1-87	IOB4A65	AH13	–	–	HSIO_R15	R15
IOB4A31	P1-88	IOB4A31	AH8	–	–	HSIO_W17	W17
IOB4A64	P1-89	IOB4A64	AG14	–	–	HSIO_R14	R14
IOB4A30	P1-90	IOB4A30	AG9	–	–	HSIO_W16	W16
IOB4A63	P1-91	IOB4A63	AH14	–	–	HSIO_T16	T16
IOB4A29	P1-92	IOB4A29	AH7	–	–	HSIO_V12	V12
IOB4A62	P1-93	IOB4A62	AG15	–	–	HSIO_U17	U17
IOB4A28	P1-94	IOB4A28	AG8	–	–	HSIO_W14	W14
IOB4A61	P1-95	IOB4A61	AG16	–	–	HSIO_U18	U18
IOB4A27	P1-96	IOB4A27	AE15	–	–	HSIO_Y14	Y14
IOB4A60	P1-97	IOB4A60	AF17	–	–	HSIO_V16	V16
IOB4A26	P1-98	IOB4A26	AF15	–	–	HSIO_AA13	AA13
IOB4A59	P1-99	IOB4A59	AH16	–	–	HSIO_V17	V17
IOB4A25	P1-100	IOB4A25	AE17	–	–	HSIO_AB13	AB13
IOB4A58	P1-101	IOB4A58	AH17	–	–	HSIO_AA18	AA18
IOB4A24	P1-102	IOB4A24	AD17	–	–	HSIO_AB14	AB14
VCCIO3B4A	P1-103	VCCIO4A	–	–	–	HSIO_AB19	AB19
VCCIO3B4A	P1-104	VCCPD3B4A	–	–	–	HSIO_Y15	Y15
IOB4A57	P1-105	IOB4A57	AH18	–	–	HSIO_AB20	AB20
IOB4A23	P1-106	IOB4A23	V13	–	–	HSIO_AB15	AB15
IOB4A56	P1-107	IOB4A56	AG18	–	–	HSIO_AA20	AA20
IOB4A22	P1-108	IOB4A22	W14	–	–	HSIO_AA15	AA15
IOB4A55	P1-109	IOB4A55	AH19	–	–	HSIO_AB21	AB21
EMAC1_RX_CLK	P1-110	IOB4A21	AA13	ETH1_RXC	R5	ETH1_RXC	C6
IOB4A54	P1-111	IOB4A54	AG19	–	–	HSIO_AA21	AA21
IOB4A20	P1-112	IOB4A20	Y13	GPIO_F1	F1	GPIO_A12	A12
IOB4A53	P1-113	IOB4A53	AH21	GPIO_T5	T5	GPIO_G12	G12
IOB4A19	P1-114	IOB4A19	AF13	–	–	–	–
IOB4A52	P1-115	IOB4A52	AG21	GPIO_R3	R3	GPIO_H12	H12
IOB4A18	P1-116	IOB4A18	AG13	–	–	–	–
IOB4A51	P1-117	IOB4A51	AH22	–	–	–	–
IOB4A17	P1-118	IOB4A17	AH12	GPIO_T1	T1	GPIO_E11	E11
IOB4A50	P1-119	IOB4A50	AH23	–	–	–	–
IOB4A16	P1-120	IOB4A16	AF18	GPIO_R1	R1	GPIO_D12	D12
VCCIO3B4A	P1-121	VCCIO4A	–	–	–	HSIO_V14	V14
VCCIO3B4A	P1-122	VCCPD3B4A	–	–	–	–	–
IOB4A49	P1-123	IOB4A49	AH24	–	–	HSIO_W13	W13
IOB4A15	P1-124	IOB4A15	AG23	–	–	–	–
IOB4A48	P1-125	IOB4A48	AG24	–	–	HSIO_V15	V15
IOB4A14	P1-126	IOB4A14	AF23	–	–	–	–
IOB4A47	P1-127	IOB4A47	AG25	–	–	HSIO_T15	T15

continues on next page

Table 2 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
IOB4A13	P1-128	IOB4A13	AF22	–	–	–	–
IOB4A46	P1-129	IOB4A46	AF25	–	–	HSIO_U15	U15
IOB4A12	P1-130	IOB4A12	AF21	–	–	–	–
IOB4A45	P1-131	IOB4A45	AH26	GPIO_P1	P1	GPIO_F13	F13
IOB4A11	P1-132	IOB4A11	AF20	–	–	–	–
IOB4A44	P1-133	IOB4A44	AG26	GPIO_N1	N1	GPIO_E13	E13
IOB4A10	P1-134	IOB4A10	AG20	–	–	HSIO_W12	W12
IOB4A43	P1-135	IOB4A43	AH27	–	–	HSIO_W18	W18
IOB4A9	P1-136	IOB4A9	AE19	–	–	HSIO_U13	U13
IOB4A42	P1-137	IOB4A42	AG28	–	–	HSIO_Y18	Y18
IOB4A8	P1-138	IOB4A8	AD19	–	–	HSIO_U14	U14
VCCIO3B4A	P1-139	VCCIO4A	–	–	–	HSIO_AB18	AB18
VCCIO3B4A	P1-140	VCCIO4A	–	–	–	HSIO_T12	T12
IOB4A41	P1-141	IOB4A41	AF28	–	–	HSIO_W19	W19
IOB4A7	P1-142	IOB4A7	AE23	–	–	HSIO_U12	U12
IOB4A40	P1-143	IOB4A40	AF27	–	–	HSIO_Y19	Y19
IOB4A6	P1-144	IOB4A6	AE24	–	–	HSIO_T13	T13
IOB4A39	P1-145	IOB4A39	AE22	–	–	GND	–
IOB4A5	P1-146	IOB4A5	AD20	–	–	HSIO_R12	R12
IOB4A38	P1-147	IOB4A38	AD23	–	–	CLK_60M	–
IOB4A4	P1-148	IOB4A4	AE20	–	–	HSIO_AB12	AB12
IOB4A37	P1-149	IOB4A37	AC23	–	–	GND	–
IOB4A3	P1-150	IOB4A3	U13	–	–	HSIO_AA12	AA12
IOB4A36	P1-151	IOB4A36	AC22	–	–	–	–
IOB4A2	P1-152	IOB4A2	U14	–	–	HSIO_Y13	Y13
IOB4A35	P1-153	IOB4A35	AA18	–	–	–	–
IOB4A1	P1-154	IOB4A1	AA15	–	–	–	–
IOB4A34	P1-155	IOB4A34	AA19	–	–	–	–
IOB4A0	P1-156	IOB4A0	Y15	–	–	–	–
VCCIO5A	P1-157	VCCIO5A	–	–	–	–	–
VCCPD5A	P1-158	VCCIO5A	–	–	–	–	–
EMAC1_TX_CLK	P1-159	IOB5A15	AE26	ETH1_GTXCLK	P4	ETH1_GTXCLK	D18
IOB5A7	P1-160	IOB5A7	Y19	GPIO_F2	F2	GPIO_H13	H13
EMAC1_MDC	P1-161	IOB5A14	AF26	ETH1_MDC	N8	ETH1_MDC	B5
IOB5A6	P1-162	IOB5A6	AA20	GPIO_T6	T6	GPIO_G13	G13
EMAC1_TXD1	P1-163	IOB5A13	AB23	ETH1_TXD1	P3	ETH1_TXD1	D9
EMAC1_MDIO	P1-164	IOB5A5	Y18	ETH1_MDIO	P7	ETH1_MDIO	E18
EMAC1_RX_CTL	P1-165	IOB5A12	AC24	ETH1_RX_DV	P8	ETH1_RX_DV	C4
EMAC1_TXD3	P1-166	IOB5A4	Y17	ETH1_TXD3	R4	ETH1_TXD3	A8
IOB5A11	P1-167	IOB5A11	AA23	GPIO_L1	L1	GPIO_B4	B4
EMAC1_RXD2	P1-168	IOB5A3	V15	ETH1_RXD2	R6	ETH1_RXD2	B7
EMAC1_RXD0	P1-169	IOB5A10	AA24	ETH1_RXD0	R8	ETH1_RXD0	A5
EMAC1_RXD1	P1-170	IOB5A2	V16	ETH1_RXD1	P9	ETH1_RXD1	A6
EMAC1_TXD2	P1-171	IOB5A9	W15	ETH1_TXD2	N4	ETH1_TXD2	B8
EMAC1_TX_CTL	P1-172	IOB5A1	AD26	ETH1_TX_EN	T3	ETH1_TX_EN	C5
EMAC1_RXD3	P1-173	IOB5A8	Y16	ETH1_RXD3	P6	ETH1_RXD3	A7
EMAC1_TXD0	P1-174	IOB5A0	AE25	ETH1_TXD0	T2	ETH1_TXD0	D8

continues on next page

Table 2 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
VCCIO5A	P1-175	VCCIO5A	–	–	–	–	–
VCCPD5A	P1-176	VCCIO5A	–	–	–	–	–
VCC33	P1-177	VCC33	–	–	–	V_3P3V	–
VCC33	P1-178	VCC33	–	–	–	V_3P3V	–
VCC33	P1-179	VCC33	–	–	–	V_3P3V	–
VCC33	P1-180	VCC33	–	–	–	V_3P3V	–
GND	P1-181	GND	–	–	–	GND	–
GND	P1-182	GND	–	–	–	GND	–
GND	P1-183	GND	–	–	–	GND	–
GND	P1-184	GND	–	–	–	GND	–
GND	P1-185	GND	–	–	–	GND	–
GND	P1-186	GND	–	–	–	GND	–
GND	P1-187	GND	–	–	–	GND	–
GND	P1-188	GND	–	–	–	GND	–
GND	P1-189	GND	–	–	–	GND	–
GND	P1-190	GND	–	–	–	GND	–
GND	P1-191	GND	–	–	–	GND	–
GND	P1-192	GND	–	–	–	GND	–

3.16.2 Connector P2

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
GND	P2-1	GND	–	–	–	GND	–
GND	P2-2	GND	–	–	–	GND	–
REFCLK0L_P	P2-3	REFCLK0L_P	V5	XCVR0_REF _CLK_P	–	XCVR0_REF _CLK_P	L19
REFCLK1L_P	P2-4	REFCLK1L_P	P8	XCVR1_REF _CLK_P	–	XCVR1_REF _CLK_P	J19
REFCLK0L_N	P2-5	REFCLK0L_N	V4	XCVR0_REF _CLK_N	–	XCVR0_REF _CLK_N	L20
REFCLK1L_N	P2-6	REFCLK1L_N	N8	XCVR1_REF _CLK_N	–	XCVR1_REF _CLK_N	J20
GND	P2-7	GND	–	–	–	GND	–
GND	P2-8	GND	–	–	–	GND	–
GXB_RX_L0_P	P2-9	GXB_RX_L0_P	AF2	RX0_P	M22	RX0_P	G20
GXB_RX_L3_P	P2-10	GXB_RX_L3_P	P2	RX4_P	A20	RX3_P	R20
GXB_RX_L0_N	P2-11	GXB_RX_L0_N	AF1	RX0_N	M21	RX0_N	G19
GXB_RX_L3_N	P2-12	GXB_RX_L3_N	P1	RX4_N	A19	RX3_N	R19
GND	P2-13	GND	–	–	–	GND	–
GND	P2-14	GND	–	–	–	GND	–
GXB_TX_LO_P	P2-15	GXB_TX_LO_P	AD2	TX0_P	P22	TX0_P	F22
GXB_TX_L3_P	P2-16	GXB_TX_L3_P	M2	TX4_P	B22	TX3_P	T22
GXB_TX_LO_N	P2-17	GXB_TX_LO_N	AD1	TX0_N	P21	TX0_N	F21
GXB_TX_L3_N	P2-18	GXB_TX_L3_N	M1	TX4_N	B21	TX3_N	T21

continues on next page

Table 3 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
GND	P2-19	GND	–	–	–	GND	–
GND	P2-20	GND	–	–	–	GND	–
GXB_RX_L1_P	P2-21	GXB_RX_L1_P	AB2	RX1_P	T22	RX1_P	K22
GXB_RX_L4_P	P2-22	GXB_RX_L4_P	K2	RX5_P	C20	RX4_P	L5
GXB_RX_L1_N	P2-23	GXB_RX_L1_N	AB1	RX1_N	T21	RX1_N	K21
GXB_RX_L4_N	P2-24	GXB_RX_L4_N	K1	RX5_N	C19	RX4_N	L6
GND	P2-25	GND	–	–	–	GND	–
GND	P2-26	GND	–	–	–	GND	–
GXB_TX_L1_P	P2-27	GXB_TX_L1_P	Y2	TX1_P	V22	TX1_P	H22
GXB_TX_L4_P	P2-28	GXB_TX_L4_P	H2	TX5_P	D22	TX4_P	N6
GXB_TX_L1_N	P2-29	GXB_TX_L1_N	Y1	TX1_N	V21	TX1_N	H21
GXB_TX_L4_N	P2-30	GXB_TX_L4_N	H1	TX5_N	D21	TX4_N	N7
GND	P2-31	GND	–	–	–	GND	–
GND	P2-32	GND	–	–	–	GND	–
GXB_RX_L2_P	P2-33	GXB_RX_L2_P	V2	RX2_P	W20	RX2_P	M22
GXB_RX_L5_P	P2-34	GXB_RX_L5_P	F2	RX6_P	F22	RX5_P	K6
GXB_RX_L2_N	P2-35	GXB_RX_L2_N	V1	RX2_N	W19	RX2_N	M21
GXB_RX_L5_N	P2-36	GXB_RX_L5_N	F1	RX6_N	F21	RX5_N	K7
GND	P2-37	GND	–	–	–	GND	–
GND	P2-38	GND	–	–	–	GND	–
GXB_TX_L2_P	P2-39	GXB_TX_L2_P	T2	TX2_P	Y22	TX2_P	P21
GXB_TX_L5_P	P2-40	GXB_TX_L5_P	D2	TX6_P	H22	TX5_P	M7
GXB_TX_L2_N	P2-41	GXB_TX_L2_N	T1	TX2_N	Y21	TX2_N	P22
GXB_TX_L5_N	P2-42	GXB_TX_L5_N	D1	TX6_N	H21	TX5_N	N8
GND	P2-43	GND	–	–	–	GND	–
GND	P2-44	GND	–	–	–	GND	–
–	P2-45	–	–	RX3_P	AA20	–	–
–	P2-46	–	–	RX7_P	L20	–	–
–	P2-47	–	–	RX3_N	AA19	–	–
–	P2-48	–	–	RX7_N	L19	–	–
GND	P2-49	GND	–	–	–	GND	–
GND	P2-50	GND	–	TX3_P	AB22	GND	–
–	P2-51	–	–	TX7_P	K22	–	–
–	P2-52	–	–	TX3_N	AB21	–	–
–	P2-53	–	–	TX7_N	K21	–	–
–	P2-54	–	–	–	–	–	–
GND	P2-55	GND	–	–	–	–	–
GND	P2-56	GND	–	–	–	–	–
–	P2-57	–	–	–	–	–	–
–	P2-58	–	–	–	–	–	–
–	P2-59	–	–	–	–	–	–
–	P2-60	–	–	–	–	–	–
VCC33	P2-61	VCC33	–	–	–	V_3P3V	–
VCC33	P2-62	VCC33	–	–	–	V_3P3V	–
–	P2-63	–	–	–	–	–	–
–	P2-64	–	–	–	–	–	–
–	P2-65	–	–	–	–	–	–

continues on next page

Table 3 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
–	P2-66	–	–	–	–	–	–
–	P2-67	–	–	–	–	–	–
–	P2-68	–	–	–	–	–	–
–	P2-69	–	–	–	–	–	–
HPS_GPIO37	P2-70	HPS_GPIO37	A5	GPIO_E11	E11	GPIO_B19	B19
HPS_GPIO44	P2-71	HPS_GPIO44	B12	GPIO_F11	F11	GPIO_B20	B20
–	P2-72	–	–	–	–	–	–
–	P2-73	–	–	–	–	–	–
–	P2-74	–	–	–	–	–	–
VCC33	P2-75	VCC33	–	–	–	V_3P3V	–
VCC33	P2-76	VCC33	–	–	–	V_3P3V	–
VCC18	P2-77	VCCIO7B	B13	–	–	–	–
VCC25	P2-78	VCCPD7B	E17	–	–	–	–
HPS_GPIO33	P2-79	HPS_GPIO33	A6	GPIO_E14	E14	–	–
HPS_GPIO27	P2-80	HPS_GPIO27	A9	GPIO_L7	L7	–	–
USB_DIR	P2-81	HPS_GPIO31	A7	–	–	MSS_IO15	F1
USB_D6	P2-82	HPS_GPIO24	J12	–	–	MSS_IO24	F6
USB_CLK	P2-83	HPS_GPIO29	A8	–	–	MSS_IO14	G2
USB_D7	P2-84	HPS_GPIO25	A11	–	–	MSS_IO25	F3
USB_D4	P2-85	HPS_GPIO22	J13	–	–	MSS_IO22	D1
USB_D5	P2-86	HPS_GPIO23	A12	–	–	MSS_IO23	D2
USB_D1	P2-87	HPS_GPIO16	J14	–	–	MSS_IO19	E1
USB_NXT	P2-88	HPS_GPIO32	J16	–	–	MSS_IO16	G5
HPS_GPIO14	P2-89	HPS_GPIO14	J15	GPIO_C14	C14	–	–
HPS_GPIO21	P2-90	HPS_GPIO21	A13	GPIO_M7	M7	–	–
HPS_GPIO28	P2-91	HPS_GPIO28	D15	–	BOOT- MODE	–	–
HPS_GPIO34	P2-92	HPS_GPIO34	C14	GPIO_D14	D14	–	–
HPS_GPIO26	P2-93	HPS_GPIO26	C15	GPIO_K4	K4	–	–
HPS_GPIO19	P2-94	HPS_GPIO19	A14	GPIO_L6	L6	–	–
USB_STP	P2-95	HPS_GPIO30	H16	–	–	MSS_IO17	G4
HPS_GPIO35	P2-96	HPS_GPIO35	B14	GPIO_C15	C15	–	–
HPS_GPIO20	P2-97	HPS_GPIO20	E16	GPIO_K5	K5	–	–
USB_D2	P2-98	HPS_GPIO17	A15	–	–	MSS_IO20	G3
USB_D3	P2-99	HPS_GPIO18	D17	–	–	MSS_IO21	F5
USB_D0	P2-100	HPS_GPIO15	A16	–	–	MSS_IO18	F2
VCC18	P2-101	VCCIO7B	B13	–	–	–	–
VCC25	P2-102	VCCPD7B	E17	–	–	–	–
VCC33	P2-103	VCCIO7D	D6	–	–	–	–
VCC33	P2-104	VCCPD7D	E13	–	–	–	–
EMAC0_TXD3	P2-105	HPS_GPIO4	C4	ETH0_TXD3	H13	ETH0_TXD3	G15
EMAC0_TXD0	P2-106	HPS_GPIO1	C10	ETH0_TXD0	C16	ETH0_TXD0	G14
EMAC0_TXD1	P2-107	HPS_GPIO2	F5	ETH0_TXD1	A16	ETH0_TXD1	F15
EMAC0_TXD2	P2-108	HPS_GPIO3	C9	ETH0_TXD2	A15	ETH0_TXD2	H15
EMAC0_RXD3	P2-109	HPS_GPIO13	D5	ETH0_RXD3	D16	ETH0_RXD3	D13
EMAC0_RXD0	P2-110	HPS_GPIO5	C8	ETH0_RXD0	G15	ETH0_RXD0	D22
EMAC0_RXD2	P2-111	HPS_GPIO12	E5	ETH0_RXD2	D17	ETH0_RXD2	D14

continues on next page

Table 3 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
EMAC0_MDC	P2-112	HPS_GPIO7	C7	ETH0_MDC	B15	ETH0_MDC	B15
EMAC0_TX_CLK	P2-113	HPS_GPIO0	E4	ETH0_GTXCLK	B14	ETH0_GTXCLK	G17
EMAC0_TX_CTL	P2-114	HPS_GPIO9	C6	ETH0_TX_EN	C17	ETH0_TX_EN	A15
EMAC0_MDIO	P2-115	HPS_GPIO6	D4	ETH0_MDIO	A17	ETH0_MDIO	H17
EMAC0_RXD1	P2-116	HPS_GPIO11	C5	ETH0_RXD1	H15	ETH0_RXD1	C22
EMAC0_RX_CTL	P2-117	HPS_GPIO8	F4	ETH0_RX_DV	E16	ETH0_RX_DV	B13
EMAC0_RX_CLK	P2-118	HPS_GPIO10	G4	ETH0_RXC	G14	ETH0_RXC	E15
VCC33	P2-119	VCCIO7D	D6	–	–	V_3P3V	–
VCC33	P2-120	VCCPD7D	E13	–	–	V_3P3V	–
HPS_GPIO64	P2-121	HPS_GPIO64	B16	GPIO_N7	N7	GPIO_A21	A21
HPS_GPIO59	P2-122	HPS_GPIO59	B18	GPIO_M4	M4	–	–
HPS_GPIO66	P2-123	HPS_GPIO66	C16	GPIO_N5	N5	GPIO_A20	A20
LCD_T_INT	P2-124	HPS_GPIO57	A18	–	–	GPIO_B21	B21
HPS_GPIO58	P2-125	HPS_GPIO58	C17	GPIO_L3	L3	–	–
I2C0_SDA	P2-126	HPS_GPIO55	A19	I2C1_SDA	H6	MSS_IO27	B1
HPS_GPIO63	P2-127	HPS_GPIO63	C19	GPIO_N6	N6	GPIO_C19	C19
HPS_GPIO65	P2-128	HPS_GPIO65	B19	GPIO_M9	M9	GPIO_B22	B22
CAN0_TX	P2-129	HPS_GPIO62	H17	CAN0_TX	F17	MSS_IO31	E4
CAN1_RX	P2-130	HPS_GPIO53	A20	CAN1_RX	F15	MSS_IO29	C2
HPS_GPIO52	P2-131	HPS_GPIO52	K18	GPIO_F13	F13	GPIO_D21	D21
UART0_TX	P2-132	HPS_GPIO50	B21	UART0_TX	K8	MSS_IO36	E3
HPS_GPIO60	P2-133	HPS_GPIO60	J17	GPIO_M5	M5	–	–
HPS_GPIO51	P2-134	HPS_GPIO51	A21	GPIO_M3	M3	GPIO_D20	D20
CAN1_TX	P2-135	HPS_GPIO54	J18	CAN1_TX	F16	MSS_IO28	D3
HPS_GPIO48	P2-136	HPS_GPIO48	C21	GPIO_M8	M8	GPIO_C20	C20
CAN0_RX	P2-137	HPS_GPIO61	A17	CAN0_RX	G17	MSS_IO32	B2
UART0_RX	P2-138	HPS_GPIO49	A22	UART0_RX	J8	MSS_IO35	A3
I2C0_SCL	P2-139	HPS_GPIO56	C18	I2C1_SCL	H5	MSS_IO26	C1
VCC33	P2-140	VCC33	–	–	–	V_3P3V	–
VCC33	P2-141	VCC33	–	–	–	V_3P3V	–
VCC33	P2-142	VCC33	–	–	–	–	–
HPS_GPI10	P2-143	HPS_GPI10	U15	GPIO_E13	E13	–	–
HPS_GPI1	P2-144	HPS_GPI1	K27	GPIO_J3	J3	–	–
HPS_GPI11	P2-145	HPS_GPI11	U16	GPIO_D13	D13	–	–
HPS_GPI5	P2-146	HPS_GPI5	P26	GPIO_E10	E10	–	–
HPS_GPI7	P2-147	HPS_GPI7	T16	GPIO_F12	F12	–	–
HPS_GPI4	P2-148	HPS_GPI4	R28	–	–	–	–
HPS_GPI2	P2-149	HPS_GPI2	R20	GPIO_D11	D11	–	–
HPS_GPI6	P2-150	HPS_GPI6	T17	GPIO_K3	K3	–	–
HPS_GPI13	P2-151	HPS_GPI13	V24	–	–	–	–
HPS_GPI12	P2-152	HPS_GPI12	AC27	GPIO_G12	G12	–	–
HPS_GPI8	P2-153	HPS_GPI8	Y28	GPIO_D12	D12	MSS_IO37	D4
HPS_GPI3	P2-154	HPS_GPI3	R21	GPIO_G13	G13	MSS_IO34	B3
HPS_GPI9	P2-155	HPS_GPI9	Y26	GPIO_F10	F10	MSS_IO30	E5
HPS_GPI0	P2-156	HPS_GPI0	M25	GPIO_L8	L8	MSS_IO33	A2
VCC33	P2-157	VCC33	–	–	–	V_3P3V	–
VCC33	P2-158	VCC33	–	–	–	V_3P3V	–

continues on next page

Table 3 – continued from previous page

MXXEVP		MCV		M100PF		M100PFS	
Function	Con- nector	Function	FPGA Pin	Function	FPGA Pin	Function	FPGA Pin
HPS_RST_N	P2-159	HPS_RSTN	A23	POR_N	–	POR_N	–
CLKEXT_P	P2-160	CLKEXTA	–	OCLK_P	–	OCLK_P	–
VCCBAT	P2-161	VCCBAT	D7	–	–	V_3P3V	–
CLKEXT_N	P2-162	CLKEXTB	–	OCLK_N	–	OCLK_N	–
VCC33	P2-163	VCC33	–	–	–	V_3P3V	–
VCC25	P2-164	IDTV4	–	–	–	–	–
IDT_SDAT	P2-165	IDT_SDAT	–	–	–	PMIC_SDA	–
CLKEXTCD_P	P2-166	–	–	–	–	–	–
IDT_SCLK	P2-167	IDT_SCLK	–	–	–	PMIC_SCL	–
CLKEXTCD_N	P2-168	–	–	–	–	–	–
IDT_SEL0	P2-169	PROG	–	–	–	PMIC_TP	–
VCC25	P2-170	–	–	–	–	–	–
IDT_SEL1	P2-171	–	–	–	–	PLL_AC1	–
CLKEXTF	P2-172	CLKEXTF	–	GPIO_L5	L5	GPIO_A13	A13
IDT_SEL2	P2-173	–	–	–	–	PLL_AC2	–
CLK25_PHY0	P2-174	CLKEXTE	–	CLK25_3	–	CLK25_O	–
VCC33	P2-175	VCC33	–	–	–	V_3P3V	–
VCC33	P2-176	VCC33	–	–	–	V_3P3V	–
VCC33	P2-177	VCC33	–	–	–	V_3P3V	–
VCC33	P2-178	VCC33	–	–	–	V_3P3V	–
VCC33	P2-179	VCC33	–	–	–	V_3P3V	–
VCC33	P2-180	VCC33	–	–	–	V_3P3V	–
GND	P2-181	GND	–	–	–	GND	–
GND	P2-182	GND	–	–	–	GND	–
GND	P2-183	GND	–	–	–	GND	–
GND	P2-184	GND	–	–	–	GND	–
GND	P2-185	GND	–	–	–	GND	–
GND	P2-186	GND	–	–	–	GND	–
GND	P2-187	GND	–	–	–	GND	–
GND	P2-188	GND	–	–	–	GND	–
GND	P2-189	GND	–	–	–	GND	–
GND	P2-190	GND	–	–	–	GND	–
GND	P2-191	GND	–	–	–	GND	–
GND	P2-192	GND	–	–	–	GND	–