MX10 Hardware Manual

Release 1

ARIES Embedded GmbH

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
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- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
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- Do not attempt to open the device.
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- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	27.10.2017	bnh	Initial creation

CHAPTER

TWO

OVERVIEW

2.1 MX10 System on Module

The MX10 module is a non-volatile and fully programmable solution based on Altera's MAX 10 FPGA by Intel. The MX10 incorporates advantages of MAX 10 FPGA such as instant-on functionality, integrated analog-to-digital converters (ADCs) and dual configuration flash. The module delivers full-featured FPGA capabilities including support for various soft-core CPUs, advanced DSP and video-processing algorithms as well as external DDR3 controllers.

Fig. 2.1: MX10 SoM

Its integrated and configurable Power management circuitry provides a wide range of supply voltages, which can be accessed via the MxM2-Card Edge connector. MX10 can be bought with an installed single cell charge controller for Lithium cells, which enables usage in mobile applications.

2.2 Block Diagram

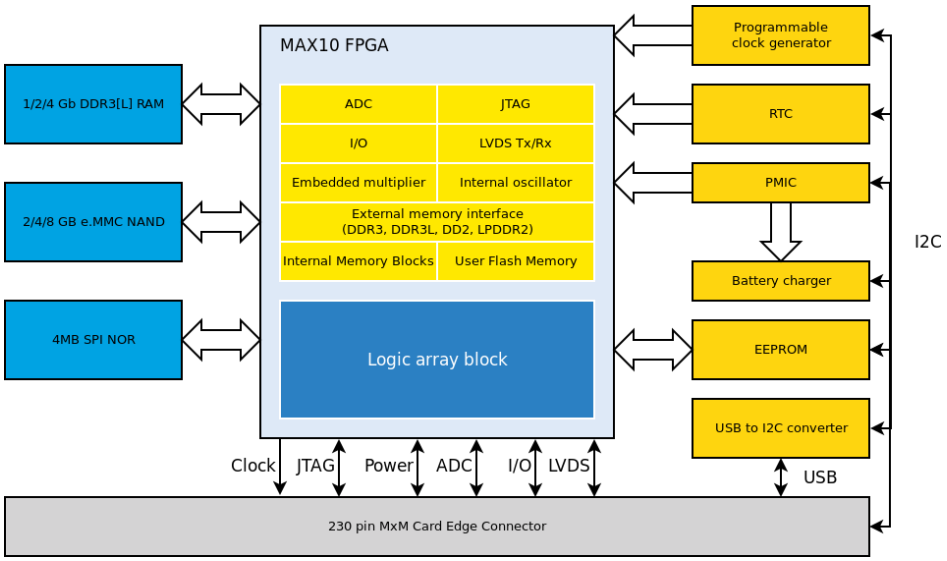

Fig. 2.2: MX10 SoM blockdiagram

Picture Fig. 2.2 shows the modules main devices along with the interconnection amongst themselves.

2.3 Feature Set

The MX10 System on Module features:

- MAX 10 FPGA in F256 package
- wide range of MAX 10 devices: from 10M04DC to 10M50DA
- optional 4 MB SPI NOR
- optional 4 GB e.MMC
- optional 128/256/512M x8 DDR3 DRAM (for 10M 16/25/40/50 FPGAs)
- optional programmable clock generator and PLL, with optional external reference input
- optional RTC with external battery backup
- optional Li-Ion/Li-Po charger
- 178 FPGA GPIO pins, including 13 LVDS transmitters and 54 receivers
- programmable high-efficient PMIC, FPGA IO voltages are configurable
- MxM2 Card Edge Connector
- Size: 70mm x 35mm

2.4 Available Configurations

MX10 is available in different configurations, which are shown in the following table.

	MX10				
	Ultimate	Standard		Custom	Light
Model name	MX10-U	MX10-S16	MX10-S8	MX10-C	MX10-L
FPGA	10M50DA F256	10M16DA F256	10M08DA F256	10MxxDyF256 04..50, C/A	10M04DC F256
ADC	2	1	1	0/1/2	0
RAM	512 MiB	128 MiB	—	128/256/512	—
Clock	25MHz XO, PLL IDT 5P49V5923	25MHz XO, PLL IDT 5P49V5923	25MHz XO	25MHz XO, PLL opt.	25MHz XO
SPI NOR	4 MiB	—	—	0/2/4 MiB	—
e.MMC	4 GiB	4 GiB	—	0..64 GiB	—
RTC	MCP794xx	—	—	Optional	—
GPIO LVDS Tx/Rx	100 (?) 13/16 (?)				
I/O voltage	programmable 1.8/2.5/3.0/3.3V				
Li-Pol charger	Yes (LTC4155)	—		Optional (LTC4155)	—

The corresponding part number is listed in the table below. Please feel free to contact us, if you wish to buy a custom configuration.

Model	Part number
MX10-U	MX10-50DABAC610
MX10-S16	MX10-16DAB0A600
MX10-S8	MX10-08DA000800
MX10-L	MX10-04DC000800

2.5 Dimensions

The size of a Mx10 Module is shown in figure Fig. 2.3.

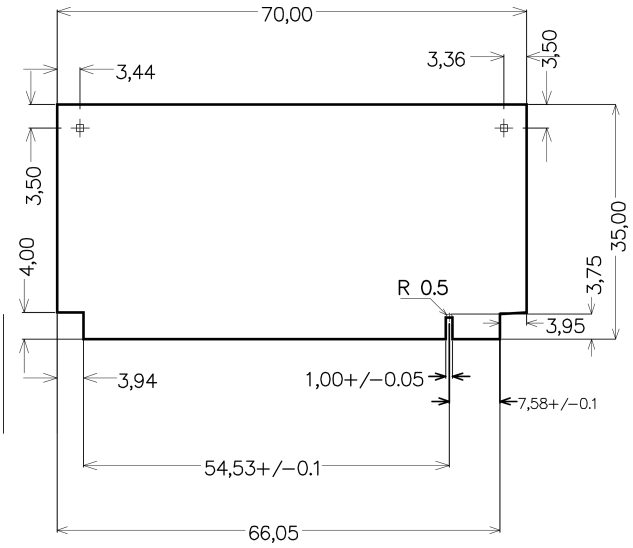

Fig. 2.3: Dimensions of the Mx10 SoM

2.6 Handling Recommendations

Inserting the module into a baseboard might require a certain mechanical force. To avoid mechanical damage to the components populated on MX10 it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in figure Fig. 2.4.

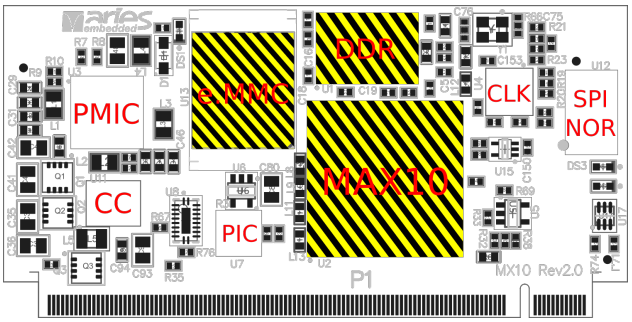

Fig. 2.4: BGA component location on top side of Mx10 SoM

2.7 Parts Location

Pictures Fig. 2.5 and Fig. 2.6 show the location of every part on the top and bottom side of the module.

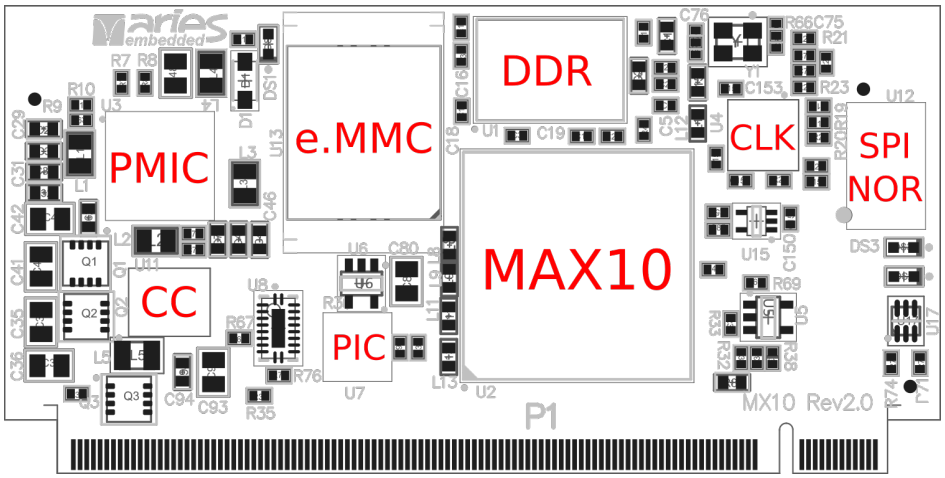

Fig. 2.5: Localization of parts on top side of Mx10 SoM

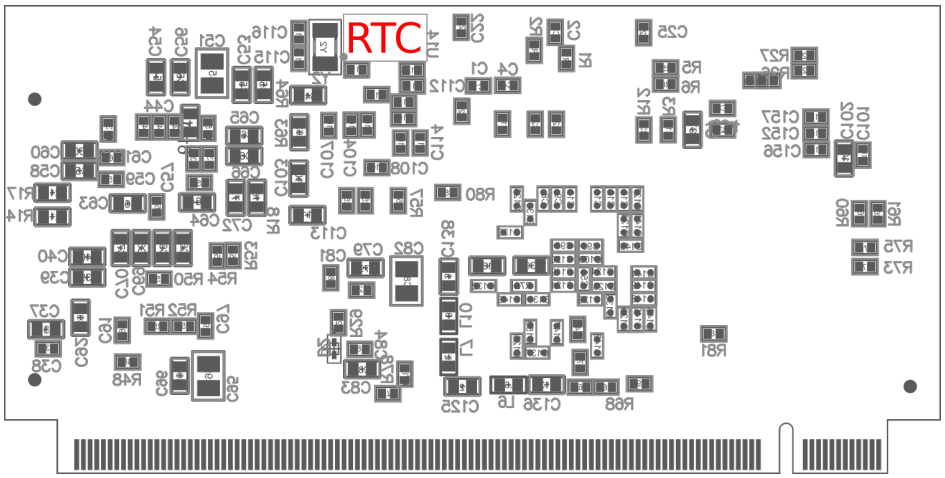

Fig. 2.6: Localization of parts on bottom side of the Mx10 SoM

CHAPTER

THREE

RESOURCES

3.1 MAX10 FPGA

The MX10 SoM was developed around Intels MAX10 FPGA family in the F256 package. These FPGAs provide high processing capabilities within a low cost, small form factor programmable logic device. The MAX10 devices in use, provide dual configuration flash storage and thus enable dynamical switching between two FPGA configurations on a single chip. Furthermore, MAX10 provides up to two ADC units for analog signal conversion and external memeory interfaces. Refer to *Related Links* for further information on the different MAX10 devices.

Table 3.1 describes the FPGAs signals on the module, along with the connections to the MxM2 connector.

FPGA Bank	FPGA Pin	Module connection	Signal on connector	Connector Pin
1A	F5		ADC1_IN1	185
1A	C4		ADC2_IN1	168
1A	F4		ADC1_IN2	183
1A	C3		ADC2_IN8	170
1A	H5		ADC1_IN3	181
1A	E3		ADC2_IN3	172
1A	G5		ADC1_IN4	179
1A	F2		ADC2_IN4	174
1A	G2		ADC1_IN5	173
1A	C2		ADC2_IN5	180
1A	F1		ADC1_IN6	171
1A	B2		ADC2_IN6	182
1A	E1		ADC1_IN7	167
1A	B1		ADC2_IN7	184
1A	D1		ADC1_IN8	169
1A	C1		ADC2_IN2	186
1B	G6		JTAG_EN	198
1B	H2		JTAG_TMS	194
1B	J1	RTC_MFP		
1B	H3		JTAG_TCK	197
1B	G1		JTAG_TDI	195
1B	H1		JTAG_TDO	196
1B	J5	LV_RX		
1B	H6	LV_TX		
1B	J3	LV_SCL		
1B	J2	LV_SDA		
2	M3	CLK0_N		10

Continued on next page

Table 3.1 – continued from previous page

FPGA Bank	FPGA Pin	Module connection	Signal on connector	Connector Pin
2	L1	PMIC_INTN		
2	L3	CLK0_P		12
2	K2	PMIC_STNDBY		
2	K6		IO2_K6	34
2	M2	PMIC_SDVSEL		
2	J6		IO2_J6	32
2	L2	SPI_MOSI		
2	N2	DPCLK0		143
2	M1	CLK_SEL		
2	P1	DPCLK1		104
2	N1	SPI_SSN		
2	K5	SPI_SCLK		
2	L6	SPI_MISO		
2	N3	CLK_SDOE		
2	N4	CHRG_INTN		
3	P4		IO3_TX1_N	109
3	P2		IO3_RX2_N	82
3	N5		IO3_TX1_P	107
3	R1		IO3_RX2_P	84
3	M6		IO3_TX3_N	101
3	R3		IO3_RX4_N	80
3	L7		IO3_TX3_P	103
3	R2		IO3_RX4_P	78
3	R4		IO3_TX5_N	97
3	T3		IO3_RX6_N	74
3	P5		IO3_TX5_P	99
3	T2		IO3_RX6_P	72
3	R6		IO3_TX13_N	83
3	T5		IO3_RX14_N	70
3	R5		IO3_TX13_P	81
3	T4		IO3_RX14_P	68
3	M7		IO3_TX15_N	91
3	T7		IO3_T7	204
3	L8		IO3_TX15_P	93
3	T6		IO3_T6	28
3	R7		IO3_TX16_N	87
3	T8		IO3_RX17_N	57
3	P6		IO3_TX16_P	89
3	R8		IO3_RX17_P	59
3	P9		IO3_TX18_N	73
3	T9		IO3_RX19_N	51
3	P8		IO3_TX18_P	71
3	R9		IO3_RX19_P	53
3	M8		IO3_TX20_N	69
3	M9		IO3_TX20_P	67
3	T11		IO3_TX22_N	79
3	R10		IO3_TX22_P	77
4	P10		IO4_TX34_N	64
4	R11		IO3_RX35_N	90

Continued on next page

Table 3.1 – continued from previous page

FPGA Bank	FPGA Pin	Module connection	Signal on connector	Connector Pin
4	P11		IO4_TX34_P	62
4	R12		IO3_RX35_P	88
4	M10		IO4_TX36_N	60
4	T13		IO4_T13	206
4	L9		IO4_TX36_P	58
4	T12		IO4_T12	30
4	P13		IO4_TX37_N	63
4	P12		IO4_TX37_P	61
4	M11		IO4_TX57_N	54
4	L10		IO4_TX57_P	52
5	P14	Pullup to VCC_DDR		
5	T14	DDR_ADDR14		
5	R14	Pulldown to GND		
5	T15	DDR_ADDR00		
5	L11	DDR_ADDR12		
5	L12	DDR_ADDR11		
5	N14	DDR_ADDR10		
5	M15	DDR_ADDR09		
5	P15	DDR_ADDR08		
5	M14	DDR_ADDR07		
5	N16	DDR_ADDR06		
5	R15	DDR_ADDR05		
5	P16	DDR_ADDR04		
5	R16			
5	K11	DDR_ADDR03		
5	K12	DDR_ADDR02		
5	K14	DDR_ADDR01		
5	M16	GND		
5	L15	GND		
5	L16	GND		
6	J11	DDR_ADDR13		
6	J14	DDR_ODT		
6	J12	CLK25_1		
6	K15	DDR_RESET_N		
6	J15	DDR_WE_N		
6	H15	DDR_CAS_N		
6	J16	DDR_RAS_N		
6	H16	DDR_CS_N		
6	D16	DDR_CKE		
6	C16	DDR_BA2		
6	H11	DDR_DATA00		
6	H12	DDR_DATA01		
6	G14	DDR_DATA02		
6	G16	DDR_DATA03		
6	G15	DDR_DM		
6	F16	DDR_DATA04		
6	G11	DDR_DQS_P		
6	B15	DDR_VREF		
6	G12	DDR_DQS_N		

Continued on next page

Table 3.1 – continued from previous page

FPGA Bank	FPGA Pin	Module connection	Signal on connector	Connector Pin
6	B16	DDR_BA1		
6	F14	DDR_DATA05		
6	E15	DDR_DATA06		
6	E14	DDR_DATA07		
6	E16	GND		
6	D14	DDR_BA0		
6	D15	DDR_CLK_P		
6	C14	DDR_ADDR15		
6	C15	DDR_CLK_N		
7	D12	EMMC_DAT0		
7	C13	EMMC_DAT1		
7	E11	EMMC_DAT2		
7	C12	EMMC_DAT3		
7	F11	EMMC_DAT4		
7	A14	EMMC_DAT5		
7	F12	EMMC_DAT6		
7	A15		IO7_A15	203
7	F10	EMMC_DAT6		
7	E10	EMMC_DAT7		
7	B13	EMMC_CLK		
7	A13	EMMC_RSTN		
8	D9		IO8_D9	31
8	C9		IO8_C9	29
8	F9	CLK_O1		
8	B12		IO8_RX41_P	120
8	E9		IO8_E9	27
8	B11		IO8_RX41_N	118
8	C10		IO8_C10	127
8	A11		IO8_RX43_P	122
8	B10		DEV_CLRN	164
8	A12		IO8_RX43_N	124
8	B8		IO8_RX44_P	114
8	A10		IO8_A10	113
8	B7		IO8_RX44_N	106
8	A9		IO8_A9	205
8	F8		CFG_SEL	199
8	B9		IO8_RX45_P	130
8	E8	NCONFIG	NCONFIG	193
8	A8		IO8_RX45_N	128
8	B6		IO8_RX46_P	94
8	A7		IO8_RX47_P	100
8	C6		IO8_RX46_N	98
8	A6		IO8_RX47_N	102
8	B5		IO8_B5	111
8	B4		IO8_RX49_P	119
8	C5	CRC_ERR		
8	A5		IO8_RX49_N	117
8	F7	NSTATUS		
8	A3		IO8_RX51_P	121

Continued on next page

Table 3.1 – continued from previous page

FPGA Bank	FPGA Pin	Module connection	Signal on connector	Connector Pin
8	E7	CONF_DONE		
8	A2		IO8_RX51_N	123
8	B3		IO8_RX52_P	134
8	A4		IO8_RX52_N	132
	D2		AIN1	177
	F3		AIN2	178

3.2 I2C bus

An I2C bus connects the major components of the Module. The available I2C devices along with their address can be found in the following table.

To gain external access to the bus, MX10 has a programmable PIC16F1454, which acts as a USB to I2C converter. Its USB *D+* and *D-* signals are available on the MxM2 onnector. No external components are needed on a baseboard to provide USB access. Nevertheless, some ESD protection within the USB data lines is advised.

I2C address	Device	Description
0x08	PF3000	PMIC
0x09	LTC4155	Charge controller
0x57	MCP794xx	EEPROM
0x6A	5P49V5623	Programmable clock generator
0x6F	MCP794xx	RTC

3.3 Programmable Clock Generator and PLL

Some configurations of MX10 house an IDT VersaClock 5 5P49V5923 I2C programmable clock generator with external 25 MHz crystal. Furthermore, it is possible to use an external LVDS signal *CLK_REF_P* and *CLK_REF_N* as reference clock. Configurations may be stored in on-chip One-Time Programmable (OTP) memory or changed using the I2C interface. The selection between reference clock and internal crystal oszillator (wired to the 25MHz crystal) can be done via the *CLK_SEL* signal.

CLK_SDOE can be configured to either shutdown the PLL or enable/disable the outputs. Refer to 5P49V5923's datasheet for further information.

Modules without clock generator have an MEMS or XO oscillator installed, which provides a single 25 MHz reference clock to the FPGAs internal PLL and/or global clock input. It is also available at the MxM2 connector at signal *CLK25_0*.

A differential clock input to CLK0 of the FPGA is available at the MxM2 connector, as well.

Signal	Connector pin	FPGA function	FPGA pin	
CLK_REF_P	6			positive reference input
CLK_REF_N	4			negative reference input
CLK_SEL		IO_2_M1	M1	clock selection
CLK_SDOE		IO_2_N3	N3	Output enable/disable
CLK_O2	3			configurable clock output
CLK_O1		IO_8_F9	F9	configurable clock output
CLK25_0	7			25MHz clock output
CLK25_1		IO_6_J12	J12	25MHz clock output
CLK0_P	12	CLK0N	L3	external clock input for the FPGA
CLK0_N	10	CLK0P	M3	external clock input for the FPGA

3.4 Realtime clock/calendar and EEPROM

MX10 has a MCP794xx realtime clock/calendar with integrated EEPROM and external 32.768 kHz crystal. Access to clock and EEPROM is possible via I2C. In case of a power failure, this device can automatically switch to an external power source (e.g. a lithium cell) if provided to the MX10 module on signal *LI_CELL*, to keep its configuration after power down.

Signal	FPGA function	FPGA pin	
RTC_MFP	IO_1B_J1	J1	Multifunction Pin

3.5 4MB NOR Flash

Connected via SPI to the FPGA, some configurations of MX10 are available with an installed 4MB AT25DF321A NOR flash with a supply voltage of 3.3V. It is capable of 100,000 program/erase cycles and has a data retention of 20 years.

This flash device provides 64 sectors of 64-kByte each. Every sector can be locked/unlocked independently and even set to read-only permanently.

Signal	FPGA function	FPGA pin
SPI_SSN	IO_2_N1	N1
SPI_MISO	IO_2_L6	L6
SPI_MOSI	IO_2_L2	L2
SPI_CLK	IO_2_K5	K5

3.6 4GB e.MMC NAND Flash

MX10 has the capability to support a THGBM4G5DIHBAIR 4GB e.MMC NAND Flash device. Its connection to the FPGA is described in the following table:

Signal	FPGA function	FPGA pin
EMMC_DAT0	IO_7_D12	D12
EMMC_DAT1	IO_7_C13	C13
EMMC_DAT2	IO_7_E11	E11
EMMC_DAT3	IO_7_C12	C12
EMMC_DAT4	IO_7_F11	F11
EMMC_DAT5	IO_7_A14	A14
EMMC_DAT6	IO_7_F12	F12
EMMC_DAT7	IO_7_F10	F10
EMMC_CMD	IO_7_E10	E10
EMMC_CLK	IO_7_B13	B13
EMMC_RSTN	IO_7_A13	A13

3.7 DDR3[L] RAM

MX10 can optionally provide up to 4GB DDR3[L] RAM (only for 10M16/25/40/50). The 1GB module in use, is SAMSUNGs K4B1G08461. Pin-compatible options with higher capacity are also available. The connection between the SDRAM Module and MAX10 FPGA is described in the following table.

Signal	FPGA function	FPGA pin
DDR_ADDR00	IO_5_T15	T15
DDR_ADDR01	IO_5_K14	K14
DDR_ADDR02	IO_5_K12	K12
DDR_ADDR03	IO_5_K11	K11
DDR_ADDR04	IO_5_P16	P16
DDR_ADDR05	IO_5_R15	R15
DDR_ADDR06	IO_5_N16	N16
DDR_ADDR07	IO_5_M14	M14
DDR_ADDR08	IO_5_P15	P15
DDR_ADDR09	IO_5_M15	M15
DDR_ADDR10	IO_5_N14	N14
DDR_ADDR11	IO_5_L12	L12
DDR_ADDR12	IO_5_L11	L11
DDR_ADDR13	IO_6_J11	J11
DDR_ADDR14	IO_5_T14	T14
DDR_ADDR15	IO_6_C14	C14
DDR_DATA00	IO_6_H11	H11
DDR_DATA01	IO_6_H12	H12
DDR_DATA02	IO_6_G14	G14
DDR_DATA03	IO_6_G16	G16
DDR_DATA04	IO_6_F16	F16
DDR_DATA05	IO_6_F14	F14
DDR_DATA06	IO_6_E15	E15
DDR_DATA07	IO_6_E14	E14
DDR_BA0	IO_6_D14	D14
DDR_BA1	IO_6_B16	B16
DDR_BA2	IO_6_C16	C16

Continued on next page

Table 3.2 – continued from previous page

Signal	FPGA function	FPGA pin
DDR_CS_N	IO_6_H16	H16
DDR_RAS_N	IO_6_J16	J16
DDR_CAS_N	IO_6_H15	H15
DDR_WE_N	IO_6_J15	J15
DDR_DM	IO_6_G15	G15
DDR_CKE	IO_6_D16	D16
DDR_RESET_N	IO_6_K15	K15
DDR_ODT	IO_6_J14	J14
DDR_DQS_P	IO_6_G11	G11
DDR_DQS_N	IO_6_G12	G12

3.8 PMIC

To supply the MX10 SoM with the different needed voltages, the SoM houses a MC32PF3000A0EP programmable power management integrated circuit (PMIC). It incorporates four adjustable high efficieny buck regulaters, six adjustable general purpose linear regulators and can be controlled via the I2C bus. Besides this, it provides coin cell charging and always-on power supply for the RTC as well es reference voltage for DDR.

Signal	Connector pin	FPGA function	FPGA pin	
PMIC_INTN		IO_2_L1	L1	Interrupt signal to FPGA
PMIC_SDVSEL		IO_2_M2	M2	VCC_SD voltage selection
PMIC_STNDBY		IO_2_K2	K2	Standby input signal
PMIC_VOTP	220			Supply to program OTP fuses
PWR_SW	222			Power ON/OFF input

The following table should give an insight into the output voltages, generated by PMIC.

PMIC Output	MAX10 power rail	Default Voltage	Possible voltages	Imax
SW1A/1B	VCC	1.2V	0.7..1.425V	2.75A
SW2	VCCIO3..4	2.5 or 3.3V	1.5..1.85V 2.5..3.3V	1.25A
SW3	VCCIO5..6	1.5V	0.9..1.65V	1.5A
LDO1	VCCIO1B	2.5V	1.8..3.3V	100mA
LDO2	VCCD_PLL, VCCINT	1.2V	0.8..1.55V	250mA
LDO3	VCCIO8	3.3V	1.8..3.3V	100mA
LDO4	VCCA, VCCA_ADC, VCCIO1A	2.5V	1.8..3.3V	350mA
V33	VCCIO2	3.3V	2.85..3.3V	350mA
VCC_SD	VCCIO7	1.8V	1.8..1.85V 2.85..3.3V	100mA

3.9 Lithium-Ion/Polymer battery charger

Some configurations of MX10 provide a LT4155 Lithium-Ion/Polymer single cell battery charger. It features a NTC Thermistor input for battery protection and can be controlled via I2C. The output signal *CHGOUT* and the NTC signal are provided to the MxM2 connector. The *CHRG_INTN* output signal is routed to FPGA signal *IO_2_N4*. It can be set to trigger an interrupt at certain events like a faulty cell. To activate and mask these events, it is necessary to program the LT4155's register 0x06 via I2C.

Modules with battery charger can be run from a Lithium-Ion/Polymer cell.

Connector Pin	Signal	Function
210	CHGOUT	Charger output
212		
214		
200	NTC	Thermistor input

Figure Fig. 3.1 shows the battery charging circuit.

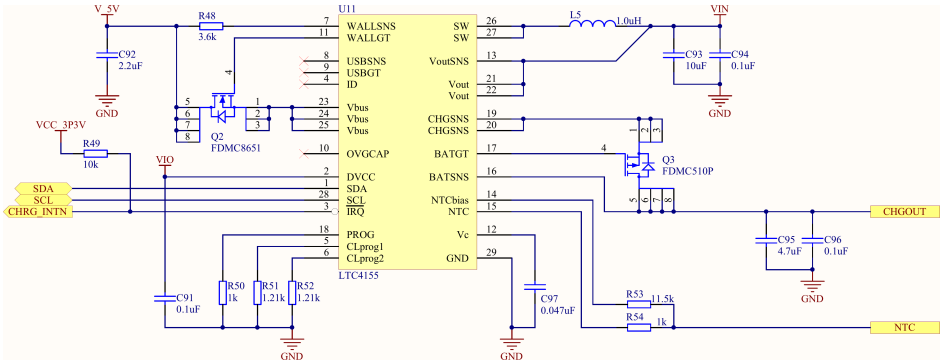

Fig. 3.1: Schematic extract showing the charging circuitry

3.10 MxM 2 Connector

For space efficient connection to a baseboard, MX10 uses a MxM2 Card Edge Connector. Its full pinout is provided in the following table.

Function	FPGA pin	Pin	Pin	FPGA pin	Function
GND		1	2		GND
CLK_O2		3	4		CLK_REF_N
GND		5	6		CLK_REF_P
CLK25_0		7	8		GND
GND		9	10	M3	CLK0_N
NC		11	12	L3	CLK0_P
GND		13	14		GND
NC		15	16		NC
NC		17	18		NC
NC		19	20		NC
NC		21	22		NC
GND		23	24		GND
GND		25	26		GND
IO8_E9	E9	27	28	T6	IO3_T6
IO8_C9	C9	29	30	T12	IO4_T12
IO8_D9	D9	31	32	J6	IO2_J6
NC		33	34	K6	IO2_K6
GND		35	36		GND
NC		37	38		NC
NC		39	40		NC

Continued on next page

Table 3.3 – continued from previous page

Function	FPGA pin	Pin	Pin	FPGA pin	Function
NC		41	42		NC
NC		43	44		NC
GND		45	46		GND
NC		47	48		NC
NC		49	50		NC
IO3_RX19_N	T9	51	52	L10	IO4_TX57_P
IO3_RX19_P	R9	53	54	M11	IO4_TX57_N
GND		55	56		GND
IO3_RX17_N	T8	57	58	L9	IO4_TX36_P
IO3_RX17_P	R8	59	60	M10	IO4_TX36_N
IO4_TX37_P	P12	61	62	P11	IO4_TX34_P
IO4_TX37_N	P13	63	64	P10	IO4_TX34_N
GND		65	66		GND
IO3_TX20_P	M9	67	68	T4	IO3_RX14_P
IO3_TX20_N	M8	69	70	T5	IO3_RX14_N
IO3_TX18_P	P8	71	72	T2	IO3_RX6_P
IO3_TX18_N	P9	73	74	T3	IO3_RX6_N
GND		75	76		GND
IO3_TX22_P	R10	77	78	R2	IO3_RX4_P
IO3_TX22_N	T11	79	80	R3	IO3_RX4_N
IO3_TX13_P	R5	81	82	P2	IO3_RX2_N
IO3_TX13_N	R6	83	84	R1	IO3_RX2_P
GND		85	86		GND
IO3_TX16_N	R7	87	88	R12	IO3_RX35_P
IO3_TX16_P	P6	89	90	R11	IO3_RX35_N
IO3_TX15_N	M7	91	92		NC
IO3_TX15_P	L8	93	94	B6	IO8_RX46_P
GND		95	96		GND
IO3_TX5_N	R4	97	98	C6	IO8_RX46_N
IO3_TX5_P	P5	99	100	A7	IO8_RX47_P
IO3_TX3_N	M6	101	102	A6	IO8_RX47_N
IO3_TX3_P	L7	103	104	P1	DPCLK1
GND		105	106	B7	IO8_RX44_N
IO3_TX1_P	N5	107	108		GND
IO3_TX1_N	P4	109	110		NC
IO8_B5	B5	111	112		GND
IO8_A10	A10	113	114	B8	IO8_RX44_P
GND		115	116		GND
IO8_RX49_N	A5	117	118	B11	IO8_RX41_N
IO8_RX49_P	B4	119	120	B12	IO8_RX41_P
IO8_RX51_P	A3	121	122	A11	IO8_RX43_P
IO8_RX51_N	A2	123	124	A12	IO8_RX43_N
GND		125	126		GND
IO8_C10	C10	127	128	A8	IO8_RX45_N
NC		129	130	B9	IO8_RX45_P
NC		131	132	A4	IO8_RX52_N
NC		133	134	B3	IO8_RX52_P
GND		135	136		GND
NC		137	138		NC

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Table 3.3 – continued from previous page

Function	FPGA pin	Pin	Pin	FPGA pin	Function
NC		139	140		NC
NC		141	142		NC
DPCLK0	N2	143	144		NC
GND		145	146		GND
NC		147	148		NC
NC		149	150		NC
SCL		151	152		SDA
GND		153	154		GND
USBD_D_P		155	156		NC
USBD_D_N		157	158		NC
NC		159	160		PIC_nRST
NC		161	162		PIC_DIS
VCCA_2P5V		163	164	B10	DEV_CLRN
REFGND		165	166		REFGND
ADC1_IN7	E1	167	168	C4	ADC2_IN1
ADC1_IN8	D1	169	170	C3	ADC2_IN8
ADC1_IN6	F1	171	172	E3	ADC2_IN3
ADC1_IN5	G2	173	174	F2	ADC2_IN4
REFGND		175	176		REFGND
AIN1	D2	177	178	F3	AIN2
ADC1_IN4	G5	179	180	C2	ADC2_IN5
ADC1_IN3	H5	181	182	B2	ADC2_IN6
ADC1_IN2	F4	183	184	B1	ADC2_IN7
ADC1_IN1	F5	185	186	C1	ADC2_IN2
REFGND		187	188		REFGND
VCC_USB		189	190		VCC_USB
VCC_USB		191	192		VCC_USB
NCONFIG	E8	193	194	H2	JTAG_TMS
JTAG_TDI	G1	195	196	H1	JTAG_TDO
JTAG_TCK	H3	197	198	G6	JTAG_EN
CFG_SEL	F8	199	200		NTC
GND		201	202		GND
IO7_A15	A15	203	204	T7	IO3_T7
IO8_A9	A9	205	206	T13	IO4_T13
GND		207	208		GND
V_5V		209	210		CHGOUT
V_5V		211	212		CHGOUT
V_5V		213	214		CHGOUT
GND		215	216		GND
VCC_IO		217	218		VCC_IO8
VCC_IO1B		219	220		PMIC_VOTP
RSTN		221	222		PWR_SW
VIO		223	224		GND
VCC_3P3V		225	226		LI_CELL
VIN		227	228		VIN
GND		229	230		GND

The following MxM connector is recommended for usage with Mx10 (refer to hyperlink 9 in the *Related Links* for detailed information):

Manufacturer	Part number	board-to-board distance Mx10 and Carrier Board	Overall height
Aces	88882-2D08	5,0mm	7,0mm

For interlocking the module with a carrier board, Mx10 has two holes for inserting M2.5 mounting screws.

CHAPTER

FOUR

POWER SUPPLY

4.1 Power inputs

MX10 Net name	MX10 Devices	Default Voltage	Voltage	Notes
V_5V	PMIC, charge controller, early power LDO		4.6..5.5V [4.35..5.5V]	Main MX10 power input [with optional charge controller]
LI_Cell	PMIC, RTC	3.0V	1.8..3.3V	Backup Li coin cell (e.g. CR2032, optional)

4.2 Battery in-/output

MX10 net name	MX10 Devices	Default Voltage	PMIC Voltages	Notes
CHGOUT	Charge Controller	3.7V	[2.8..4.2V]	1s Li-Pol battery (In/Out, optional) [Vlowbat..Vfloat]

CHGOUT is only available if a charge controller is installed on the module. If the module is running from a battery, its voltage is provided to *VIN*.

4.3 Power outputs

MX10 Net name	Default Voltage	PMIC Voltages	Imax	Notes
VCC_IO	2.5V or 3.3V	1.5..1.85V; 2.5..3.3V	1A	Power output for low-voltage (2.5..3.3V) devices
VCC_USB	5.0V	5.00..5.15V	600mA	Power output for 5V devices

4.4 Bank voltages

MAX10 FPGA Bank Number	MX10 Net name	MAX10 power rail	Default Voltage	Notes
1A	VCCA_2P5V	VCCIO1A	2.5V	
1B	VCC_IO1B	VCCIO1B	2.5V	JTAG, I2C and serial IO, VCCIO1B should be the same as VCC_IO1A (2.5V) if ADC is used
2	VCCIO_3P3V	VCCIO2	3.3V	
3, 4	VCC_IO	VCCIO3..4	2.5V or 3.3V	2.5V for LVDS I/O support
5, 6	VCC_DDR	VCCIO5..6	1.5V	
7	VCC_SD	VCCIO7	1.8V	
8	VCC_IO8	VCCIO8	3.3V	

4.5 Auxiliary in-/outputs

MX10 net name	MX10 Devices	Default Voltage	PMIC Voltages	Imax	Notes
VIN	PMIC		4.3..4.55V		Front-end LDO input or charge controller output
VIO	PIC16F1454, PMIC and charge controller I2C	3.3V		150mA	early power LDO output, pull-up for a power button

VIO provides an early 3.3V power supply with limited current capability. It is available even before the PMIC is operational.

VIN is the input signal to LDO1, LDO3 and LDO4 inside the PMIC. It is normally provided by the PMIC itself, but can be provided externally.

Important: This feature should be used carefully! Please contact us for further information on this subject, since there might be some modifications on the module needed!

CHAPTER

FIVE

RELATED LINKS

1. MAX10 FPGA overview: https://www.altera.com/products/fpga/max-series/max-10/overview.html
2. PIC16F1415: http://ww1.microchip.com/downloads/en/DeviceDoc/40001639B.pdf
3. Programmable clock generator: https://www.idt.com/document/dst/5p49v5923-datasheet
4. Realtime clocK: http://ww1.microchip.com/downloads/en/DeviceDoc/20005009F.pdf
5. NOR flash: https://www.adestotech.com/wp-content/uploads/doc3686.pdf
6. PMIC: https://cache.nxp.com/docs/en/data-sheet/PF3000.pdf
7. Battery charger: http://cds.linear.com/docs/en/datasheet/4155fd.pdf
8. MxM2 Connector drawing: http://www.acesconn.com/userfiles/f2d/88882-2Dxx-aces%20rev-E.pdf