MTrion

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CONTENTS:

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	02.10.2024	fn	Initial creation

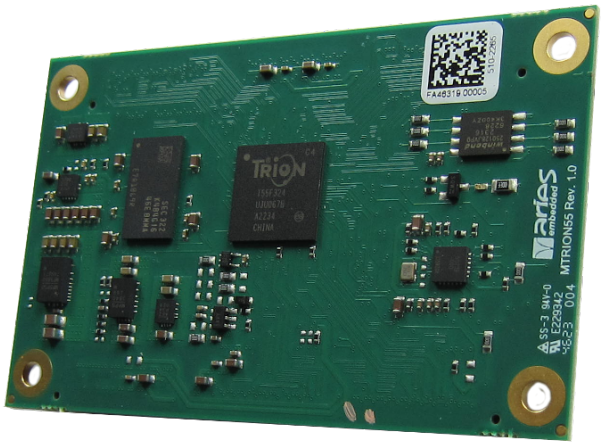
CHAPTER

TWO

OVERVIEW

2.1 MTrion - SoM based on Efinix® Trion® FPGA

MTrion System on Modules support the Trion® FPGA family and are the ideal solution to get FPGA projects quickly to market. The Mtrion SoMs support on-board DDR3 RAM, expose the MIPI-CSI and LVDS signals to the baseboard, they are the ideal fit for digital-logic as well as RISC-V based softcore implementations. Trion products are designed into a broad range of applications in many diverse markets. The Trion family of FPGAs is supported in customer designs until at least 2033, so are the MTrion SoMs. Based on the feature set MTrion supports various target markets such as e.g. Industrial Automation, video processing and the Internet-of-Things.



2.2 Feature Set

- **Trion FPGA in 324 ball FBGA package**
  - **T20**
    - 1.044 bit Embedded RAM
    - 36x 18x18 Multipliers
    - 7 PLLs
  - **T35**
    - 1.475 bit Embedded RAM
    - 120x 18x18 Multipliers
    - 7 PLLs
  - **T55 (Standard for MTrion)**
    - 2.765 bit Embedded RAM
    - 150x 18x18 Multipliers
    - 8 PLLs
  - **T85**
    - 4.055 bit Embedded RAM
    - 240x 18x18 Multipliers
    - 8 PLLs
  - **T120**
    - 5.407 bit Embedded RAM
    - 320x 18x18 Multipliers
    - 8 PLLs
- 128 MBit SPI NOR FLASH
- 512MByte DDR3 SDRAM
- programmable clock generator and PLL, with optional external reference input
- **161 FPGA GPIO pins**
  - including 29 LVDS transmitters and receivers
  - MIPI0 interface, 4 lanes
  - MIPI1 interface, 4 lanes
- Size: 77mm x 48mm
- temperature range 0°C…+70°C
- optional temperature range -40°C…+85°C

2.3 Order Codes

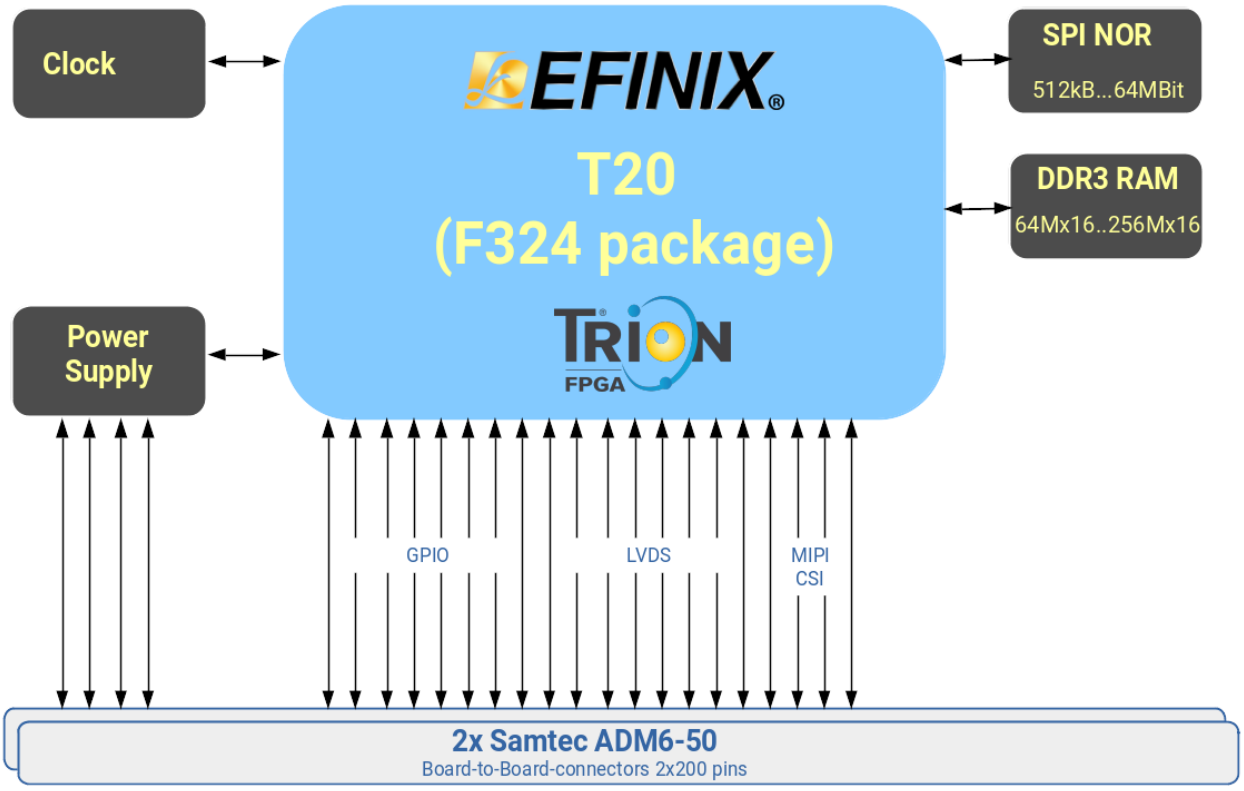
The MTrion is available in the following standard configurations:

MTrion55

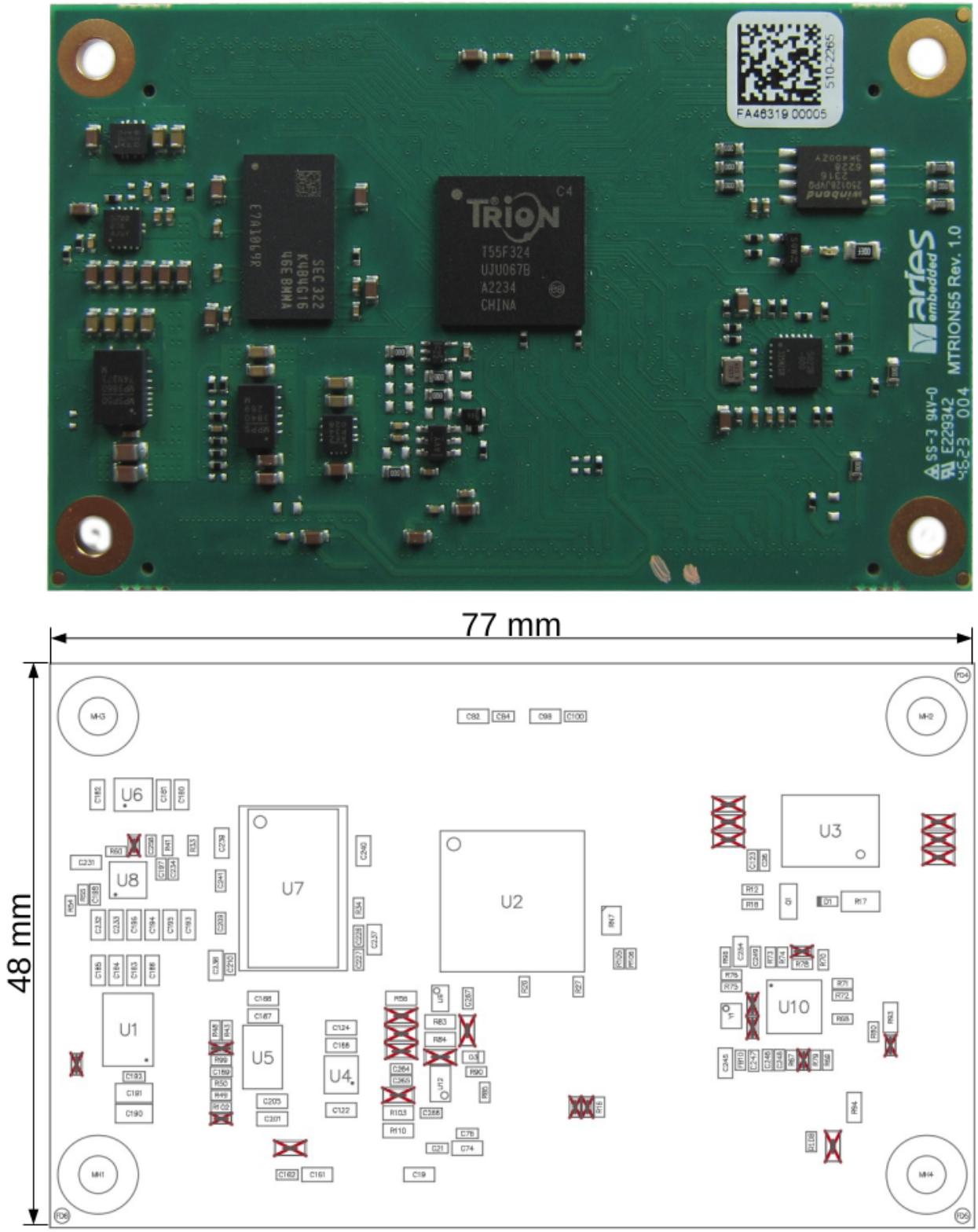
- **Trion FPGA in 324 ball FBGA package**
  - **T55 (Standard for MTrion)**
    - 2.765 bit Embedded RAM
    - 150x 18x18 Multipliers
    - 8 PLLs
- 128 MBit SPI NOR FLASH
- 512MByte DDR3 SDRAM
- programmable clock generator

Please contact ARIES Embedded for more information about the availability of other standard products of MSRZFive or custom configurations.

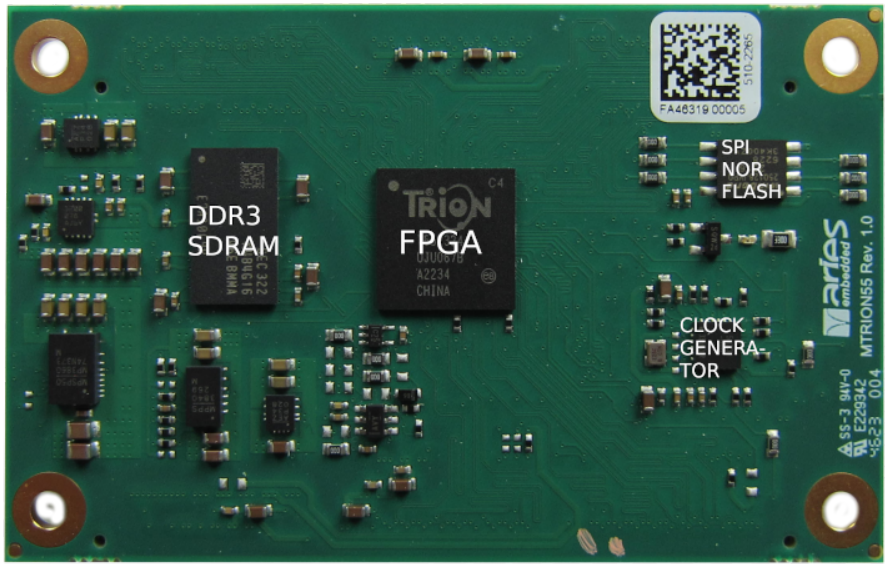
2.4 Block Diagram



2.5 Dimensions

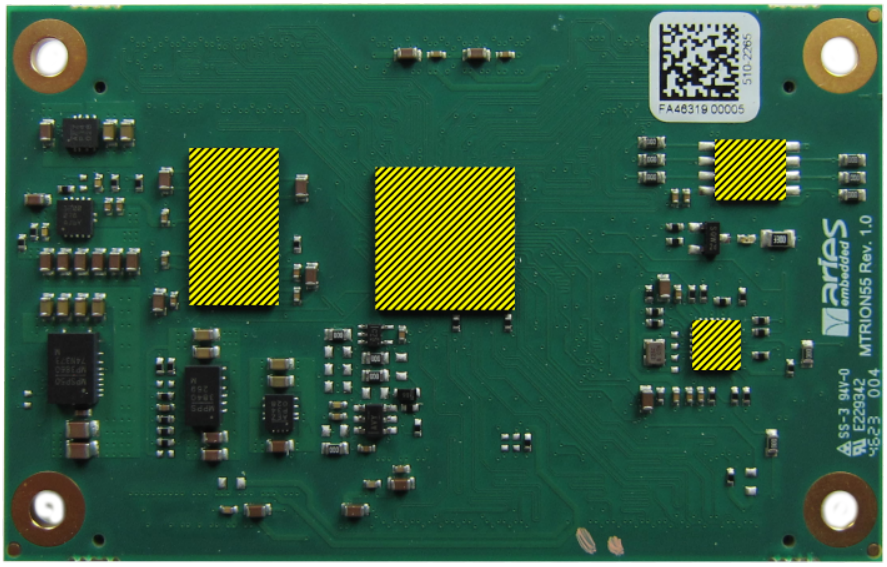


2.6 Part Overview



2.7 Handling Recommendations

To avoid mechanical damage to the components populated on MTrion it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

RESOURCES

3.1 Components

3.1.1 FPGA

MTrion provides a Trion® FPGA, which is built on a 40 nm process with a logic density range from 4K to 120K logic elements (LEs) and standard interfaces such as GPIO, PLLs, oscillators, MIPI, DDR, LVDS, etc. Trion FPGAs target general-purpose custom logic markets (mobile, IoT, general consumer, industrial, and medical) as well as fast-growing markets such as compute acceleration and deep learning in edge devices

FPGA features

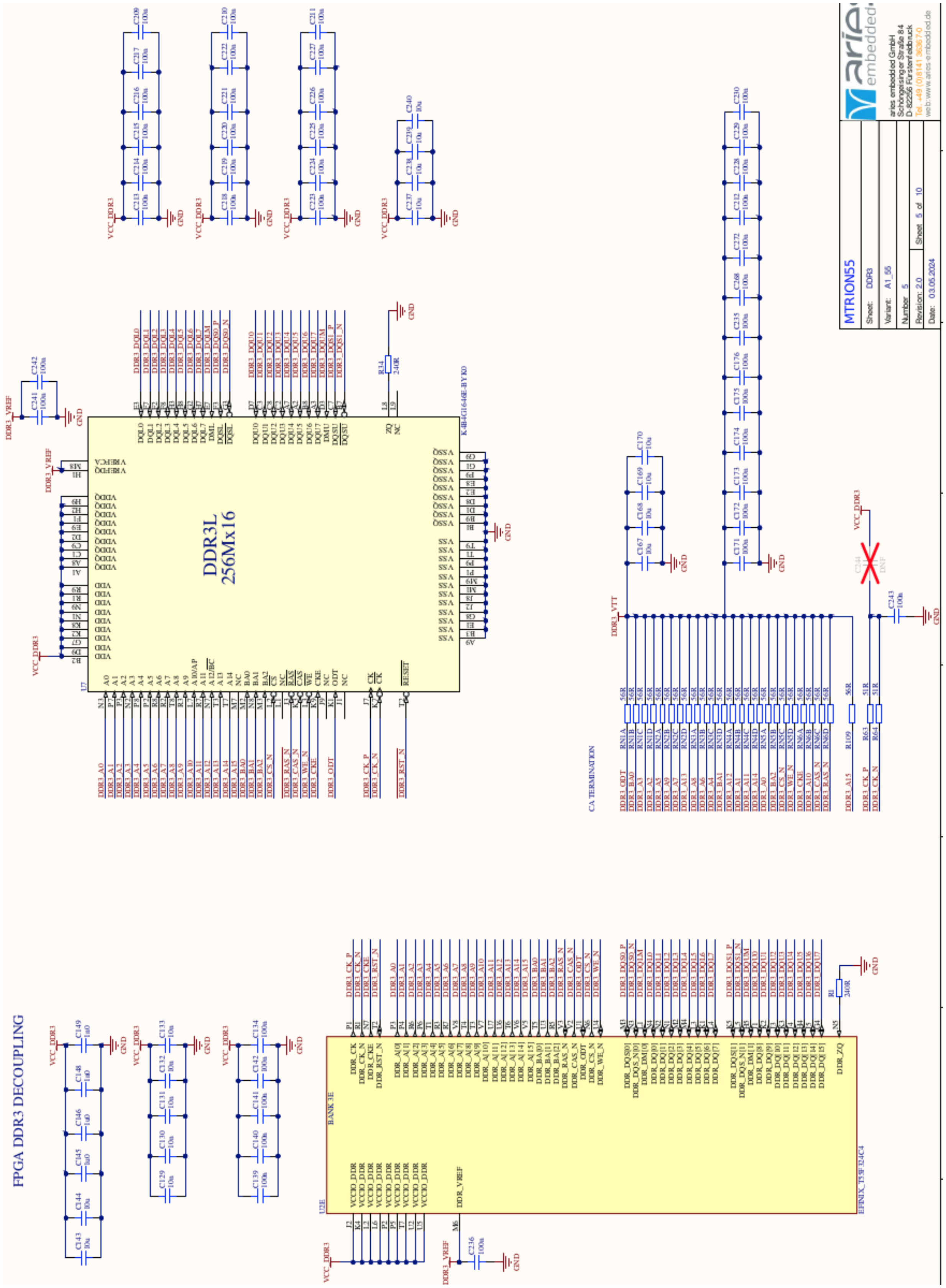
Feature	T20	T35	T55	T85	T120
Embedded RAM Bits (kb)	1,044	1,475	2,765	4,055	5,407
18x18 Multipliers	36	120	150	240	320
PLLs	7	7	8	8	8
LVDS (TX, RX)	20, 26	20, 26	52, 52	52, 52	52, 52
MIPI 4-lane DPHY with built-in CSI-2 controller	2 RX 2 TX	2 RX 2 TX	3 RX 3 TX	3 RX 3 TX	3 RX 3 TX

3.1.2 DDR3 SDRAM

The MTrion is equipped with the Samsung K4B4G1646E-BYK0 DDR3 SDRAM resulting in 4Gb of DDR3 memory and up to 1600 Mbps. Device is available in the commercial temperaturerange 0°C. . +85°C.

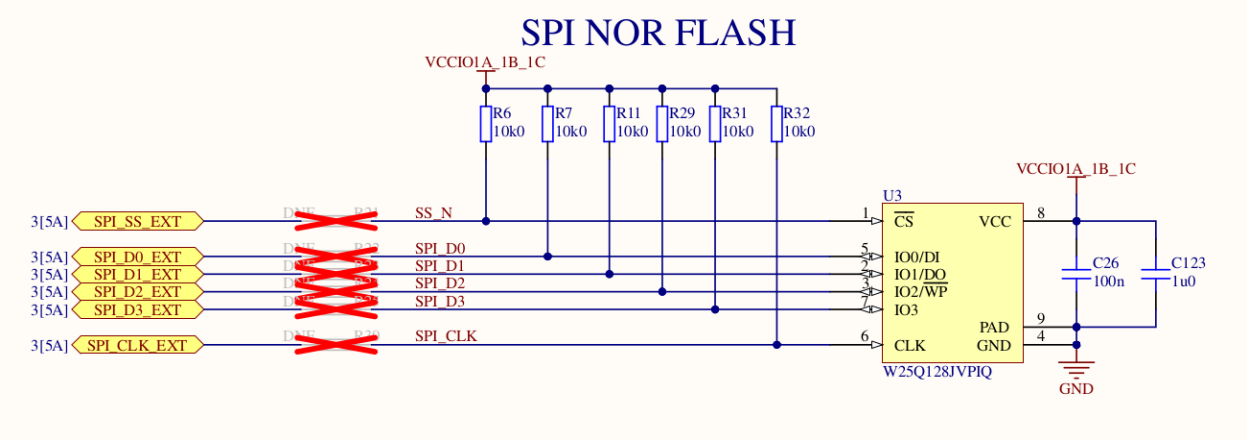
FPGA Signals for DDR3

FPGA Pin	Function	DDR3 Pin	FPGA Pin	Function	DDR3 Pin
P3	DDR3_A0	N3	N4	DDR3_DQL0	E3
P4	DDR3_A1	P7	N2	DDR3_DQL1	F7
R6	DDR3_A2	P3	N1	DDR3_DQL2	F2
P6	DDR3_A3	N2	M2	DDR3_DQL3	F8
T1	DDR3_A4	P8	M4	DDR3_DQL4	H3
R3	DDR3_A5	P2	L3	DDR3_DQL5	H8
R7	DDR3_A6	R8	K1	DDR3_DQL6	G2
V8	DDR3_A7	R2	L4	DDR3_DQL7	H7
T4	DDR3_A8	T8	L1	DDR3_DQLM	E7
T3	DDR3_A9	R3	M3	DDR3_DQS0_P	F3
V7	DDR3_A10	L7	N3	DDR3_DQS0_N	G3
U7	DDR3_A11	R7	J1	DDR3_DQU0	D7
U6	DDR3_A12	N7	K2	DDR3_DQU1	C3
T6	DDR3_A13	T3	J3	DDR3_DQU2	C8
V6	DDR3_A14	T7	K3	DDR3_DQU3	C2
V5	DDR3_A15	M7	J4	DDR3_DQU4	A7
T5	DDR3_BA0	M2	H4	DDR3_DQU5	A2
U3	DDR3_BA1	N8	J5	DDR3_DQU6	B8
R5	DDR3_BA2	M3	G4	DDR3_DQU7	A3
N6	DDR3_CS_N	L2	H5	DDR3_DQUM	D3
V3	DDR3_RAS_N	J3	K5	DDR3_DQS1_P	C7
V2	DDR3_CAS_N	K3	L5	DDR3_DQS1_N	B7
U4	DDR3_WE_N	L3	M6	DDR3_VREF	H1, M8
N7	DDR3_CKE	K9	–	–	–
U1	DDR3_ODT	K1	–	–	–
P1	DDR3_CK_P	J7	–	–	–
R1	DDR3_CK_N	K7	–	–	–
T2	DDR3_RST_N	T2	–	–	–


FPGA DDR3 DECOUPLING
DDR3L
256Mx16
K4B4G1646E-BYK0
CA TERMINATION
BANK 3E
EFINIX_T35F324C4
MTRION55
Sheet: DDR3
Variant: A1_55
Number: 5
Revision: 2.0
Sheet 5 of 10
Date: 03.05.2024
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck

3.1.3 SPI NOR FLASH

The MTrion offers the Windbond W25Q128JVPIQ (128M-bit) Serial Flash memory, which provides a storage solution for systems with limited space, pins and power. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1uA for power-down. The W25Q128JV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI.



J1 Connector Pin	Function	SPI Pin	FPGA Pin
153	SPI_SS_EXT	1	P15
151	SPI_D0_EXT	5	M13
149	SPI_D1_EXT	2	N14
145	SPI_D2_EXT	3	K14
143	SPI_D3_EXT	7	K18
155	SPI_CLK_EXT	6	N13

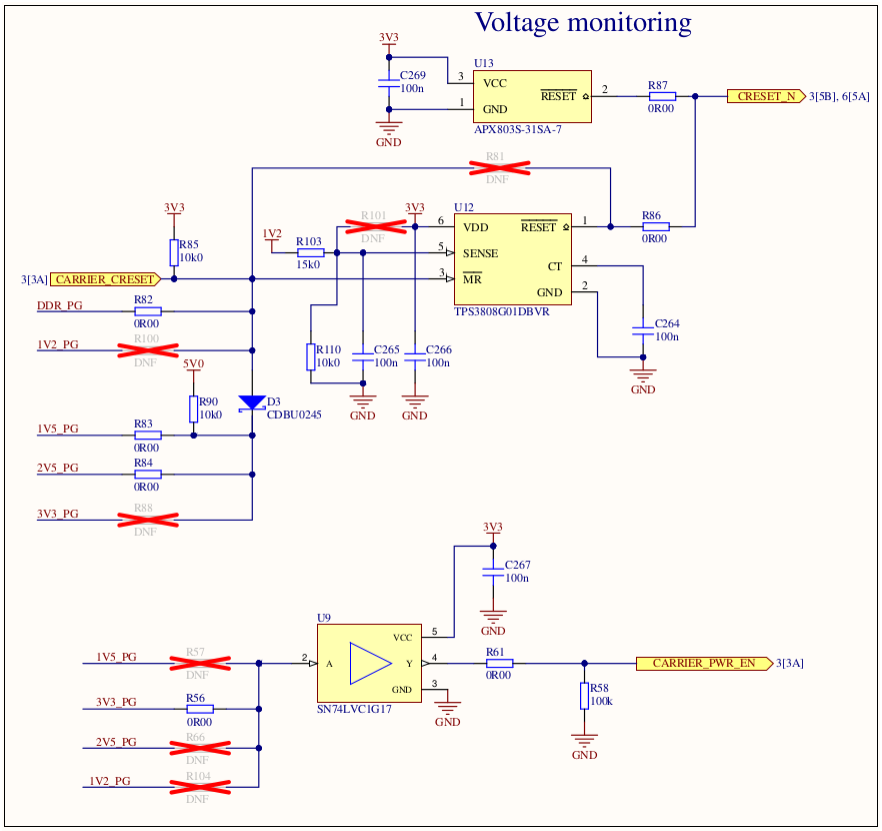
3.1.4 SPI Hardware Settings

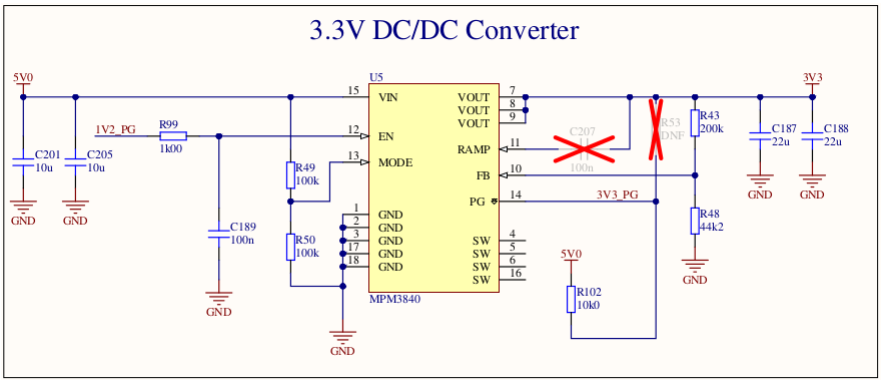
Configuration Mode	Parallel/Serial	TEST_N	SS_N	CBUS2, CBUS1, CBUS0	Width
SPI Active	Serial	1	1	3'b111	x1
	Parallel	1	1	3'b110	x2
	Parallel	1	1	3'b101	x4
SPI Passive	Serial	1	0	3'b111	x1
	Parallel	1	0	3'b110	x2
	Parallel	1	0	3'b101	x4
	Parallel	1	0	3'b100	x8
	Parallel	1	0	3'b011	x16
	Parallel	1	0	3'b010	x32

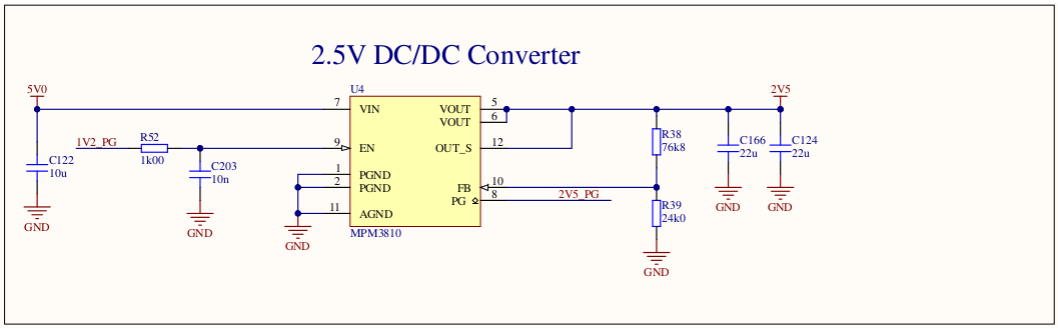
3.1.5 Power supply

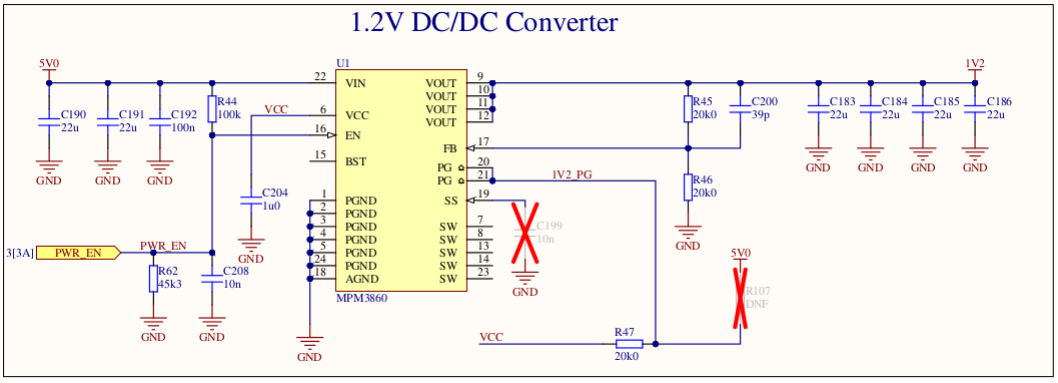
The module must be supplied with the following voltage:

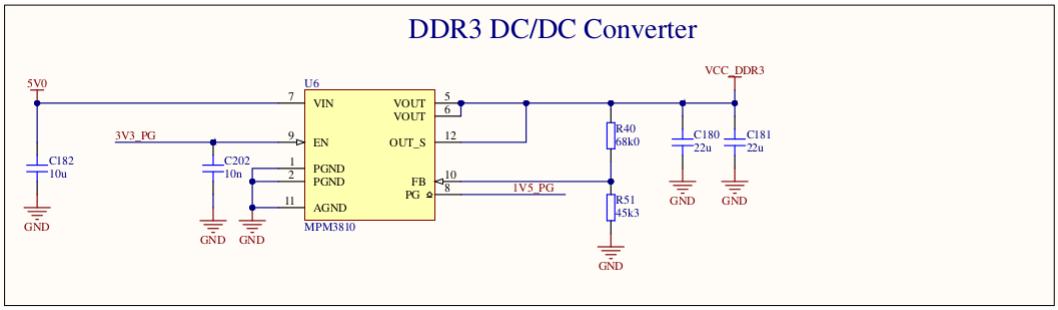
min. voltage	max. voltage
4.0 V	5.5 V

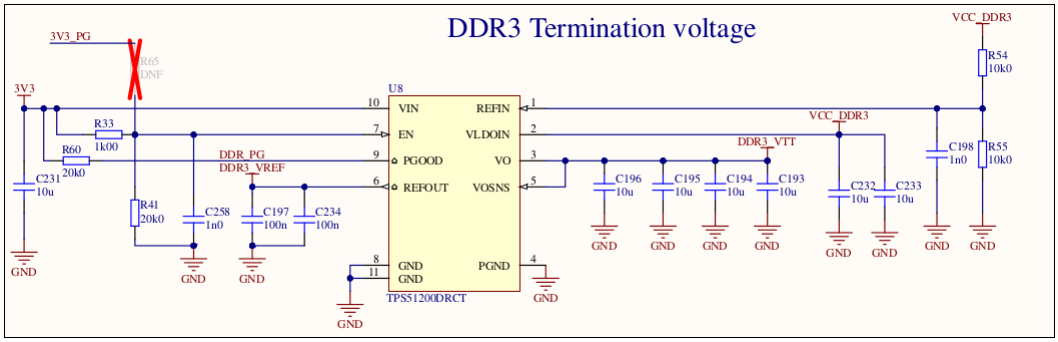





2.5V DC/DC Converter
5V0
U4
VIN
VOUT
VOUT
EN
OUT_S
PGND
PGND
FB
PG
AGND
MPM3810
1V2_PG
R52
1k00
C122
10u
C203
10n
2V5_PG
R38
76k8
R39
24k0
C166
22u
C124
22u
2V5
GND


1.2V DC/DC Converter
5V0
U1
VIN
VCC
EN
BST
PGND
AGND
SW
VOUT
FB
PG
SS
MPM3860
C190
22u
C191
22u
C192
100n
R44
100k
C204
1u0
C208
10n
R62
45k3
PWR_EN
3[3A]
C199
10n
R45
20k0
C200
39p
R46
20k0
C183
22u
C184
22u
C185
22u
C186
22u
1V2
1V2_PG
R47
20k0
R107
DNF
GND


DDR3 DC/DC Converter
5V0
U6
VIN
VOUT
EN
OUT_S
PGND
FB
PG
AGND
MPM3810
3V3_PG
C182
10u
C202
10n
1V5_PG
R40
68k0
R51
45k3
C180
22u
C181
22u
VCC_DDR3
GND

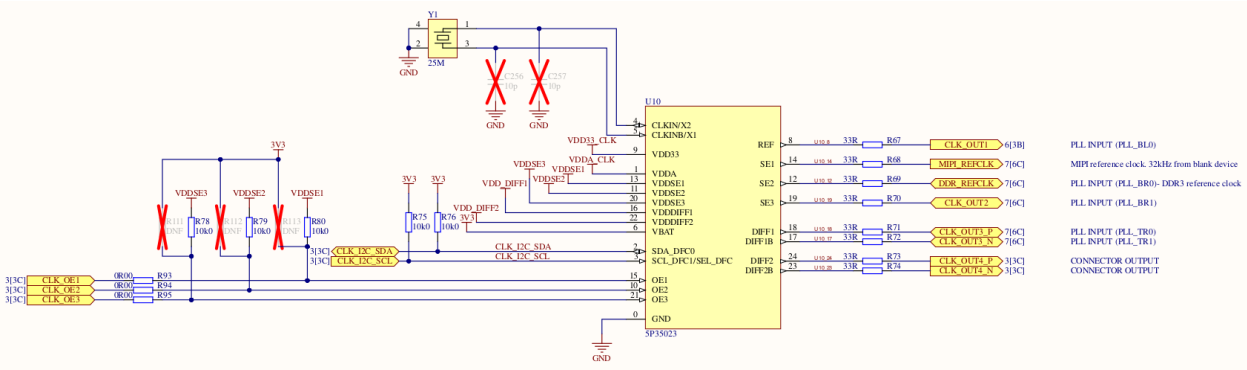

DDR3 Termination voltage
3V3_PG
R65
DNF
3V3
U8
VIN
EN
PGOOD
REFOUT
REFIN
VLDOIN
VO
VOSNS
GND
PGND
TPS51200DRCT
R33
1k00
R60
20k0
DDR_PG
DDR3_VREF
C231
10u
R41
20k0
C258
1n0
C197
100n
C234
100n
C196
10u
C195
10u
C194
10u
C193
10u
DDR3_VTT
C232
10u
C233
10u
C198
1n0
R54
10k0
R55
10k0
VCC_DDR3
GND

3.1.6 Clock Generator

The MTrion offers the Renesas 5P35023 VersaClock® programmable clock generator, which is designed for low-power, consumer, and high-performance PCI Express applications. The 5P35023 has built-in unique features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshot Reduction Technology (ORT) and Extreme Low Power DCO.

FPGA Pin	Function	Clock Generator Pin	J1 Connector Pin
–	CLK_I2C_SDA	2	93
–	CLK_I2C_SCL	3	95
–	CLK_OE1	15	87
–	CLK_OE2	10	89
–	CLK_OE3	21	91
L14	CLK_OUT1	8	–
F10	MIPI_REFCLK	14	–
U8	DDR_REFCLK	12	–
T8	CLK_OUT2	19	–
C9	CLK_OUT3_P	18	–
D9	CLK_OUT3_N	17	–
–	CLK_OUT4_P	24	101
–	CLK_OUT4_N	23	99

.



3.2 Pin Out

3.2.1 MIPI

MIPI0

FPGA Pin	Function	J2 Connector Pin		FPGA Pin	Function	J2 Connector Pin
E5	MIPI0_RX_0_P	4		B6	MIPI0_TX_0_P	57
D5	MIPI0_RX_0_N	6		A6	MIPI0_TX_0_N	59
E8	MIPI0_RX_1_P	10		A7	MIPI0_TX_1_P	51
D8	MIPI0_RX_1_N	12		B7	MIPI0_TX_1_N	53
F6	MIPI0_RX_2_P	16		B8	MIPI0_TX_2_P	45
F5	MIPI0_RX_2_N	18		A8	MIPI0_TX_2_N	47
E6	MIPI0_RX_3_P	22		A5	MIPI0_TX_3_P	39
D6	MIPI0_RX_3_N	24		B5	MIPI0_TX_3_N	41
E7	MIPI0_RX_4_P	28		A4	MIPI0_TX_4_P	33
F7	MIPI0_RX_4_N	30		B4	MIPI0_TX_4_N	35

MIPI1

FPGA Pin	Function	J2 Connector Pin		FPGA Pin	Function	J2 Connector Pin
D4	MIPI1_RX_0_P	34		B3	MIPI1_TX_0_P	27
E4	MIPI1_RX_0_N	36		A3	MIPI1_TX_0_N	29
F3	MIPI1_RX_1_P	40		B2	MIPI1_TX_1_P	21
G3	MIPI1_RX_1_N	42		A2	MIPI1_TX_1_N	23
G1	MIPI1_RX_2_P	46		C1	MIPI1_TX_2_P	15
F1	MIPI1_RX_2_N	48		B1	MIPI1_TX_2_N	17
H2	MIPI1_RX_3_P	52		D2	MIPI1_TX_3_P	9
G2	MIPI1_RX_3_N	54		E2	MIPI1_TX_3_N	11
D3	MIPI1_RX_4_P	58		E1	MIPI1_TX_4_P	3
E3	MIPI1_RX_4_N	60		D1	MIPI1_TX_4_N	5

3.2.2 LVDS

LVDS RX

FPGA Pin	Function	J2 Connector Pin		FPGA Pin	Function	J2 Connector Pin
D13	GPIOT_RX01_P	67		D18	GPIOT_RX16_P	146
C13	GPIOT_RX01_N	69		E18	GPIOT_RX16_N	148
C16	GPIOT_RX02_P	73		H18	GPIOT_RX17_P	140
D16	GPIOT_RX02_N	75		G18	GPIOT_RX17_N	142
D11	GPIOT_RX03_P	79		B18	GPIOT_RX18_P	134
C11	GPIOT_RX03_N	81		C18	GPIOT_RX18_N	136
D15	GPIOT_RX04_P	85		A17	GPIOT_RX19_P	128
E15	GPIOT_RX04_N	87		B17	GPIOT_RX19_N	130
D14	GPIOT_RX05_P	91		B16	GPIOT_RX20_P	175
E14	GPIOT_RX05_N	93		A16	GPIOT_RX20_N	177
E12	GPIOT_RX06_P	97		B15	GPIOT_RX21_P	169
D12	GPIOT_RX06_N	99		A15	GPIOT_RX21_N	171
E13	GPIOT_RX07_P	103		B14	GPIOT_RX22_P	163
F13	GPIOT_RX07_N	105		A14	GPIOT_RX22_N	165
E11	GPIOT_RX08_P	109		B13	GPIOT_RX23_P	157
F11	GPIOT_RX08_N	111		A13	GPIOT_RX23_N	159
E16	GPIOT_RX09_P	115		A12	GPIOT_RX24_P	151
F16	GPIOT_RX09_N	117		B12	GPIOT_RX24_N	153
G17	GPIOT_RX11_P	176		A11	GPIOT_RX27_P	145
H17	GPIOT_RX11_N	178		B11	GPIOT_RX27_N	147
G16	GPIOT_RX12_P	170		A10	GPIOT_RX28_P	139
H16	GPIOT_RX12_N	172		B10	GPIOT_RX28_N	141
G15	GPIOT_RX13_P	164		B9	GPIOT_RX29_P	133
H15	GPIOT_RX13_N	166		A9	GPIOT_RX29_N	135
G14	GPIOT_RX14_P	158		–	–	–
F14	GPIOT_RX14_N	160		–	–	–
D17	GPIOT_RX15_P	152		–	–	–
E17	GPIOT_RX15_N	154		–	–	–

LVDS TX

FPGA Pin	Function	J1 Connector Pin		FPGA Pin	Function	J1 Connector Pin
V12	GPIOB_TX10_P	116		T17	GPIOB_TX00_P	176
U12	GPIOB_TX10_N	118		R17	GPIOB_TX00_N	178
R12	GPIOB_TX11_P	110		U18	GPIOB_TX01_P	170
T12	GPIOB_TX11_N	112		T18	GPIOB_TX01_N	172
P12	GPIOB_TX12_P	104		R18	GPIOB_TX02_P	164
N12	GPIOB_TX12_N	106		P18	GPIOB_TX02_N	166
N11	GPIOB_TX13_P	98		U16	GPIOB_TX03_P	158
P11	GPIOB_TX13_N	100		V16	GPIOB_TX03_N	160
N10	GPIOB_TX14_P	92		U15	GPIOB_TX04_P	152
P10	GPIOB_TX14_N	94		V15	GPIOB_TX04_N	154
U10	GPIOB_TX15_P	86		T15	GPIOB_TX05_P	146
V10	GPIOB_TX15_N	88		R15	GPIOB_TX05_N	148
N9	GPIOB_TX16_P	80		V14	GPIOB_TX06_P	140
P9	GPIOB_TX16_N	82		U14	GPIOB_TX06_N	142
V9	GPIOB_TX17_P	74		P14	GPIOB_TX07_P	134
U9	GPIOB_TX17_N	76		R14	GPIOB_TX07_N	136
U11	GPIOB_TX18_P	68		V13	GPIOB_TX08_P	128
T11	GPIOB_TX18_N	70		U13	GPIOB_TX08_N	130
T9	GPIOB_TX19_P	62		P13	GPIOB_TX09_P	122
R9	GPIOB_TX19_N	64		R13	GPIOB_TX09_N	124

3.2.3 JTAG

FPGA Pin	Function	J1 Connector Pin
P16	JTAG_TMS	161
P17	JTAG_TDO	163
R16	JTAG_TDI	165
T16	JTAG_TCK	167

3.2.4 Further pins

FPGA Pin	Function	J1 Connector Pin
N17	CRESET_N	159
N18	CDONE	157
N15	GPIOL_04_CSI	169
M15	GPIOL_05_CSO/RGMII_TXD0	171
M14	GPIOL_11_CBUS0	173
M16	GPIOL_12_CBUS1	175
M17	GPIOL_13_CBUS2	177
L15	GPIOL_17/RGMII_TXCTL	133
L17	GPIOL_24/RGMII_TXCLK	135
L16	GPIOL_22/RGMII_TXD3	137
L18	GPIOL_20/RGMII_TXD2	139
M18	GPIOL_18/RGMII_TXD1	141
K17	GPIOL_66_CLK0/RGMII_RXD1	125
K15	GPIOL_63_CTRL1/RGMII_RXD2	127
K16	GPIOL_62_CTRL0/RGMII_RXD3	129
H14	GPIOL_72_CLK6/RGMII_RXC	105
H13	GPIOL_73_CLK7/RGMII_RXCTL	107
G13	GPIOL_75_CTRL5/RGMII_RXD0	109
J17	GPIOL_156/CBSEL0	113
J18	GPIOL_157/CBSEL1	115
J14	GPIOL_150_NSTATUS	119
J15	GPIOL_151_TEST_N	117

FPGA Pin	Function	J2 Connector Pin
G5	GPIOR_173_CTRL12	70
G6	GPIOR_174_CLK15	72
H6	GPIOR_178_CLK11	74
K6	GPIOR_183_CTRL10	76
R8	GPIOR_188_PLLIN2	66
E9	GPIOR_168_PLLIN2	64

3.3 MTrion Connectors

Connector Bottom J1

Contact Overview

FPGA Pin	Function	Connector Pin		FPGA Pin	Function	Connector Pin
J1A						
–	5V0	1		–	–	2
–	5V0	3		–	–	4
–	5V0	5		–	–	6
–	5V0	7		–	CARRIER_PWR_EN	8
–	5V0	9		–	–	10
–	5V0	11		–	PWR_EN	12
–	5V0	13		–	–	14
–	5V0	15		–	CARRIER_CRESET	16
–	5V0	17		–	–	18
–	5V0	19		–	3V3	20
–	–	21		–	3V3	22
–	3V3	23		–	–	24
–	3V3	25		–	VDD_DIFF2_IN	26
–	3V3	27		–	–	28
–	–	29		–	2V5	30
–	VCCIO1A_1B_1C_CON	31		–	2V5	32
–	VCCIO1A_1B_1C_CON	33		–	–	34
–	VCCIO1A_1B_1C_CON	35		–	VCCIO3D_TR_BR	36
–	–	37		–	VCCIO3D_TR_BR	38
–	2V5	39		–	–	40
–	2V5	41		–	3V3	42
–	2V5	43		–	3V3	44
–	–	45		–	–	46
–	VCCIO1D_1E_1F_1G	47		–	–	48
–	VCCIO1D_1E_1F_1G	49		–	–	50
–	VCCIO1D_1E_1F_1G	51		–	–	52
–	–	53		–	–	54
–	3V3	55		–	–	56
–	3V3	57		–	–	58
–	3V3	59		–	–	60
–	GND	181		–	GND	183
–	GND	182		–	GND	184
J1B						
–	VCCIO4E	61		T9	GPIOB_TX19_P	62
–	VCCIO4E	63		R9	GPIOB_TX19_N	64
–	–	65		–	GND	66
–	2V5	67		U11	GPIOB_TX18_P	68
–	2V5	69		T11	GPIOB_TX18_N	70
–	2V5	71		–	GND	72

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Table 1 – continued from previous page

FPGA Pin	Function	Connector Pin		FPGA Pin	Function	Connector Pin
–	–	73		V9	GPIOB_TX17_P	74
–	VCCIO4F	75		U9	GPIOB_TX17_N	76
–	VCCIO4F	77		–	GND	78
–	–	79		N9	GPIOB_TX16_P	80
–	3V3	81		P9	GPIOB_TX16_N	82
–	3V3	83		–	GND	84
–	–	85		U10	GPIOB_TX15_P	86
–	CLK_OE1	87		V10	GPIOB_TX15_N	88
–	CLK_OE2	89		–	GND	90
–	CLK_OE3	91		N10	GPIOB_TX14_P	92
–	CLK_I2C_SDA	93		P10	GPIOB_TX14_N	94
–	CLK_I2C_SCL	95		–	GND	96
–	–	97		N11	GPIOB_TX13_P	98
–	CLK_OUT4_N	99		P11	GPIOB_TX13_N	100
–	CLK_OUT4_P	101		–	GND	102
–	–	103		P12	GPIOB_TX12_P	104
H14	GPIOL_72_CLK6/RGMII_RXC	105		N12	GPIOB_TX12_N	106
H13	GPIOL_73_CLK7/RGMII_RXCTL	107		–	GND	108
G13	GPIOL_75_CTRL5/RGMII_RXD0	109		R12	GPIOB_TX11_P	110
–	–	111		T12	GPIOB_TX11_N	112
J17	GPIOL_156/CBSEL0	113		–	GND	114
J18	GPIOL_157/CBSEL1	115		V12	GPIOB_TX10_P	116
J15	GPIOL_151_TEST_N	117		U12	GPIOB_TX10_N	118
J14	GPIOL_150_NSTATUS	119		–	GND	120
–	GND	185		–	GND	187
–	GND	186		–	GND	188
J1C						
–	–	121		P13	GPIOB_TX09_P	122
–	–	123		R13	GPIOB_TX09_N	124
K17	GPIOL_66_CLK0/RGMII_RXD1	125		–	GND	126
K15	GPIOL_63_CTRL1/RGMII_RXD2	127		V13	GPIOB_TX08_P	128
K16	GPIOL_62_CTRL0/RGMII_RXD3	129		U13	GPIOB_TX08_N	130
–	–	131		–	GND	132
L15	GPIOL_17/RGMII_TXCTL	133		P14	GPIOB_TX07_P	134
L17	GPIOL_24/RGMII_TXCLK	135		R14	GPIOB_TX07_N	136
L16	GPIOL_22/RGMII_TXD3	137		–	GND	138
L18	GPIOL_20/RGMII_TXD2	139		V14	GPIOB_TX06_P	140
M18	GPIOL_18/RGMII_TXD1	141		U14	GPIOB_TX06_N	142
–	SPI_D3_EXT	143		–	GND	144
–	SPI_D2_EXT	145		T15	GPIOB_TX05_P	146
–	–	147		R15	GPIOB_TX05_N	148
–	SPI_D1_EXT	149		–	GND	150
–	SPI_D0_EXT	151		U15	GPIOB_TX04_P	152
–	SPI_SS_EXT	153		V15	GPIOB_TX04_N	154
–	SPI_CLK_EXT	155		–	GND	156
N18	CDONE	157		U16	GPIOB_TX03_P	158
N17	CRESET_N	159		V16	GPIOB_TX03_N	160

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Table 1 – continued from previous page

FPGA Pin	Function	Connector Pin		FPGA Pin	Function	Connector Pin
P16	JTAG_TMS	161		–	GND	162
P17	JTAG_TDO	163		R18	GPIOB_TX02_P	164
R16	JTAG_TDI	165		P18	GPIOB_TX02_N	166
T16	JTAG_TCK	167		–	GND	168
N15	GPIOL_04_CSI	169		U18	GPIOB_TX01_P	170
M15	GPIOL_05_CSO/RGMII_TXD0	171		T18	GPIOB_TX01_N	172
M14	GPIOL_11_CBUS0	173		–	GND	174
M16	GPIOL_12_CBUS1	175		T17	GPIOB_TX00_P	176
M17	GPIOL_13_CBUS2	177		R17	GPIOB_TX00_N	178
–	–	179		–	GND	180
–	GND	189		–	GND	191
–	GND	190		–	GND	192

Connector Top J2

Contact Overview

FPGA Pin	Function	Connector Pin		FPGA Pin	Function	Connector Pin
J2A						
–	GND	1		–	GND	2
E1	MIPI1_TX_4_P	3		E5	MIPI0_RX_0_P	4
D1	MIPI1_TX_4_N	5		D5	MIPI0_RX_0_N	6
–	GND	7		–	GND	8
D2	MIPI1_TX_3_P	9		E8	MIPI0_RX_1_P	10
E2	MIPI1_TX_3_N	11		D8	MIPI0_RX_1_N	12
–	GND	13		–	GND	14
C1	MIPI1_TX_2_P	15		F6	MIPI0_RX_2_P	16
B1	MIPI1_TX_2_N	17		F5	MIPI0_RX_2_N	18
–	GND	19		–	GND	20
B2	MIPI1_TX_1_P	21		E6	MIPI0_RX_3_P	22
A2	MIPI1_TX_1_N	23		D6	MIPI0_RX_3_N	24
–	GND	25		–	GND	26
B3	MIPI1_TX_0_P	27		E7	MIPI0_RX_4_P	28
A3	MIPI1_TX_0_N	29		F7	MIPI0_RX_4_N	30
–	GND	31		–	GND	32
A4	MIPI0_TX_4_P	33		D4	MIPI1_RX_0_P	34
B4	MIPI0_TX_4_N	35		E4	MIPI1_RX_0_N	36
–	GND	37		–	GND	38
A5	MIPI0_TX_3_P	39		F3	MIPI1_RX_1_P	40
B5	MIPI0_TX_3_N	41		G3	MIPI1_RX_1_N	42
–	GND	43		–	GND	44
B8	MIPI0_TX_2_P	45		G1	MIPI1_RX_2_P	46
A8	MIPI0_TX_2_N	47		F1	MIPI1_RX_2_N	48
–	GND	49		–	GND	50
A7	MIPI0_TX_1_P	51		H2	MIPI1_RX_3_P	52
B7	MIPI0_TX_1_N	53		G2	MIPI1_RX_3_N	54

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Table 2 – continued from previous page

FPGA Pin	Function	Connector Pin		FPGA Pin	Function	Connector Pin
–	GND	55		–	GND	56
B6	MIPI0_TX_0_P	57		D3	MIPI1_RX_4_P	58
A6	MIPI0_TX_0_N	59		E3	MIPI1_RX_4_N	60
–	GND	181		–	GND	183
–	GND	182		–	GND	184
J2B						
–	–	61		–	–	62
–	–	63		E9	GPIOR_168_PLLIN2	64
–	GND	65		R8	GPIOR_188_PLLIN2	66
D13	GPIOT_RX01_P	67		–	–	68
C13	GPIOT_RX01_N	69		G5	GPIOR_173_CTRL12	70
–	GND	71		G6	GPIOR_174_CLK15	72
C16	GPIOT_RX02_P	73		H6	GPIOR_178_CLK11	74
D16	GPIOT_RX02_N	75		K6	GPIOR_183_CTRL10	76
–	GND	77		–	–	78
D11	GPIOT_RX03_P	79		–	3V3	80
C11	GPIOT_RX03_N	81		–	3V3	82
–	GND	83		–	–	84
D15	GPIOT_RX04_P	85		–	VCCIO2D	86
E15	GPIOT_RX04_N	87		–	VCCIO2D	88
–	GND	89		–	–	90
D14	GPIOT_RX05_P	91		–	2V5	92
E14	GPIOT_RX05_N	93		–	2V5	94
–	GND	95		–	–	96
E12	GPIOT_RX06_P	97		–	VCCIO2E	98
D12	GPIOT_RX06_N	99		–	VCCIO2E	100
–	GND	101		–	–	102
E13	GPIOT_RX07_P	103		–	3V3	104
F13	GPIOT_RX07_N	105		–	3V3	106
–	GND	107		–	–	108
E11	GPIOT_RX08_P	109		–	VCCIO2F	110
F11	GPIOT_RX08_N	111		–	VCCIO2F	112
–	GND	113		–	–	114
E16	GPIOT_RX09_P	115		–	2V5	116
F16	GPIOT_RX09_N	117		–	2V5	118
–	GND	119		–	–	120
–	GND	185		–	GND	187
–	GND	186		–	GND	188
J2C						
–	3V3	121		–	2V5	122
–	3V3	123		–	–	124
–	3V3	125		–	GND	126
–	–	127		A17	GPIOT_RX19_P	128
–	–	129		B17	GPIOT_RX19_N	130
–	GND	131		–	GND	132

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Table 2 – continued from previous page

FPGA Pin	Function	Connector Pin		FPGA Pin	Function	Connector Pin
B9	GPIOT_RX29_P	133		B18	GPIOT_RX18_P	134
A9	GPIOT_RX29_N	135		C18	GPIOT_RX18_N	136
–	GND	137		–	GND	138
A10	GPIOT_RX28_P	139		H18	GPIOT_RX17_P	140
B10	GPIOT_RX28_N	141		G18	GPIOT_RX17_N	142
–	GND	143		–	GND	144
A11	GPIOT_RX27_P	145		D18	GPIOT_RX16_P	146
B11	GPIOT_RX27_N	147		E18	GPIOT_RX16_N	148
–	GND	149		–	GND	150
A12	GPIOT_RX24_P	151		D17	GPIOT_RX15_P	152
B12	GPIOT_RX24_N	153		E17	GPIOT_RX15_N	154
–	GND	155		–	GND	156
B13	GPIOT_RX23_P	157		G14	GPIOT_RX14_P	158
A13	GPIOT_RX23_N	159		F14	GPIOT_RX14_N	160
–	GND	161		–	GND	162
B14	GPIOT_RX22_P	163		G15	GPIOT_RX13_P	164
A14	GPIOT_RX22_N	165		H15	GPIOT_RX13_N	166
–	GND	167		–	GND	168
B15	GPIOT_RX21_P	169		G16	GPIOT_RX12_P	170
A15	GPIOT_RX21_N	171		H16	GPIOT_RX12_N	172
–	GND	173		–	GND	174
B16	GPIOT_RX20_P	175		G17	GPIOT_RX11_P	176
A16	GPIOT_RX20_N	177		H17	GPIOT_RX11_N	178
–	GND	179		–	GND	180
–	GND	189		–	GND	191
–	GND	190		–	GND	192

3.4 Schematics

Schematics for the MTrion SiP may be obtained on request. Please contact sales@aries-embedded.de.

Below the schematics of the connectors J1 and J2 are shown: