MSRZG3S hardwaremanual

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	09.09.2024	fn	Initial creation

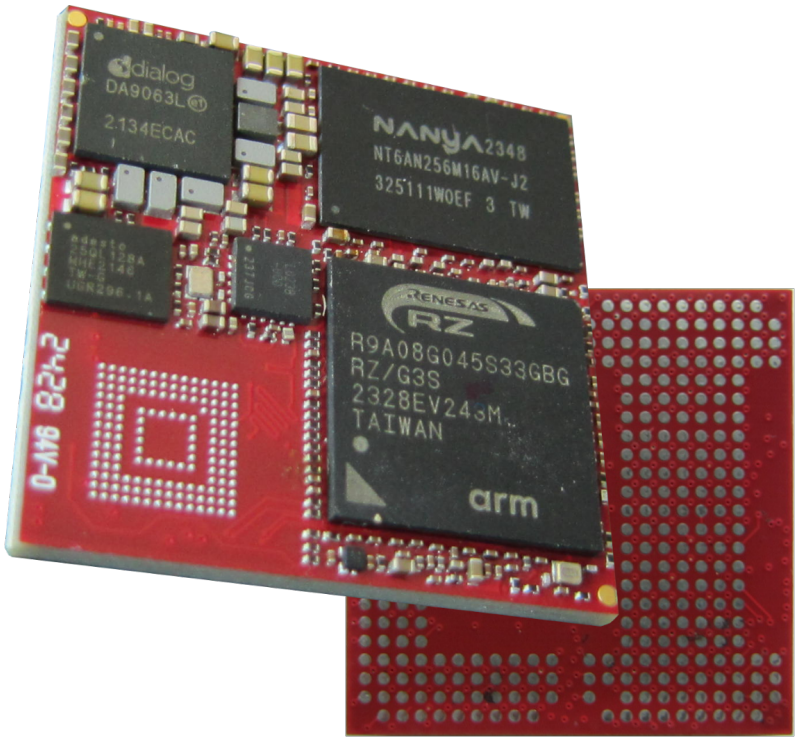
CHAPTER

TWO

OVERVIEW

2.1 MSRZG3S Microprocessor SiP

The MSRZG3S is the Open Standard Module compliant System-In-Package based on Renesas RZ Family architecture offering high-performance Cortex-A55/two Cortex-M33 cores. The MSRZG3S combines compact design and a wide range of services, bringing low power consumption, thermal efficiency and low-cost to embedded systems.



2.2 Feature Set

- **RZ/G3S general-purpose microprocessor unit**
  - Single Cortex-A55 MPCore, up to 1,1 GHz
  - two 250 MHz Cortex-M33 (one Cortex-M33 has FPU function)
- LPDDR4 SDRAM
- 4GB eMMC NAND Flash
- 125Mbit SPI NOR FLASH
- Clock Generator
- USB, CAN, Ethernet
- UART, I2C, I2S, SPI
- JTAG, SDIO, PCIE
- ADC, PWM, GPIO
- size S, 30x30 mm^2
- signal count: 332
- -25°C..+70°C commercial temperature range
- -40°C..+85°C industrial temperature range

2.3 Order Codes

The MSRZG3S SiP is available in the following standard configurations:

MSRZG3S-A0A

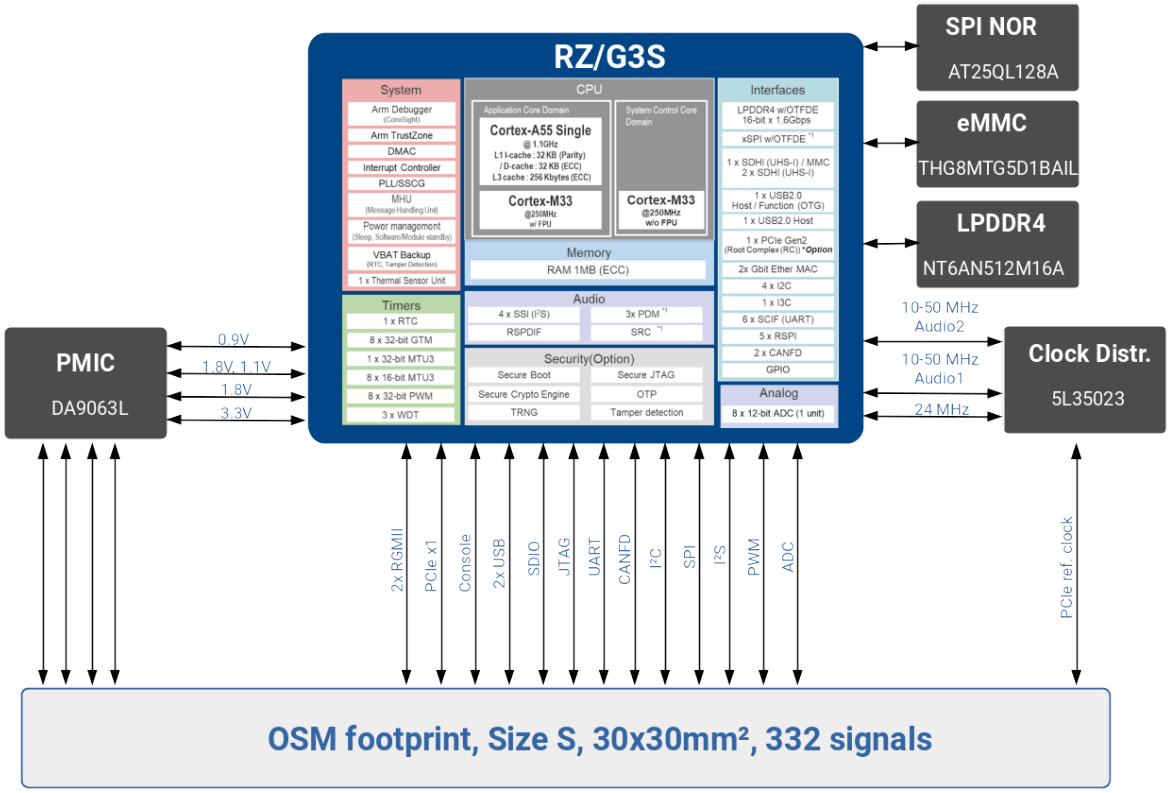
- RZ/G3S CPU
- R9A08G045S33GBG
- 512MB LPDDR4 SDRAM
- No eMMC NAND Flash
- 128MBit SPI NOR
- -25°C..+85°C

MSRZG3S-BAA

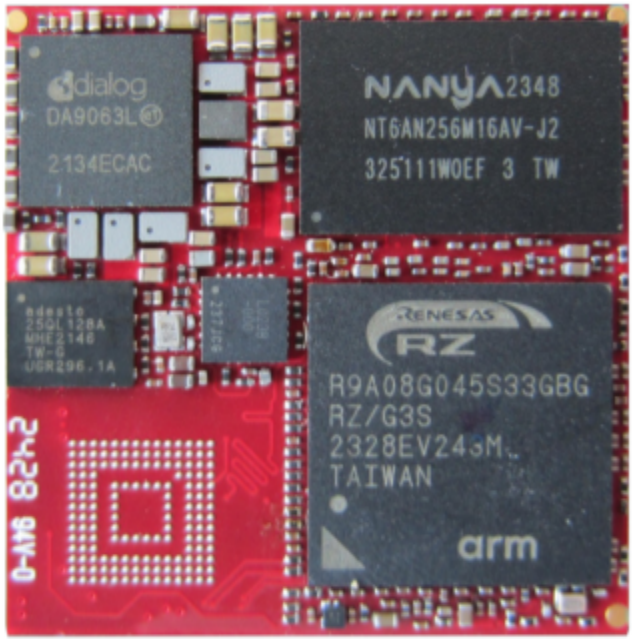
- RZ/G3S CPU
- R9A08G045S33GBG
- 1GB LPDDR4 SDRAM
- 4GB eMMC NAND Flash
- 128MBit SPI NOR
- -25°C..+85°C

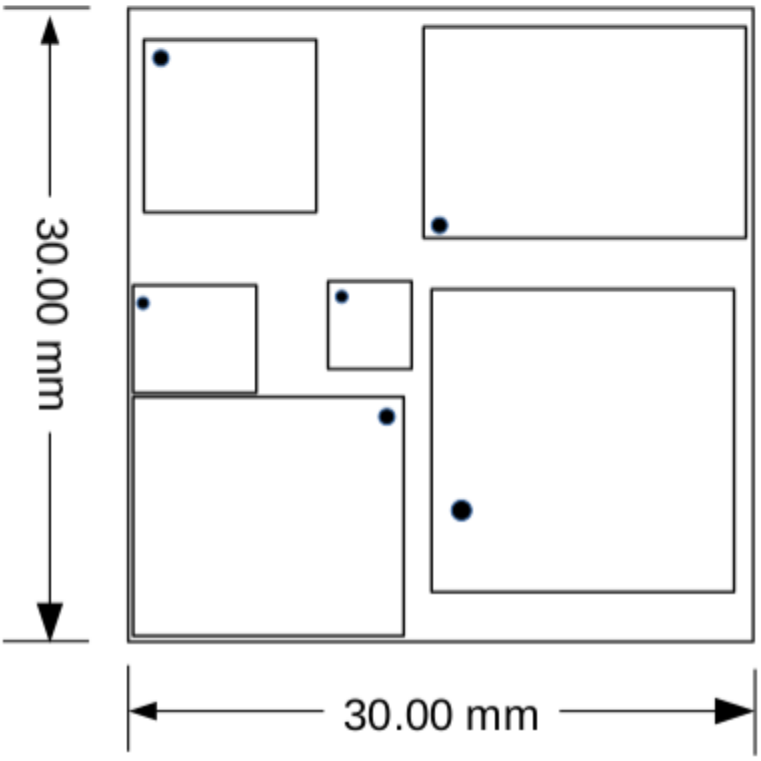
Please contact ARIES Embedded for more information about the availability of other standard products of MSRZG3S or custom configurations.

2.4 Block Diagram



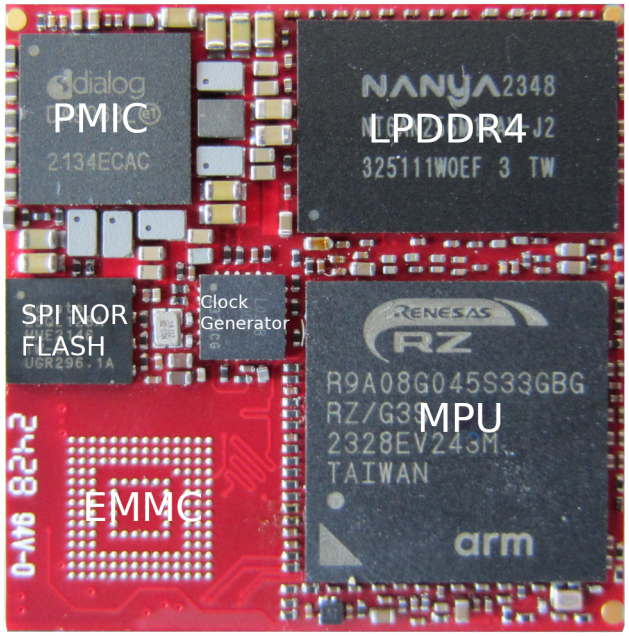
2.5 Dimensions



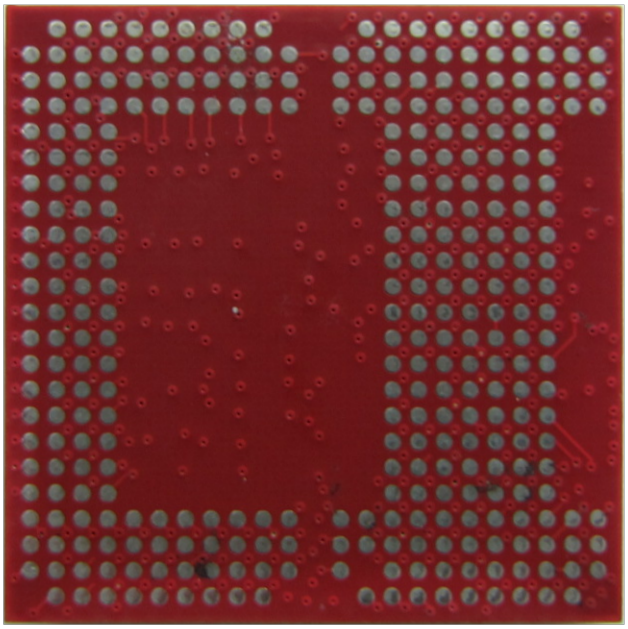


2.6 Part Overview

Assembly Top

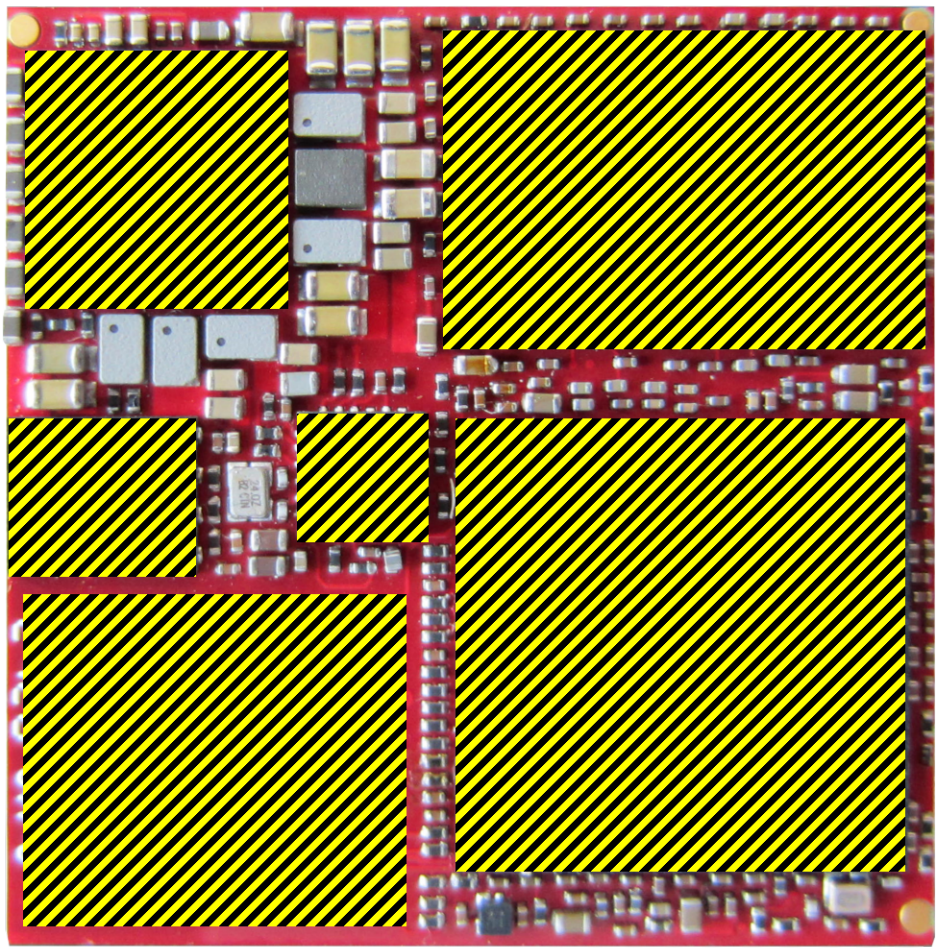


Assembly Bottom



2.7 Handling Recommendations

To avoid mechanical damage to the components populated on MSRZG3S it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

RESOURCES

3.1 Components

3.1.1 MPU

The R9A08G045S33GBG microprocessor is based on the high-performance Arm Cortex-A55 Single MPCore operating at up to 1.1 GHz and two Arm Cortex-M33 250MHz cores. One Cortex-M33 has FPU function. The Cortex-A55 processor includes a 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache, and a 256-Kbyte L3 cache.

Features	R9A08G045S33GBG
Package	BGA Package (14x14mm)
CPU	Arm Cortex-A55 Single MPCore 1.1 GHz two Arm Cortex-M33 Processors 250 MHz
On-chip RAM	1 MB (ECC)
LPDDR4 Memory	LPDDR4 or DDR4

For more information about the R9A08G045S33GBG microprocessor please refer to the documentation which is available from Renesas.

3.1.2 Boot table

Selection of Boot CPU

Signal Name	Function	Description
BOOTCPUSEL	BOOT CPU Select	Select the CPU to cold boot. 0:Cortex-M33 cold boot 1:Cortex-A55 cold boot

Selection of Boot Mode

Signal Name		Boot Mode	Interface Module	Connected Device	Cortex-A55 Cold Boot	Cortex-M33 Cold Boot
MD_BOOT1	MD_BOOT0					
0	0	Boot mode 0	SDHI0	eSD (3.3 V at startup)	O	X
0	1	Boot mode 1	SDHI0	1.8-V/3.3-V eMMC	O	X
1	0	Boot mode 2	xSPI	1.8-V/3.3-V Single, Quad, or Octal serial flash memory	O	O
1	1	Boot mode 3	SCIF0	Downloading through SCIF	O	O

Boot Device I/F Voltage Setting Pin

Signal Name	Function	Description
MD_BOOT2	Boot Device I/F Voltage Settings	Boot Device I/F Voltage Settings; This pin is valid only for boot mode 1 (eMMC) and boot mode 2 (Serial Flash Memory); 0: 3.3 V / 1: 1.8V

3.1.3 LPDDR4 SDRAM

The MSRZG3S is equipped with 1 block of Nanya NT6AN512M16AV-J2 LPDDR4 SDRAM. Device is available in the commercial temperature range -30°C…+105°C.

MPU Signals for LPDDR4

MPU Pin	Function	LPDDR4 Pin	MPU Pin	Function	LPDDR4 Pin
W27	DDR_CKE	J4	H23	DDR_DQ15	B9
U23	DDR_CS#	H4	H22	DDR_DM1	C10
U26	DDR_CK_P	J8	F27	DDR_DQS1_P	D10
U27	DDR_CK_N	J9	F26	DDR_DQS1_N	E10
P26	DDR_CA0	H2	AE27	DDR_RESET#	T11
R27	DDR_CA1	J2			
P24	DDR_CA2	H9			
P22	DDR_CA3	H10			
R26	DDR_CA4	H11			
U24	DDR_CA5	J11			
J26	DDR_DQ0	B2			
L27	DDR_DQ1	C2			
L26	DDR_DQ2	E2			
M26	DDR_DQ3	F2			
H26	DDR_DQ4	F4			
L25	DDR_DQ5	E4			
L22	DDR_DQ6	C4			
L23	DDR_DQ7	B4			
H27	DDR_DM0	C3			
K27	DDR_DQS0_P	D3			
K26	DDR_DQS0_N	E3			
E26	DDR_DQ8	B11			
D27	DDR_DQ9	C11			
D26	DDR_DQ10	E11			
C27	DDR_DQ11	F11			
H25	DDR_DQ12	F9			
H24	DDR_DQ13	E9			
G27	DDR_DQ14	C9			

3.1.4 eMMC Flash

The MSRZG3S offers the Kioxia THGBMTG5D1LBAIL, which is 4GB density of e-MMC Module product housed in 153 ball BGA package. This unit is utilized advanced NAND flash device(s) and controller chip assembled as Multi Chip Module. THGBMTG5D1LBAIL has an industry standard MMC protocol for easy use.

MPU Pin	Function	eMMC Pin
B25	EMMC_DATA0	A3
A25	EMMC_DATA1	A4
A24	EMMC_DATA2	A5
B24	EMMC_DATA3	B2
B23	EMMC_DATA4	B3
A23	EMMC_DATA5	B4
B22	EMMC_DATA6	B5
A22	EMMC_DATA7	B6
A26	EMMC_CMD	M5
A21	EMMC_CLK	M6
B21	EMMC_RST#	K5

3.1.5 SPI NOR FLASH

The MSRZG3S offers the Renesas AT25QL128A (128 Mbit) serial interface Flash memory device. The erase block sizes of the AT25QL128A have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently.The devices operate on a single 1.7 V to 2.0 V power supply with current consumption as low as 5 mA active and 2 uA for Deep Power-Down. SPI clock frequencies of up to 133 MHz are supported, allowing equivalent clock rates of 266 MHz for Dual Output, and 532 MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O commands. The device supports JEDEC standard manufacturer and device identification with a 4-kbit secured OTP.

MPU Pin	Function	SPI Pin
K2	QSPI_CS#	1
H1	QSPI_IO0	5
	QSPI_IO1	2
J1	QSPI_IO2	3
J2	QSPI_IO3	7
H3	QSPI_CLK	6

3.1.6 PMIC

Power on the MSRZG3S is controlled by a DA9063L-00 Dialog Semiconductor fully integrated power management IC designed for productsbased on high integrated application processor designs requiring low power and highefficiency. The DA9063L follows a scalable approach of output currents and rails to supply the entire system and is capable of delivering a total of up to 12 A from its six DC-DC buck converters.

The module must be supplied with the following voltage:

min. voltage	max. voltage
4.25 V	5.5 V

MPU Pin	Function	PMIC Pin	SiP Pads
–	PWR_BTN#	J7	AA9
–	PMIC_TP	D5	D6
–	PMIC_SDA	A7	P16
–	PMIC_SCL	A8	C16
AG4	SYS_RST#	D9	U17
AE1	RZ_NMI	B7	–
–	CARRIER_PWR_EN	E9	V17

3.1.7 Clock Generator

The MSRZG3S offers the Renesas 5L35023 clock generator designed for low-power, consumer, and high-performance PCI Express applications with 1.8V operation voltage. The 5L35023 device is a three-PLL architecture design, and each PLL is individually programmable and allows for up to five unique frequency outputs. It has built-in unique features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshot Reduction Technology (ORT), and Extreme Low Power DCO.An internal OTP memory allows the user to store the configuration in the device without programming after power-up, then program the 5L35023 again through the I2C interface. The device has programmable VCO and PLL source selection, allowing power-performance optimization based on the application requirements

MPU Pin	Function	Clock Generator Pin	SiP Pads
G5	I2C_A_DAT	2	AA16
G4	I2C_A_CLK	3	AA20
AC7	RZ_REFCLK_24	8	–
AF17	PCIE_REFCLK_P	18	–
AG17	PCIE_REFCLK_N	17	–
–	PCIE_REFCLK_OUT	24	W1
–	PCIE_REFCLK_OUT	23	Y1

3.2 Pin Out

3.2.1 USB

MPU Pin	Function	SiP Pin
AF10	USB_OTG_D_P	AC14
AG10	USB_OTG_D_N	AB13
AA3	USB_OTG_EN	AC16
AD1	USB_OTG_ID	AB14
AA4	USB_OTG_OC#	AC15
AF4	USB_OTG_VBUS	AB16
AF8	USB_HOST_D_P	AC22
AG8	USB_HOST_D_N	AB23
AA1	USB_HOST_EN	AC20
AD2	USB_HOST_OC#	AC21

3.2.2 CAN

MPU Pin	Function	SiP Pin
AF10	CAN_A_TX	AC17
Y3	CAN_A_RX	AB17
AF4	CAN_B_TX	AC19
AF8	CAN_B_RX	AB19

3.2.3 SDIO

MPU Pin	Function	SiP Pin
D21	SDIO_CLK	F21
C21	SDIO_CMD	E20
B4	SDIO_CD#	J21
C4	SDIO_WP	D20
E20	SDIO_DATA0	G20
D20	SDIO_DATA1	G21
C20	SDIO_DATA2	H20
B20	SDIO_DATA3	H21
AF8	SDIO_PWREN	D21

3.2.4 Ethernet

MPU Pin	Function	SiP Pin
D16	ETH_A_TX_CLK	J15
A19	ETH_A_TX_CTL	K16
B19	ETH_A_TXD0	H15
A18	ETH_A_TXD1	G15
B18	ETH_A_TXD2	H16
A17	ETH_A_TXD3	G16
A16	ETH_A_COL	F15
C16	ETH_A_CRS	E16
C12	ETH_A_RX_CLK	R15
B16	ETH_A_RX_CTL	M15
B15	ETH_A_RXD0	K15
A15	ETH_A_RXD1	L15
A14	ETH_A_RXD2	N15
B14	ETH_A_RXD3	P15
B13	ETH_A_RX_ER	L16
A13	ETH_A_MDC	T16
A12	ETH_A_MDIO	T15
F8	ETH_B_TX_CLK	H1
B11	ETH_B_TX_CTL	J2
A10	ETH_B_TXD0	G1
A9	ETH_B_TXD1	F1
B10	ETH_B_TXD2	G2
B9	ETH_B_TXD3	F2
B8	ETH_B_COL	E1
A8	ETH_B_CRS	D2
E7	ETH_B_RX_CLK	P1
D7	ETH_B_RX_CTL	L1
E8	ETH_B_RXD0	J1
D8	ETH_B_RXD1	K1
A7	ETH_B_RXD2	M1
B7	ETH_B_RXD3	N1
C8	ETH_B_RX_ER	K2
A6	ETH_B_MDC	C6
B6	ETH_B_MDIO	C7

3.2.5 JTAG

MPU Pin	Function	SiP Pin
Y1	JTAG_TCK	N17
W2	JTAG_TMS	N19
V2	JTAG_TDI	P17
Y2	JTAG_TDO	R17
W1	JTAG_TRST#	R19
AF21	JTAG_DBGEN	AC18

3.2.6 UART

MPU Pin	Function	SiP Pin
AB1	CONS_RX	D22
Y4	CONS_TX	D23
D1	UART_A_RX	A14
F2	UART_A_TX	B13
AC21	UART_A_RTS#	C13
AD21	UART_A_CTS#	C14
AD20	UART_B_RX	D14
AG25	UART_B_TX	D13

3.2.7 I2C

MPU Pin	Function	SiP Pin	Clock Generator Pin
G4	I2C_A_CLK	AA15	3
G5	I2C_A_DAT	AA16	2
H4	I2C_B_CLK	AA20	–
H5	I2C_B_DAT	AA21	–

3.2.8 I2S

MPU Pin	Function	SiP Pin
B2	I2S_A_DATA_IN	V21
A2	I2S_A_DATA_OUT	W21
A3	I2S_LRCLK	W18
B3	I2S_BITCLK	W20

3.2.9 SPI

MPU Pin	Function	SiP Pin
B2	SPI_A_SDI	U15
A2	SPI_A_SDO	V15
A3	SPI_A_CS0#	Y15
B3	SPI_A_SCK	U16

3.2.10 ADC

MPU Pin	Function	SiP Pin
T4	ADC_0	M18
U1	ADC_1	N18

3.2.11 PWM

MPU Pin	Function	SiP Pin
C1	PWM_0	E18
D2	PWM_1	F18

3.2.12 GPIO

MPU Pin	Function	SiP Pin
AE24	GPIO_A_0	D17
AF25	GPIO_A_1	E17
AA5	GPIO_A_2	F17
D3	GPIO_A_3	G17
F1	GPIO_A_4	H17
B5	GPIO_A_5	J17
B1	GPIO_A_6	K17
C2	GPIO_A_7	L17
AG26	GPIO_B_0	D19
AF26	GPIO_B_1	E19
AD25	GPIO_B_2	F19
AF27	GPIO_B_3	G19

3.2.13 Audio

MPU Pin	Function	SiP Pin
AF2	RZ_AUDIO_CLK1	E3
AG2	RZ_AUDIO_CLK2	E4

3.2.14 PCIE

MPU Pin	Function	SiP Pin	Clock Generator Pin
AF17	PCIE_REFCLK_P	–	18
AG17	PCIE_REFCLK_N	–	17
AF15	PCIE_TX_D_P	AC2	–
AG15	PCIE_TX_D_N	AC3	–
AF13	PCIE_RX_D_P	AB1	–
AG13	PCIE_RX_D_N	AB2	–
E2	PCIE_PERST#	V2	–
E1	PCIE_CLKREQ#	W2	–
–	PCIE_REFCLK_OUT_P	W1	24
–	PCIE_REFCLK_OUT_N	Y1	23

3.2.15 MSRZG3S SiP Pads

Connector J1

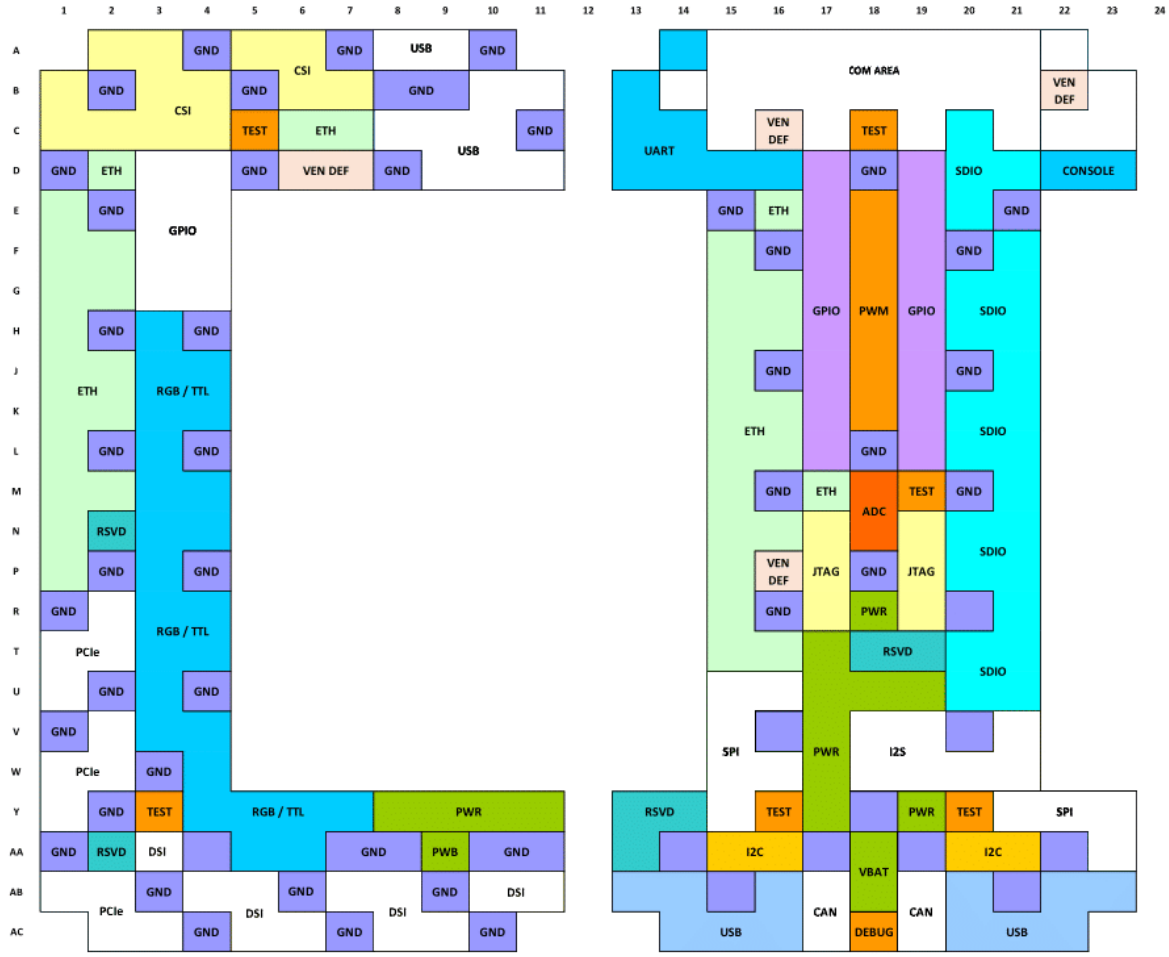


Fig. 1: Contact Overview

MPU Pin	Function	SiP Pads	MPU Pin	Function	SiP Pads
J1A			**J1B**		
D16	ETH_A_TX_CLK	J15	AA2	CAN_A_TX	AC17
B19	ETH_A_TXD0	H15	Y3	CAN_A_RX	AB17
A18	ETH_A_TXD1	G15	AG24	CAN_B_TX	AC19
B18	ETH_A_TXD2	H16	AF24	CAN_B_RX	AB19
A17	ETH_A_TXD3	G16	AF10	USB_OTG_D_P	AC14
A19	ETH_A_TX_CTL	K16	AG10	USB_OTG_D_N	AB13
C12	ETH_A_RX_CLK	R15	AA3	USB_OTG_EN	AC16
B15	ETH_A_RXD0	K15	AD1	USB_OTG_ID	AB14
A15	ETH_A_RXD1	L15	AA4	USB_OTG_OC#	AC15
A14	ETH_A_RXD2	N15	AF4	USB_OTG_VBUS	AB16

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads	MPU Pin	Function	SiP Pads
B14	ETH_A_RXD3	P15	AF8	USB_HOST_D_P	AC22
B13	ETH_A_RX_ER	L16	AG8	USB_HOST_D_N	AB23
B16	ETH_A_RX_CTL	M15	AA1	USB_HOST_EN	AC20
C16	ETH_A_CRS	E16	–	–	AB22
A16	ETH_A_COL	F15	AD2	USB_HOST_OC#	AC21
–	–	N16	–	–	AB20
A13	ETH_A_MDC	T16	–	–	D10
A12	ETH_A_MDIO	T15	–	–	D11
–	PVDD182533_0	M17	–	–	C10
F8	ETH_B_TX_CLK	H1	–	–	D9
A10	ETH_B_TXD0	G1	–	–	C8
A9	ETH_B_TXD1	F1	–	–	C9
B10	ETH_B_TXD2	G2	–	–	A9
B9	ETH_B_TXD3	F2	–	–	A8
B11	ETH_B_TX_CTL	J2	–	–	B11
E7	ETH_B_RX_CLK	P1	–	–	B10
E8	ETH_B_RXD0	J1	–	–	–
D8	ETH_B_RXD1	K1	–	–	–
A7	ETH_B_RXD2	M1	–	–	–
B7	ETH_B_RXD3	N1	–	–	–
C8	ETH_B_RX_ER	K2	–	–	–
D7	ETH_B_RX_CTL	L1	–	–	–
A8	ETH_B_CRS	D2	–	–	–
D8	ETH_B_COL	E1	–	–	–
–	–	M2	–	–	–
A6	ETH_B_MDC	C6	–	–	–
B6	ETH_B_MDIO	C7	–	–	–
J1C			**J1D**		
D21	SDIO_CLK	F21	AB1	CONS_RX	D22
C21	SDIO_CMD	E20	Y4	CONS_TX	D23
B4	SDIO_CD#	J21	D1	UART_A_RX	A14
C4	SDIO_WP	D20	F2	UART_A_TX	B13
E20	SDIO_DATA0	G20	AC21	UART_A_RTS#	C13
D20	SDIO_DATA1	G21	AD21	UART_A_CTS#	C14
C20	SDIO_DATA2	H20	AD20	UART_B_RX	D14
B20	SDIO_DATA3	H21	AG25	UART_B_TX	D13
A4	SDIO_PWREN	D21	–	–	D15
–	SD1_PVDD	C20	–	–	D16
–	–	K20	–	–	A22
–	–	K21	–	–	B23
–	–	T21	–	–	C22
–	–	U20	–	–	C23
–	–	L20	–	–	–
–	–	L21	–	–	–
–	–	M21	–	–	–
–	–	N20	–	–	–
–	–	N21	–	–	–
–	–	P20	–	–	–
–	–	P21	–	–	–

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads	MPU Pin	Function	SiP Pads
–	–	R21	–	–	–
–	–	U21	–	–	–
–	–	T20	–	–	–
J1E			**J1F**		
G4	I2C_A_CLK	AA15	T4	ADC_0	M18
G5	I2C_A_DAT	AA16	U1	ADC_1	N18
H4	I2C_B_CLK	AA20	C1	PWM_0	E18
H5	I2C_B_DAT	AA21	D2	PWM_1	F18
B2	I2S_A_DATA_IN	V21	–	–	G18
A2	I2S_A_DATA_OUT	W21	–	–	H18
–	–	V19	–	–	J18
–	–	W19	–	–	K18
–	–	V18	AE24	GPIO_A_0	D17
A3	I2S_LRCLK	W18	AF25	GPIO_A_1	E17
B3	I2S_BITCLK	W20	AA5	GPIO_A_2	F17
AG23	SPI_A_SDI	U15	D3	GPIO_A_3	G17
AC20	SPI_A_SDO	V15	F1	GPIO_A_4	H17
–	–	W16	B5	GPIO_A_5	J17
–	–	W15	B1	GPIO_A_6	K17
AF23	SPI_A_CS0#	Y15	C2	GPIO_A_7	L17
AF22	SPI_A_SCK	U16	AG26	GPIO_B_0	D19
–	–	Y22	AF26	GPIO_B_1	E19
–	–	Y23	AD25	GPIO_B_2	F19
–	–	AA23	AF27	GPIO_B_3	G19
–	–	Y21	–	–	H19
–	–	–	–	–	J19
–	–	–	–	–	K19
–	–	–	–	–	L19
–	–	–	–	–	D3
–	–	–	–	–	D4
–	–	–	AF2	RZ_AUDIO_CLK1	E3
–	–	–	AG2	RZ_AUDIO_CLK2	E4
–	–	–	–	–	F3
–	–	–	–	–	F4
–	–	–	–	–	G3
–	–	–	–	–	G4
J1G			**J1H**		
AD8	VBATTRESET#	B22	–	–	A15
–	PMIC_SCL	C16	–	–	A16
–	PMIC_SDA	P16	–	–	A17
–	PMIC_TP	D6	–	–	A18
AF20	BOOTCPUSEL	D7	–	–	A19
–	–	–	–	–	A20
–	–	–	–	–	A21
–	–	–	–	–	B15
–	–	–	–	–	B16
–	–	–	–	–	B17
–	–	–	–	–	B18

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads	MPU Pin	Function	SiP Pads
–	–	–	–	–	B19
–	–	–	–	–	B20
–	–	–	–	–	B21
–	–	–	–	–	C15
–	–	–	–	–	C17
–	–	–	–	–	C19
–	–	–	–	–	C21
J1I			**J1J**		
Y1	JTAG_TCK	N17	–	–	Y7
–	–	P19	–	–	AA6
W2	JTAG_TMS	N19	–	–	Y6
V2	JTAG_TDI	P17	–	–	AA5
Y2	JTAG_TDO	R17	–	–	Y5
W1	JTAG_TRST#	R19	–	–	Y4
AF21	JTAG_DBGEN	AC18	–	–	W4
–	–	C18	–	–	V3
–	–	–	–	–	V4
–	–	–	–	–	U3
–	–	–	–	–	T3
–	–	–	–	–	T4
–	–	–	–	–	R4
–	–	–	–	–	R3
–	–	–	–	–	P3
–	–	–	–	–	N3
–	–	–	–	–	N4
–	–	–	–	–	M3
–	–	–	–	–	M4
–	–	–	–	–	L3
–	–	–	–	–	K3
–	–	–	–	–	K4
–	–	–	–	–	J4
–	–	–	–	–	J3
–	–	–	–	–	H3
J1K			**J1L**		
–	–	AB11	–	–	C1
–	–	AB10	–	–	B1
–	–	AC9	–	–	A2
–	–	AC8	–	–	A3
–	–	AC6	–	–	A5
–	–	AC5	–	–	A6
–	–	AB5	–	–	B6
–	–	AB4	–	–	B7
–	–	AB8	–	–	B3
–	–	AB7	–	–	B4
–	–	AA3	–	–	C2
–	–	–	–	–	C3
–	–	–	–	–	C4

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads	MPU Pin	Function	SiP Pads
J1M			**J1N**		
AF13	PCIE_RX_D_P	AB1	–	5V0	Y17
AG13	PCIE_RX_D_N	AB2	–	–	Y19
AF15	PCIE_TX_D_P	AC2	–	RTC_PWR	W17
AG15	PCIE_TX_D_N	AC3	–	–	U18
E2	PCIE_PERST#	V2	–	–	AA18
E1	PCIE_CLKREQ#	W2	–	–	AB18
–	PCIE_REFCLK_OUT_P	W1	AG4	SYS_RST#	U17
–	PCIE_REFCLK_OUT_N	Y1	–	CARRIER_PWR_EN	V17
–	–	T2	AF19	BOOT_SEL0#	U19
–	–	U1	AE20	BOOT_SEL1#	R18
–	–	T1	–	–	T17
–	–	R2	–	–	M19
–	–	–	–	–	Y16
–	–	–	–	–	Y20
–	–	–	–	5V0	Y8
–	–	–	–	5V0	Y9
–	–	–	–	5V0	Y10
–	–	–	–	5V0	Y11
–	–	–	–	–	Y3
–	–	–	–	–	C5
–	–	–	–	PWR_BTN#	AA9
J1O					
–	GND	R16	–	GND	D18
–	GND	R20	–	GND	E15
–	GND	V16	–	GND	E21
–	GND	V20	–	GND	F16
–	GND	Y18	–	GND	F20
–	GND	AA14	–	GND	J16
–	GND	AA17	–	GND	J20
–	GND	AA19	–	GND	L18
–	GND	AA22	–	GND	M16
–	GND	AB15	–	GND	M20
–	GND	AB21	–	GND	P18
–	GND	R1	–	GND	A4
–	GND	U2	–	GND	A7
–	GND	U4	–	GND	A10
–	GND	V1	–	GND	B2
–	GND	W3	–	GND	B5
–	GND	Y2	–	GND	B8
–	GND	AA1	–	GND	B9
–	GND	AA4	–	GND	C11
–	GND	AA7	–	GND	D1
–	GND	AA8	–	GND	D5
–	GND	AA10	–	GND	D8
–	GND	AA11	–	GND	E2
–	GND	AB3	–	GND	H2
–	GND	AB6	–	GND	H4
–	GND	AB9	–	GND	L2

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads	MPU Pin	Function	SiP Pads
–	GND	AC4	–	GND	L4
–	GND	AC7	–	GND	P2
–	GND	AC10	–	GND	P4
J1P					
–	–	T18	–	–	–
–	–	T19	–	–	–
–	–	Y13	–	–	–
–	–	Y14	–	–	–
–	–	AA13	–	–	–
–	–	N2	–	–	–
–	–	AA2	–	–	–

3.3 Schematics

Schematics for the MSRZG3S SiP may be obtained on request.