MSRZG3E Hardwaremanual

Version: **1.0**

Created on: Aug 07, 2025

Created by: Felix Widder

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	07.08.2025	fw	Initial creation

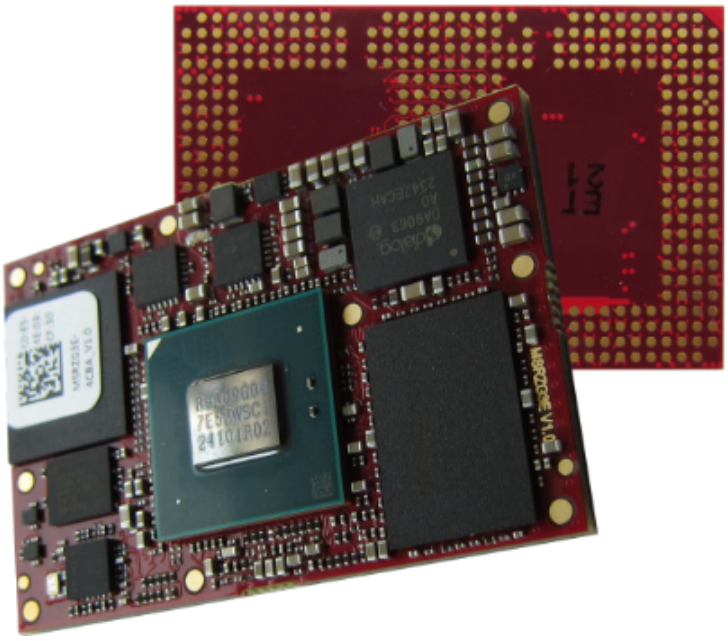
CHAPTER

TWO

OVERVIEW

2.1 MSRZG3E System In Package

The MSRZG3E is the Open Standard Module (OSM) compliant System-In-Package based on Renesas RZ Family architecture offering high-performance quad core Cortex-A55, a Cortex-M33 core as well as an Ethos-U55 NPU. The MSRZG3E combines robust industrial interfaces with ambitous multimedia features in a single architecture.



The chosen OSM form factor 'size M' supports 476 contacts, on a module size of just 30x45 mm^2. It offers almost all of the CPU functionality on the contacts and is therefore suitable for most industrial applications.

2.2 Feature Set

- Dual/Quad Cortex-A55, up to 1.8GHz
- Cortex-M33, up to 200MHz
- Ethos-U55 NPU, 1GHz, optional
- 512MB – 8GB LPDDR4 RAM
- 4GB – 64GB eMMC NAND Flash
- RGB and MIPI-DSI
- MIPI-CSI camera interface, 1, 2 or 4 lanes
- Video Codec Unit, H.264/H.265 encoding / decoding
- Frame Data Processor
- Video Signal Processor
- scaling, image rotation
- Color space conversion, color keying
- PCIe, 1 port Gen3 x2
- Dual 10/100/1000MBit Ethernet
- USB2.0 Host/OTG
- USB3.2 Host
- 2x CANFD
- UART, I2C, SPI, ADC, DAC
- compliant to the SGET OSM standard
- sizeM, 30x45mm, 476 contacts
- 0°C..+70°C commercial temperature range
- -40°C..+85°C industrial temperature range

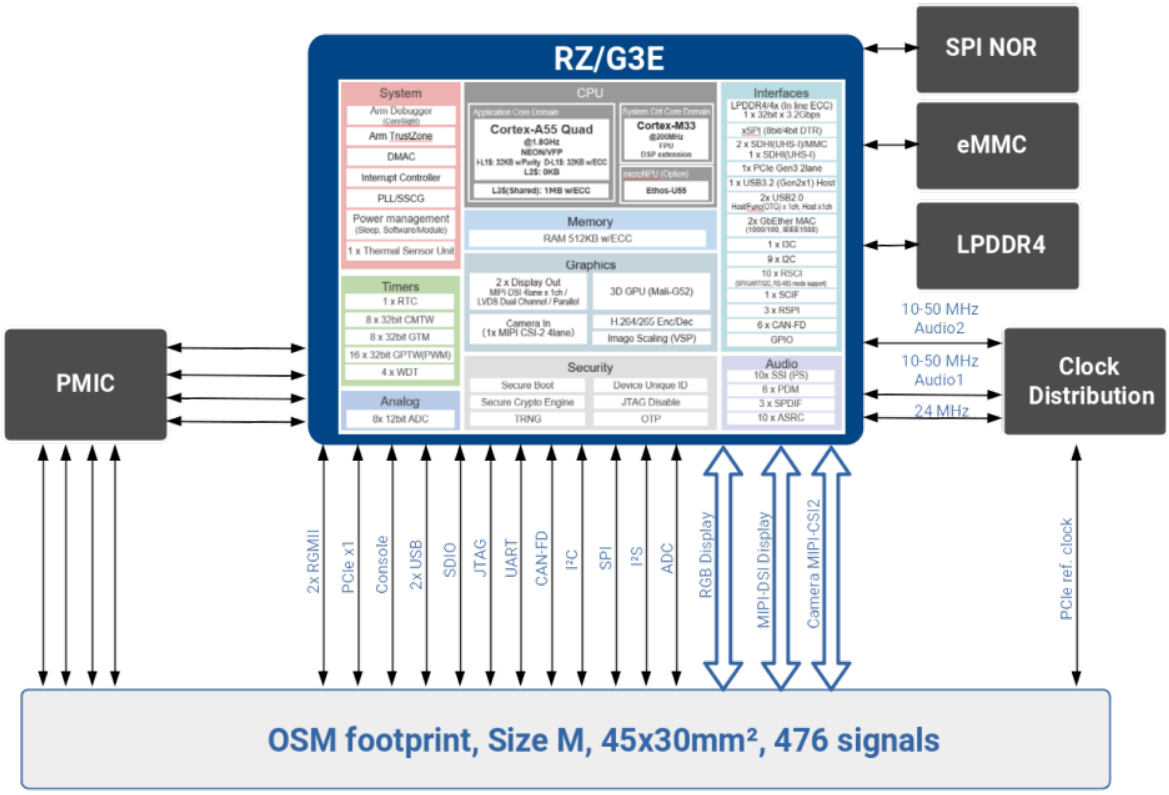
2.3 Order Codes

The MSRZG3E is only available in the following standart configuration:

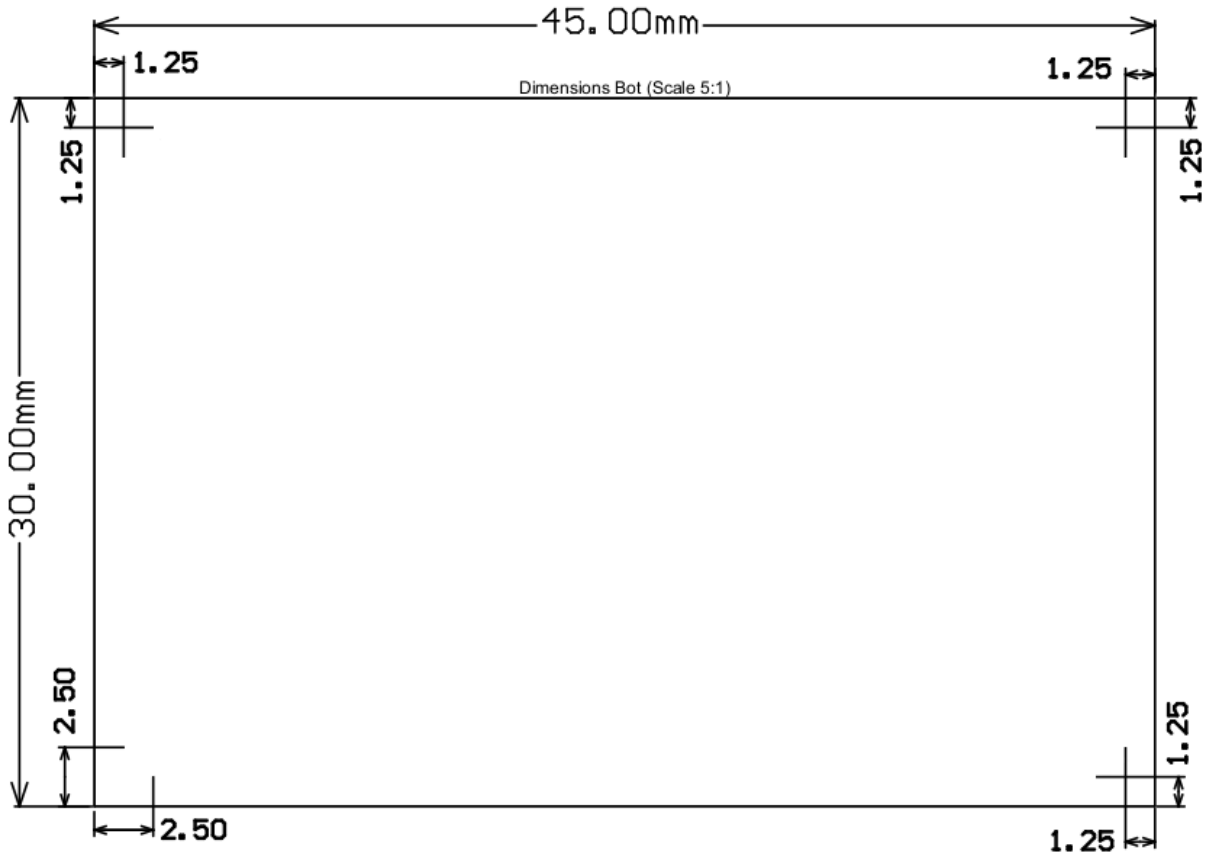
MSRZG3E-4CBA

- R9A09G047E57GBG CPU
  - Ethos-U55
  - 4x Cortex-A55, up to 1.8GHz
  - 1x Cortex-M33, up to 200MHz
  - 2GB LPDDR4 RAM
- 8GB eMMC NAND flash
- 128MBit SPI NOR
- 0°C..+70°C

2.4 Block Diagramm

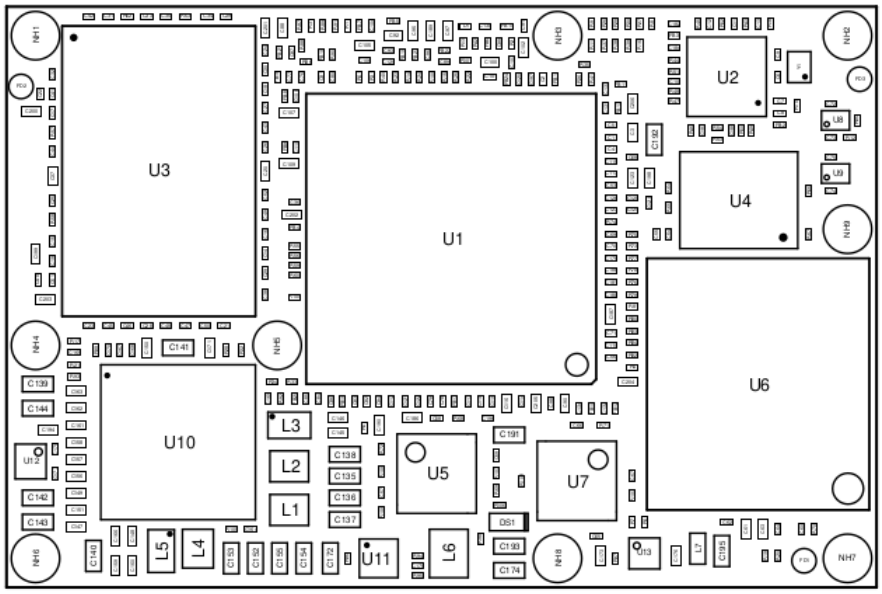


2.5 Dimensions



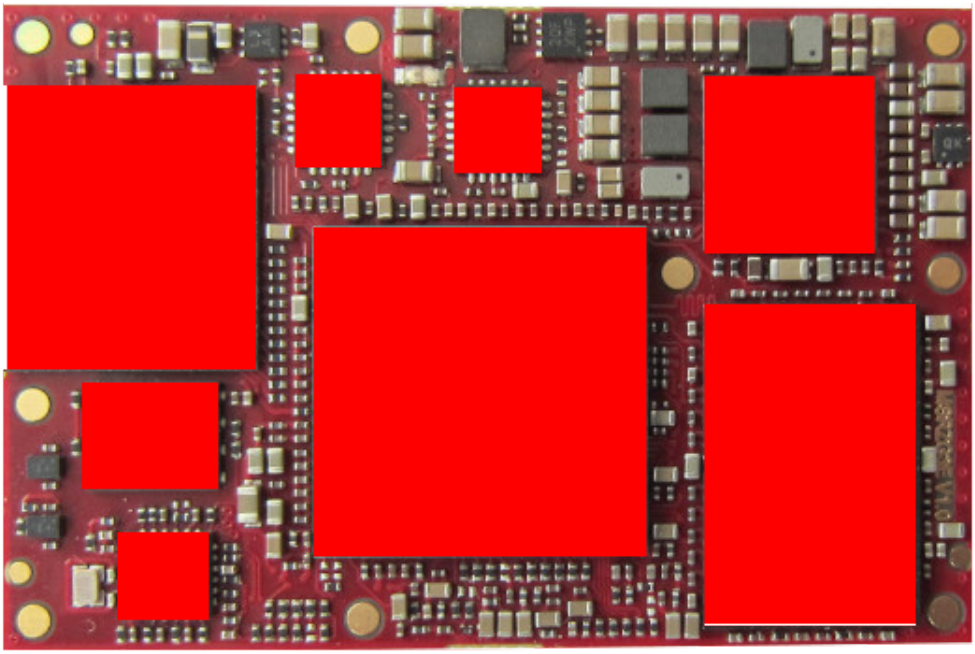
2.6 Part Overview

Assembly Top



2.7 Handling Recommendation

To avoid mechanical damage to the components populated on MSRZG3E it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) and or other sensible components. The BGA and other components are marked as shaded in the figure below:



CHAPTER

THREE

OPEN STANDARD MODUL (OSM)

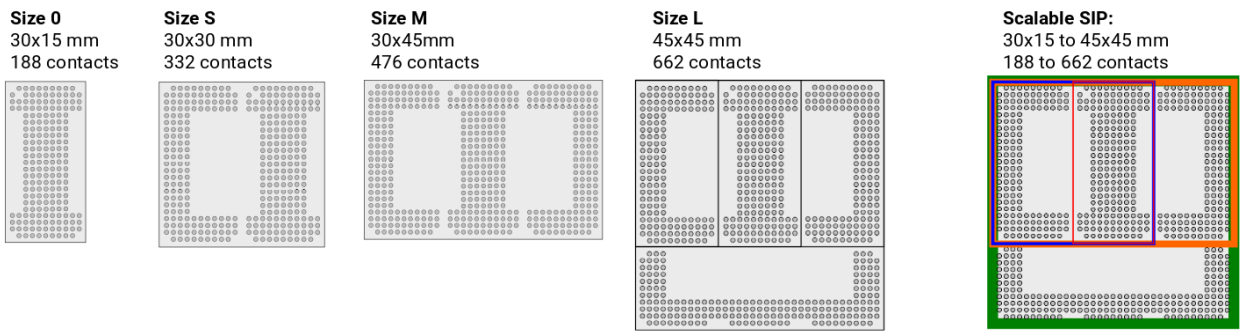
The idea of all Open Standard Modules™ is to create a new, future proof and versatile standard for small-size, low-cost embedded computer modules, combining the following key characteristics:

- Completely machine processible during soldering, assembly and testing
- Pre-tinned LGA package for direct PCB soldering without connector
- Pre-defined soft- and hardware interfaces
- Open-Source in soft- and hardware

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

3.1 Module Sizes and Dimensions

OSM SoMs are highly scalable in size, performance and functionality as they are available in different mechanical sizes and contact count:



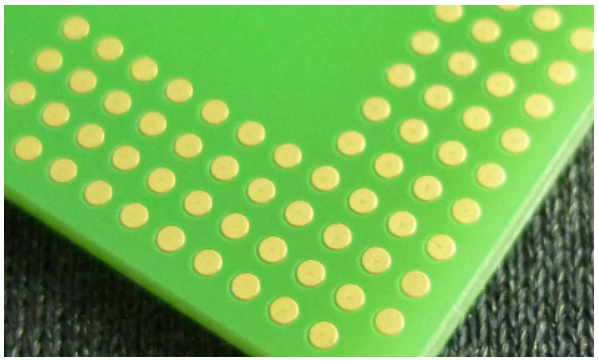
Size	Metrics	Contact Count	Colour Outline
Size-0 – “Zero”	30 mm x 15 mm	188 contacts	red
Size-S – “Small”	30 mm x 30 mm	332 contacts	blue
Size-M – “Medium”	30 mm x 45 mm	476 contacts	orange
Size-L – “Large”	45 mm x 45 mm	662 contacts	green

3.2 Contact Characteristics:

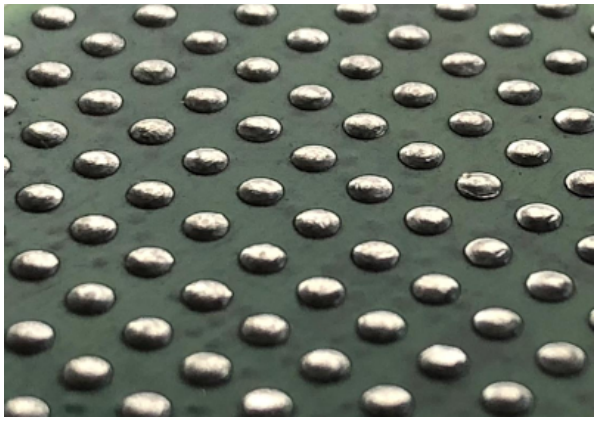
OSM SoMs are available with different contact characteristics:

3.2.1 ENIG-LGA

All OSM-SoMs by ARIES Embedded are using ENIG-LGA contacts on its PCBs:



3.2.2 Fused Tin Grid Array

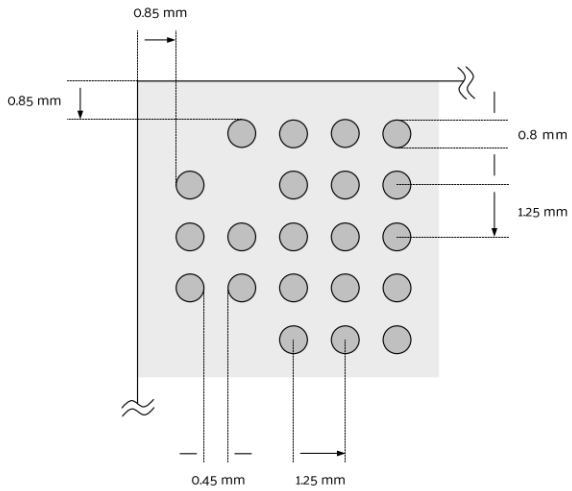


3.2.3 BGA

3.3 Contact Grid

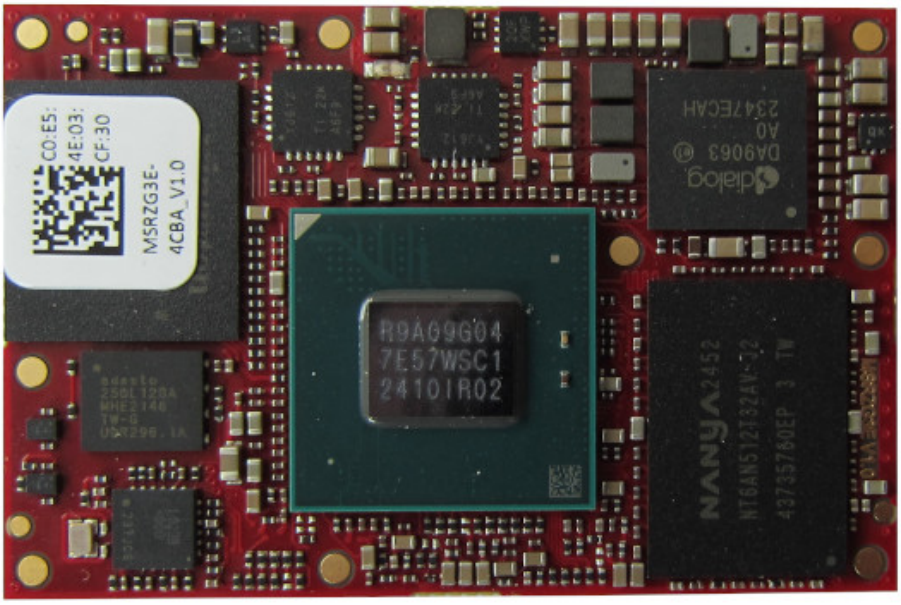
The Contact Grid for the Open Standard Module™ Specification is symmetrically and defines the following dimensions:

- Contact Diameter: 0.8 mm
- Contact Grid: 1.25 mm
- Contact-to-Contact: 0.45 mm
- Contact-to-Edge: 0.85 mm

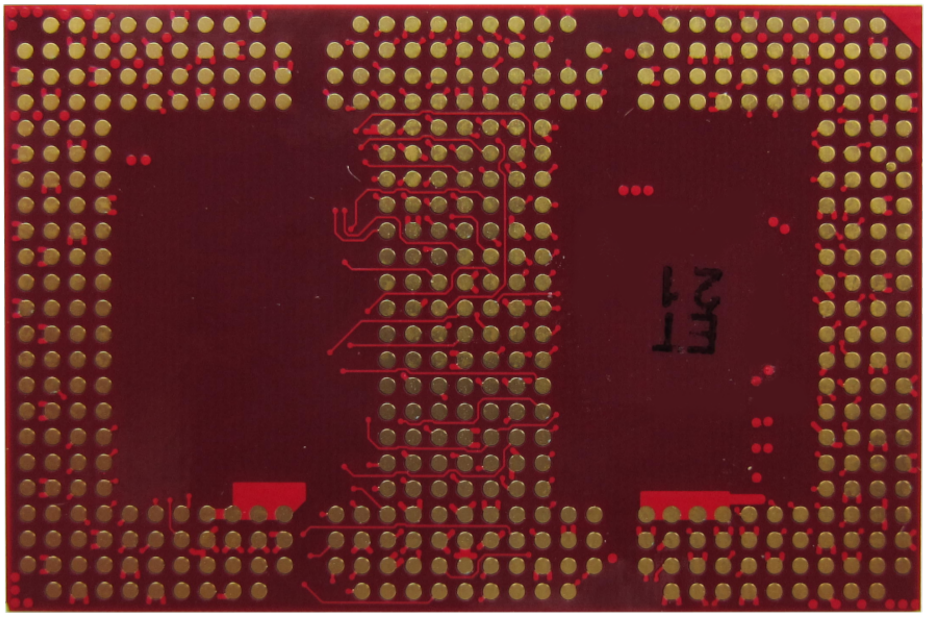


3.4 Recommendations for Processing OSM System on Modules

In the following the MSRZG3E will be used as a reference.



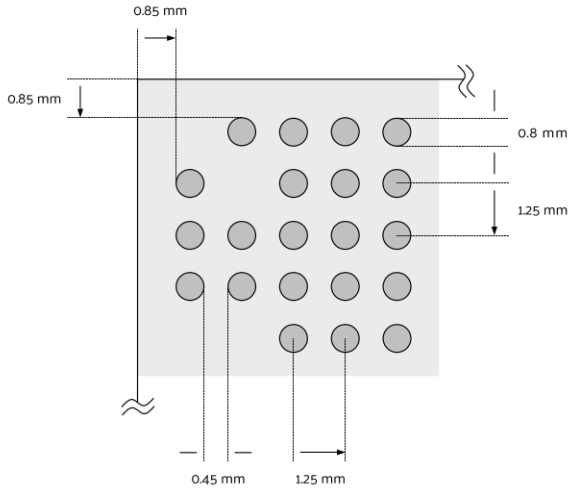
MSRZG3E is available as a LGA476 package with round flat pads on the solder side of the SoM:



3.4.1 Design

3.4.1.1 Layout PCB

The connecting pad size of the baseboard layout should be similar to the layout of e.g. the MSRZG3E baseboard. The pad size is defined with 0.8mm, the pitch 1.25mm.



3.4.1.2 Stencil

The stencil should have a with of 120µm. The openings in the stencil should be round shape with a diameter of 0.8mm, accordingly.

3.4.2 Process Recommendation

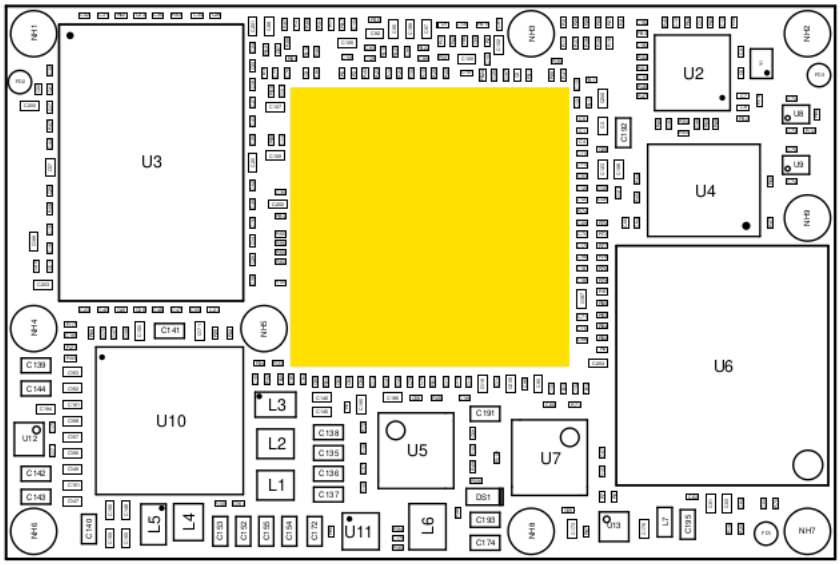
3.4.2.1 Storage

The OSM SoMs are to be handeled as moisture sensitive components. The SoMs shall be stored in suitable vacuum packages with dry packs.

The processing of the SoMs with opened package is limited to 168 hours at a maximum of 30°C and 60% air moisture. In case these values are exceeded and additional drying is necessary, the requirements of J-STD-033 have to be considered.

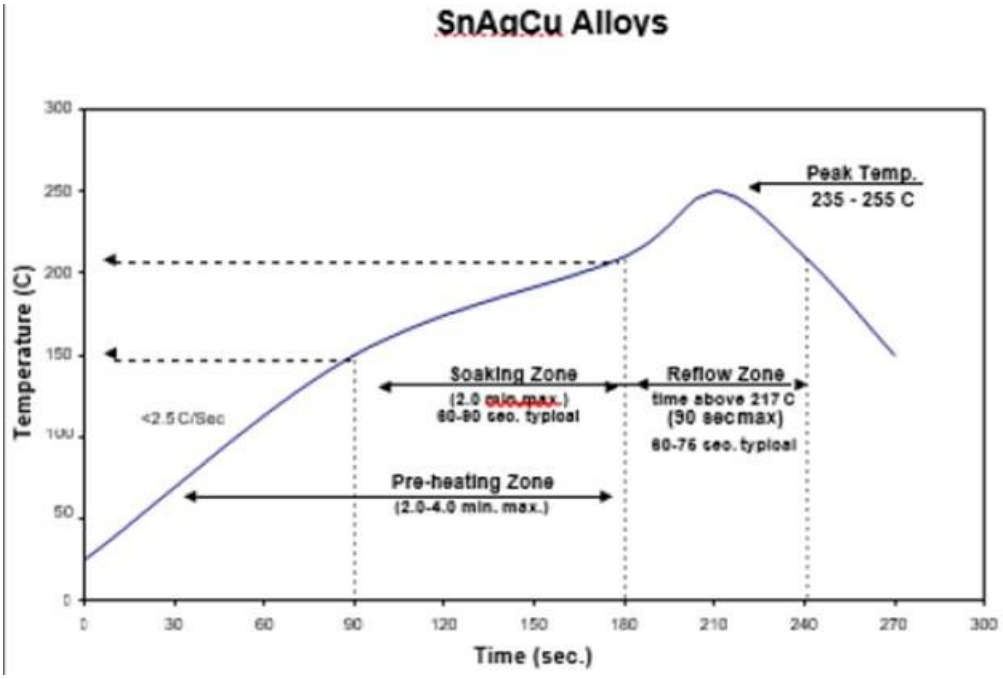
3.4.2.2 Production

For mounting the OSM SoMs the SoMs will be offered to the SMT machine in a tray or a reel. For the pickup of the SoM, using a vacuum nozzle, the SoM should be picked up by using a mechanical point as much as possible in the middle of the SoM, e.g. on U2 (yellow marking).



3.4.2.3 Reflow Soldering

The SoM can be soldered in a reflow soldering process, using a standard RoHS profile. Below picture show the recommendation for the solder paste Kester NP545.



3.5 OSM Design Guide

The primary purpose of OSM Design Guide is to serve as a suggestion for developers of OSM Carrier Boards and for OSM Module customers who wish to have a OSM based system developed. The document should also be valuable to FAEs and Product managers to help them understand the OSM Module infrastructure.

The OSM Design Guide is avaible for download (after registration) under https://sget.org/standards/osm/

CHAPTER

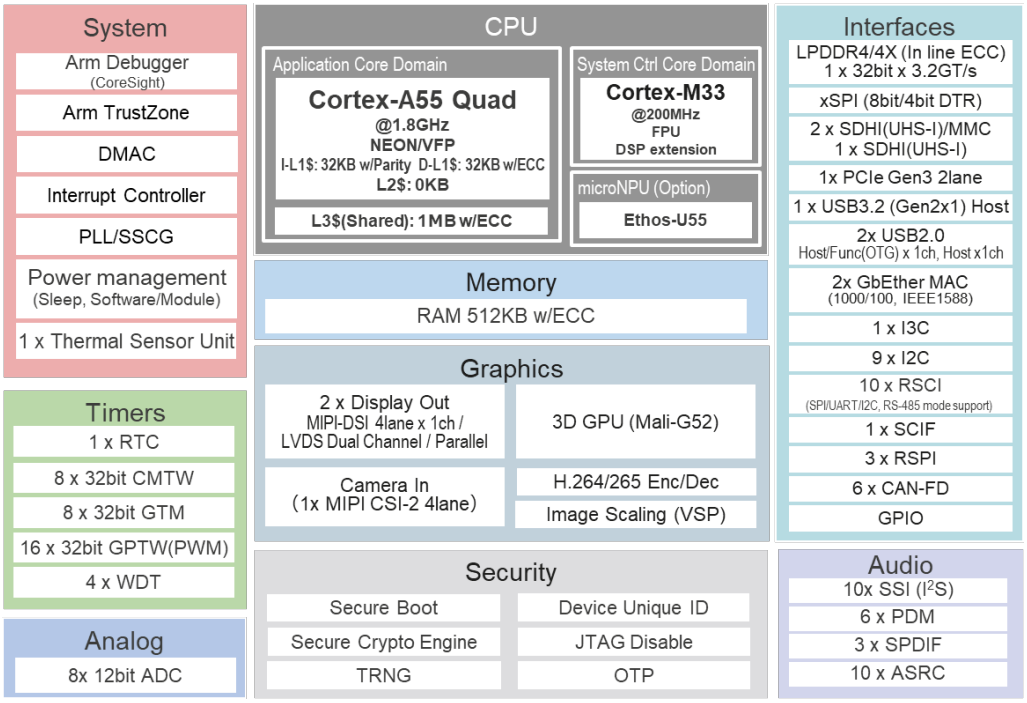
FOUR

RESOURCES

4.1 Components

4.2 MPU

RZ/G3E is a microprocessor (MPU) integrated with quad CPU and NPU in one chip, improving power efficiency, reliability, and security for human machine interface (HMI) applications. The RZ/G3E offers rich HMI functions including graphics engine (GPU), video codec, multi-screen full HD output, and Neural Processing Unit (NPU) for edge computing functions. In addition to the Cortex-A55 quad core delivering a powerful 1.8GHz to run both HMI and edge computing functions, RZ/G3E also features a Cortex-M33 core to enable low power operation. The combination of two different cores enables users to build products with both high performance and low power consumption.



For more information about the RZ/G3E microprocessor please refer to the documentation wich is available from Renesas

4.2.1 Bootmodes

MPU Pin	Function	OSM Pads	Notes
AE16	MD_BOOT0	U19	
AC14	MD_BOOT1	R18	
AB14	MD_BOOT2	Y29	Pullup 10k0
AE14	BOOTCPUSEL	D7	1:CA55 cold boot

Signal Name			Mode	Selected Module	Selected Device
MD_BOOT2	MD_BOOT1	MD_BOOT0			
0	0	0	Boot Mode 0	SD/eMMC ch0	eSD(3.3V for execution)
0	1	1	Boot Mode 3	SCIF ch0	SCIF download
1	0	0	Boot Mode 4	USB2.0 ch0	USB download
1	0	1	Boot Mode 5	SD/eMMC ch0	eMMC (IO voltage is 1.8V)
1	1	0	Boot Mode 6	xSPI	Serial flash memory (IO voltage is 1.8V)

Note:If reading or writing data from the oposite device fails, the Bootmode shifts to SCIF download. **Note**: The eSD must be mounted on the board only when using Boot Mode 0. While an SD card can be used in this mode, it is intended for evaluation purposes only. The error reset function is not supported when operating with an SD card.

For further information regarding this topic, refer to RENESAS's documentation (link valid as of June 30, 2025).

4.2.2 LPDDR4 RAM

The MSRZG3E is equipped with one block of NANYA NT6AN512T32AV-J2 LPDDR4 RAM providing up to 8 Gb of 32 bit memory. The device is designed for the commercial temperature range of -30°C to +105°C. The memory interface operates at a data rate of up to 3773 Mbps clocked at 1866 MHz

4.2.2.1 MPU Signals for LPDDR4 RAM

MPU Pin	FUNCTION	DDR4L Pin	MPU Pin	FUNCTION	DDR4L Pin	Notes
W28	DDR_DQA0	B2	R26	DDR_CAA3	H10	
Y28	DDR_DQA1	C2	U29	DDR_CAA4	H11	
AA28	DDR_DQA2	E2	U28	DDR_CAA5	J11	
Y29	DDR_DQA3	F2	N28	DDR_CAB0	R2	
AB29	DDR_DQA4	F4	M29	DDR_CAB1	P2	

continues on next page

Table 1 – continued from previous page

MPU Pin	FUNCTION	DDR4L Pin	MPU Pin	FUNCTION	DDR4L Pin	Notes
AB28	DDR_DQA5	E4	M28	DDR_CAB2	R9	
W22	DDR_DQA6	C4	L29	DDR_CAB3	R10	
W23	DDR_DQA7	B4	L28	DDR_CAB4	R11	
AC29	DDR_DQA8	B11	K29	DDR_CAB5	P11	
AA24	DDR_DQA9	C11	W26	DDR_DQSA0_P	D3	
AC28	DDR_DQA10	E11	W25	DDR_DQSA0_N	E3	
AE29	DDR_DQA11	F11	AC26	DDR_DQSA1_P	D3	
AE28	DDR_DQA12	F9	AC25	DDR_DQSA1_N	E3	
AA23	DDR_DQA13	E9	AA29	DDR_DMIA0	C3	
AD28	DDR_DQA14	C9	AD29	DDR_DMIA1	C10	
AA25	DDR_DQB0	B9	L26	DDR_DQSB0_P	W3	
J29	DDR_DQB0	AA2	L25	DDR_DQSB0_N	V3	
H28	DDR_DQB1	Y2	G26	DDR_DQSB1_P	W10	
H29	DDR_DQB2	V2	G25	DDR_DQSB1_N	V10	
J28	DDR_DQB3	U2	G29	DDR_DMIB0	Y3	
G28	DDR_DQB4	U4	C29	DDR_DMIB1	Y10	
F29	DDR_DQB5	V5	R29	DDR_CKA_P	J8	
J26	DDR_DQB6	Y4	R28	DDR_CKA_N	J9	
F28	DDR_DQB7	AA4	R20	DDR_CKEA0	J4	Pullup 33R0
E29	DDR_DQB8	AA11	N21	DDR_CKEA1	J5	Pullup 33R0
E27	DDR_DQB9	Y11	R24	DDR_CSA0	H4	
D29	DDR_DQB10	V11	U25	DDR_CSA1	H3	
B29	DDR_DQB11	U11	P29	DDR_CKB_P	P8	
E26	DDR_DQB12	U9	P28	DDR_CKB_N	P9	
D26	DDR_DQB13	V9	L20	DDR_CKEB0	P4	Pullup 33R0
C28	DDR_DQB14	Y9	L22	DDR_CKEB1	P5	Pullup 33R0
D28	DDR_DQB15	AA9	N24	DDR_CSB0	R4	
V29	DDR_CAA0	H2	N25	DDR_CSB1	R3	
V28	DDR_CAA1	J2	J23	DDR_RESETN	T11	Pulldown GND 10k0
R25	DDR_CAA2	H9	V18			Pulldown GND 120R

4.2.3 SPI NOR

MSRZG3E features a SPI-NOR device with a capacity of 128Mbits

THe SPI-NOR flash device uses the following connections:

MPU Pin	Function	SPIN-NOR Pin	Remarks
AA7	QSPI_IO0	5	
AA4	QSPI_IO1	2	
AB1	QSPI_IO2	3	Pullup 10k0
AA8	QSPI_IO3	7	Pullup 10k0
AC2	QSPI_CS#	1	Pullup 10k0
AE2	QSPI_CLK	6	Pullup 10k0

4.2.4 eMMC flash

The MSRZG3E supports one eMMC NAND Flash in the range of 4-64 GByte. The eMMC provides a high-speed memory card interface compliant with JEDEC Version 5.1, eliminating the need for users to be concerned about directly controlling Flash Memories.

If eMMC is selected(SD0_DEV_SEL = 1), the following table applies

MPU Pin	Signal	eMMC Pin
G2	SD0_DATA0	A3
J6	SD0_DATA1	A4
F1	SD0_DATA2	A5
F2	SD0_DATA3	B2
E2	SD0_DATA4	B3
J8	SD0_DATA5	B4
D1	SD0_DATA6	B5
D2	SD0_DATA7	B6
E1	SD0_CLK	M6
C1	SD0_CMD	M5
J7	SD0_RST#	K5

4.2.5 SDIO

If the SD-card is selected(SD0_DEV_SEL = 0), the following table applies

MPU Pin	Function	OSM Pads
E1	SD0_CLK	F21
C1	SD0_CMD	E20
G2	SD0_DATA0	G20
J6	SD0_DATA1	G21
F1	SD0_DATA2	H20
F2	SD0_DATA3	H21
AG1	SD0_PWEN	D21

4.2.6 PMIC

The MSZG3E uses the DA9063-A0HO1 to provide efficient power management across its components.

PMIC pin	Signal	OSM Pads	MPU Pin
J7	PWR_BTN#	AA9	
D5	PMIC_TP	D6	
A7	PMIC_SDA	P16	
A8	PMIC_SCL	C16	
A5	I2C_PM_DAT		AH3
B4	I2C_PM_CLK		AF10
D9	SYS_RST#	U17	
B7	PMIC_INT#		AG12
B9	PWEN0		AC16
C9	PWEN1		AB16
B10	PWEN2		AA16
A9	WDTUDF		AF2

4.3 Interfaces

4.3.1 I2C

MPU Pin	Function	OSM Pads
AH5	I2C_A_CLK	AA15
AG10	I2C_A_DAT	AA16
AH3	I2C_PM_CLK	AA20
AF10	I2C_PM_DAT	AA21

4.3.2 RGB

MPU Pin	Function	OSM Pads
B7	LCD_DISP	K4
B9	LCD_RESET#	J3
A12	LCD_CLK	M4
K12	LCD_HSYNC	K3
B13	LCD_VSYNC	L3
L12	LCD_DE	J4
K18	LCD_R2	Y7
E16	LCD_B2	R4
F18	LCD_G2	W4
F16	LCD_R3	AA6
G18	LCD_B3	R3
G16	LCD_G3	V3
H16	LCD_R4	Y6
J16	LCD_B4	P3
G14	LCD_G4	V4
J14	LCD_R5	AA5
A13	LCD_B5	N3
B14	LCD_G5	U3
F14	LCD_R6	Y5
H14	LCD_B6	N4
A14	LCD_G6	T3
E12	LCD_R7	Y4
F12	LCD_B7	M3
B12	LCD_G7	T4

4.3.3 UART

POWER

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
AH2	SCIF_RXD	D22	AJ2	UART_B_TX	D13
AH1	SCIF_TXD	D23	–	–	D15
Y2	UART_A_RX	A14	–	–	D16
W9	UART_A_TX	B13	–	–	A22
W8	UART_A_RTS	C13	–	–	A23
W7	UART_A_CTS	C14	–	–	C22
AJ3	UART_B_RX	D14	–	–	C23

4.3.4 PCIE

MPU Pin	Function	OSM Pad	Notes
AJ24	PCIE_A_RX_P	AB1	–
AH24	PCIE_A_RX_N	AB2	–
AJ23	PCIE_A_TX_P	AC2	–
AH23	PCIE_A_TX_N	AC4	–
A2	PCIE_PERST#	V2	–
E10	PCIE_CLKREQ#	W2	–
–	PCIE_REFCLK_OUT1_P	W1	Connected to Clock(24)
–	PCIE_REFCLK_OUT1_N	Y1	Connected to Clock(23)
AB10	PCIE_WAKE#	T2	–
AJ20	PCIE_B_RX_P	L34	–
AH21	PCIE_B_RX_N	M34	–
AJ19	PCIE_B_TX_P	K35	–
AH19	PCIE_B_TX_N	L35	–

4.3.5 ETHERNET

MSZG3E provides two Gigabit Ethernet interfaces

ETHERNET A			ETHERNET B		
MPU Pin	Function	OSM Pads	MPU Pin	Function	OSM Pads
U7	ETH_A_TX_CTL	K16	N6	ETH_B_TX_CTL	J2
U3	ETH_A_TX_CLK	J15	K2	ETH_B_TX_CLK	H1
U6	ETH_A_TXD0	H15	L3	ETH_B_TXD0	G1
P2	ETH_A_TXD1	G15	H2	ETH_B_TXD1	F1
R2	ETH_A_TXD2	H16	J1	ETH_B_TXD2	G2
P1	ETH_A_TXD3	G16	H1	ETH_B_TXD3	F2
V2	ETH_A_RX_CTL	M15	N1	ETH_B_RX_CTL	L1
R1	ETH_A_RX_CLK	R15	K1	ETH_B_RX_CLK	P1
R3	ETH_A_RXD0	K15	L6	ETH_B_RXD0	J1
R6	ETH_A_RXD1	L15	L7	ETH_B_RXD1	K1
R7	ETH_A_RXD2	N15	J2	ETH_B_RXD2	M1
U8	ETH_A_RXD3	P15	G1	ETH_B_RXD3	N1
U9	ETH_A_MDIO	T15	M2	ETH_B_MDIO	C7
U2	ETH_A_MDC	T16	M1	ETH_B_MDC	C6

4.3.6 JTAG

MPU Pin	Function	OSM Pads
AD12	JTAG_TMS	N19
AC12	JTAG_TCK	N17
AB12	JTAG_TDO	R17
W12	JTAG_TDI	P17
AE12	JTAG_TRST#	R19

4.3.7 CAN

MPU Pin	Function	OSM Pad
AD2	CAN_A_TX	AC17
AE1	CAN_A_RX	AB17
W4	CAN_B_TX	AC19
W1	CAN_B_RX	AB19

4.3.8 USB

MSZG3E provides three USB interfaces.

4.3.8.1 USB OTG

MPU Pin	Function	OSM Pad	Notes
AJ17	USB_OTG_D_P	AC14	–
AH17	USB_OTG_D_N	AB13	–
AJ4	USB_OTG_VBUS_EN	AC16	–
AE24	USB_OTG_ID	AB14	Pullup 10k0
AH4	USB_OTG_OC#	AC15	Pullup 10k0
AC22	USB_OTG_VBUS	AB16	30k0 serial resistor

4.3.8.2 USB HOST

MPU Pin	Function	OSM Pad
AJ16	USB_HOST_D_P	AC22
AH16	USB_HOST_D_N	AB23
C2	USB_HOST_VBUS_EN	AC20
B1	USB_HOST_OC#	AC21

4.3.8.3 USB 3.2

MPU Pin	Function	OSM Pad
AJ15	USB_C_D_P	D10
AH15	USB_C_D_N	D11
AH14	USB_C_SSTX_N	A9
AJ14	USB_C_SSTX_P	A8
AH13	USB_C_SSRX_N	B11
AJ12	USB_C_SSRX_P	B10

4.3.9 ADC/PWM/GPIO

MPU Pin	Function	OSM Pads
AH8	ADC_0	M18
AJ8	ADC_1	N18
AC5	DISP_BL_PWM	E18
Y1	GPIO_A_0	D17
W1	GPIO_A_1	E17
W5	GPIO_A_2	F17
W2	GPIO_A_3	G17
W3	GPIO_A_4	H17
W6	GPIO_A_5	J17
N8	GPIO_A_6	K17
G3	GPIO_A_7	L17
V1	GPIO_B_0	D19
T2	GPIO_B_1	E19
U1	GPIO_B_2	F19
T1	GPIO_B_3	G19
AC1	GPIO_C4/DISP_VDD_EN	F3
AC3	GPIO_C5/DISP_BL_EN	F4
L2	GPIO_C6/CAM_PWR	G3
N2	GPIO_C7/CAM_RST#	G4

4.3.10 DSI

MPU Pin	Function	OSM Pads
B24	DSI_DATA0_N	AB11
A24	DSI_DATA0_P	AB10
B25	DSI_DATA1_N	AC9
A25	DSI_DATA1_P	AC8
B27	DSI_DATA2_N	AC6
A27	DSI_DATA2_P	AC5
F24	DSI_DATA3_N	AB5
E24	DSI_DATA3_P	AB4
B26	DSI_DCLK_N	AB8
A26	DSI_DCLK_P	AB7

4.3.11 CSI

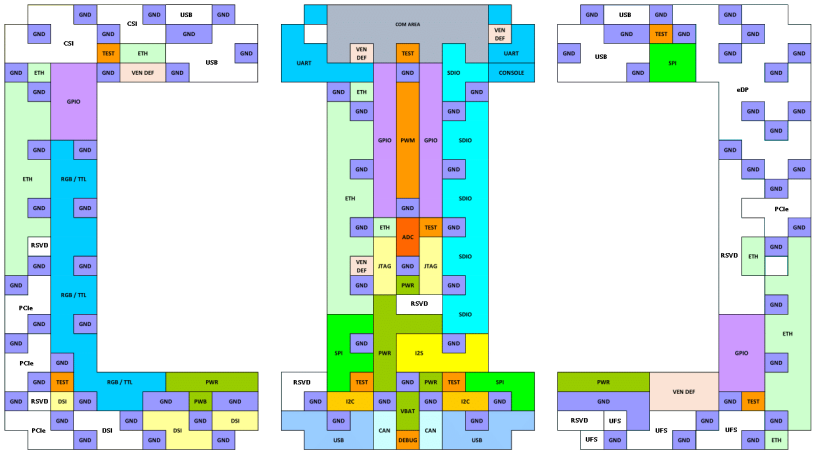
MPU Pin	Function	OSM Pad	Notes
AH25	CSI0_DATA0_N	C1	
AJ26	CSI0_DATA0_P	B1	
AH27	CSI0_DATA1_N	A2	
AJ27	CSI0_DATA1_P	A3	
AG28	CSI0_DATA2_N	A5	
AH29	CSI0_DATA2_P	A6	
AG29	CSI0_DATA3_N	B6	
AF28	CSI0_DATA3_P	B7	
AH28	CSI0_CLK_N	B3	
AJ28	CSI0_CLK_P	B4	
	CAM_MCK	C2	Connected to CLOCK(Pin 12), Pullup 33R0
L1	I2C_CAM_SDA	C3	Pullup 2k20
N7	I2C_CAM_SCL	C4	Pullup 2k20

4.3.12 POWER / SYSTEM

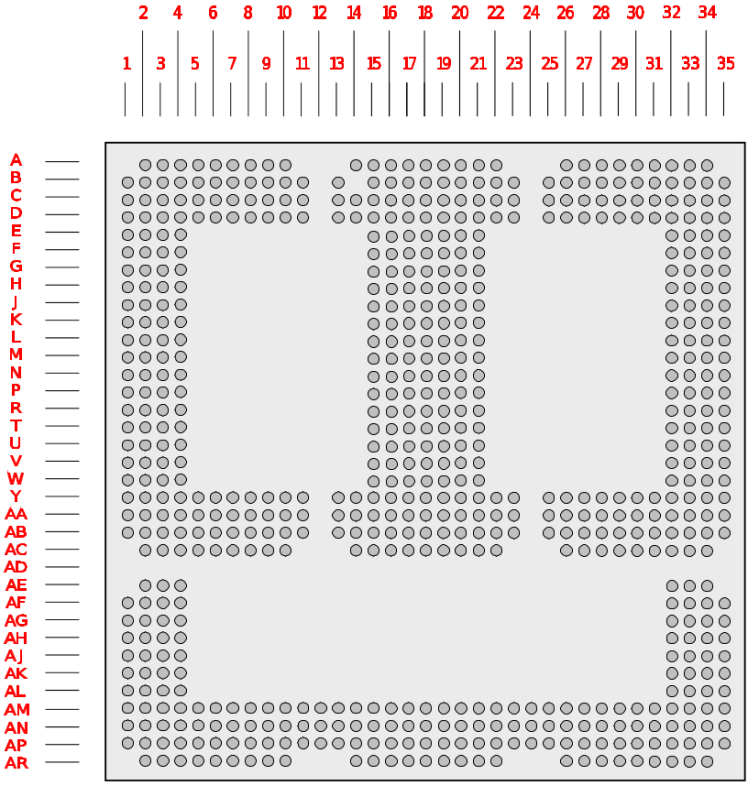
MPU Pin	Function	OSM Pads	Notes
D9	SYS_RST#	U17	Pullup 10k0
C6	CARRIER_PWR_EN	V17	Pullup 1k
AE16	MD_BOOT0	U19	Pullup 1k
AC14	MD_BOOT1	R18	Pullup 47k0
	PWR_BTN#	AA9	Connected to (PMIC)Pin J7 Pullup 10k0

4.3.13 MSZG3E SiP Pads

4.3.13.1 Contact Groups



4.3.13.2 Contact Grid Numbering



4.3.13.3 Contact Table

ETHERNET

Mpu Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
U7	ETH_A_TX_CTL	K16	L16	–	–
U3	ETH_A_TX_CLK	J15	E16	–	–
U6	ETH_A_TXD0	H15	F15	–	–
P2	ETH_A_TXD1	G15	N16	–	–
R2	ETH_A_TXD2	H16	K2	–	–
P1	ETH_A_TXD3	G16	D2	–	–
V2	ETH_A_RX_CTL	M15	E1	–	–
R1	ETH_A_RX_CLK	R15	M2	–	–
R3	ETH_A_RXD0	K15	N35	–	–
R6	ETH_A_RXD1	L15	Y35	–	–
R7	ETH_A_RXD2	N15	AA35	–	–
U8	ETH_A_RXD3	P15	Y34	–	–
U9	ETH_A_MDIO	T15	AA34	–	–
U2	ETH_A_MDC	T16	V34	–	–
N6	ETH_B_TX_CTL	J2	W35	–	–
K2	ETH_B_TX_CLK	H1	V35	–	–
L3	ETH_B_TXD0	G1	U35	–	–
H2	ETH_B_TXD1	F1	R35	–	–
J1	ETH_B_TXD2	G2	P35	–	–
H1	ETH_B_TXD3	F2	U34	–	–
N1	ETH_B_RX_CTL	L1	T35	–	–
K1	ETH_B_RX_CLK	P1	AC34	–	–
L6	ETH_B_RXD0	J1	AB35	–	–
L7	ETH_B_RXD1	K1	R34	–	–
J2	ETH_B_RXD2	M1	N33	–	–
G1	ETH_B_RXD3	N1	P33	–	–
M2	ETH_B_MDIO	C7	–	–	–
M1	ETH_B_MDC	C6	–	–	–

JTAG

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
AC12	JTAG_TCK	N17	AE12	JTAG_TRST#	R19
AD12	JTAG_TMS	N19	AD18	JTAG_DBGEN	AC18
W12	JTAG_TDI	P17	–	–	P19
AB12	JTAG_TDO	R17	–	–	CA18

CAN/USB

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
AD2	CAN_A_TX	AC17	AH13	USB_C_SSRX_N	B11
AE1	CAN_A_RX	AB17	AJ12	USB_C_SSRX_P	B10
W4	CAN_B_TX	AC19			AC20
W1	CAN_B_RX	AB19			AB22
AJ17	USB_OTG_D_P	AC14			C10
AH17	USB_OTG_D_N	AB13			D9
AJ4	USB_OTG_VBUS_EN	AC16			C8
AE24	USB_OTG_ID	AB14			C9
AC15	USB_OTG_OC#	AC15			D25
AJ4	USB_OTG_VBUS	AB16			D26
AJ16	USB_HOST_D_P	AC22			C26
AH16	USB_HOST_D_N	AB23			D27
C2	USB_HOST_VBUS_EN	AC20			C28
B1	USB_HOST_OC#	AC21			C27
AJ15	USB_C_D_P	D10			A28
AH15	USB_C_D_N	D11			A27
AH14	USB_C_SSTX_N	A9			B26
AJ14	USB_C_SSTX_P	A8			B25

SDIO

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
E1	SDIO_CLK	F21	–	–	T21
C1	SDIO_CMD	E20	–	–	U20
H8	SDIO_CD#	J21	–	–	L20
E8	SDIO_WP	D20	–	–	L21
G2	SDIO_DATA0	G20	–	–	M21
J6	SDIO_DATA1	G21	–	–	N20
F1	SDIO_DATA2	H20	–	–	N21
F2	SDIO_DATA3	H21	–	–	P20
A7	SDIO_GP_PWREN	D21	–	–	P21
AG1	SDIO_PWREN	C20	–	–	R21
–	–	K20	–	–	U21
–	–	K21	–	–	T20

ADC/PWM/GPIO

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
AH8	ADC_0	M18	G4	GPIO_C7/CAM_RST#	J18
AJ8	ADC_1	N18			K18
AC5	DISP_BL_PWM	E18			H19
Y1	GPIO_A_0	D17			J19
W10	GPIO_A_1	E17			K19
W5	GPIO_A_2	F17			L19
W2	GPIO_A_3	G17			D3
W3	GPIO_A_4	H17			D4
W6	GPIO_A_5	J17			E3
N8	GPIO_A_6	K17			E4
G3	GPIO_A_7	L17			U32
V1	GPIO_B_0	D19			U33
T2	GPIO_B_1	E19			V32
U1	GPIO_B_2	F19			V33
T1	GPIO_B_3	G19			W32
F3	GPIO_C4/DISP_VDD_EN	F18			W33
F4	GPIO_C5/DISP_BL_EN	G18			Y32
G3	GPIO_C6/CAM_PWR	H18			Y33

UART

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
AH2	SCIF_RXD	D22	AJ2	UART_B_TX	D13
AH1	SCIF_TXD	D23	–	–	D15
Y2	UART_A_RX	A14	–	–	D16
W9	UART_A_TX	B13	–	–	A22
W8	UART_A_RTS	C13	–	–	A23
W7	UART_A_CTS	C14	–	–	C22
AJ3	UART_B_RX	D14	–	–	C23

I2C

MPU Pin	Function	OSM Pads	MPU Pin	Function	OSM Pads
AH5	I2C_A_CLK	AA15	–	–	V18
AG10	I2C_A_DAT	AA16	–	–	W18
AH3	I2C_PM_CLK	AA20	–	–	W20
AF10	I2C_PM_DAT	AA21	–	–	Y22
AA3	SPI_A_SDI	U15	–	–	Y23
AB2	SPI_A_SDO	V15	–	–	AA23
AA2	SPI_A_CS0#	Y15	–	–	Y21
AA1	SPI_A_SCK	U16	–	–	C29
–	–	V21	–	–	D30
–	–	W21	–	–	C30
–	–	V19	–	–	D29
–	–	W19			

PCIe

MPU Pin	Function	OSM Pad	Notes
AJ24	PCIE_A_RX_P	AB1	–
AH24	PCIE_A_RX_N	AB2	–
AJ23	PCIE_A_TX_P	AC2	–
AH23	PCIE_A_TX_N	AC3	–
A2	PCIE_PERST#	V2	–
E10	PCIE_CLKREQ#	W2	–
–	PCIE_REFCLK_OUT_P	W1	Connected to Clock(24)
–	PCIE_REFCLK_OUT_N	Y1	Connected to Clock(23)
AB10	PCIE_WAKE#	T2	–
AJ20	PCIE_B_RX_P	L34	–
AH21	PCIE_B_RX_N	M34	–
AJ19	PCIE_B_TX_P	K35	–
AH19	PCIE_B_TX_N	L35	–

VENDOR DEFINED

MPU Pin	Function	OSM Pad	Notes
AE14	BOOTCPUSEL	D7	Boot mode selection: 0 = CM33, 1 = CA55 (only CA55 supported).
AB14	MD_BOOT2	Y29	–
–	SD0_DEV_SEL	Y30	Toggles EMMc/SDIO

RGB

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
K18	LCD_R2	Y7	G18	LCD_B3	R3
F16	LCD_R3	AA6	J18	LCD_B4	P3
H16	LCD_R4	Y6	A13	LCD_B5	N3
J14	LCD_R5	AA5	H14	LCD_B6	N4
F14	LCD_R6	Y5	F12	LCD_B7	M3
E12	LCD_R7	Y4	A12	LCD_CLK	M4
F18	LCD_G2	W4	B13	LCD_VSYNC	L3
G16	LCD_G3	V3	K12	LCD_HSYNC	K3
G14	LCD_G4	V4	B7	LCD_DISP	K4
B14	LCD_G5	U3	L12	LCD_DE	J4
A14	LCD_G6	T3	B9	LCD_RESET#	J3
B12	LCD_G7	T4	–	–	H3
E16	LCD_B2	R4			

DSI

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
B24	DSI_DATA0_N	AB11	E24	DSI_DATA3_N	AB5
A24	DSI_DATA0_P	AB10	F24	DSI_DATA3_P	AB4
B25	DSI_DATA1_N	AC9	B26	DSI_DCLK_N	AB8
A25	DSI_DATA1_P	AC8	A26	DSI_DCLK_P	AB7
B27	DSI_DATA2_N	AC6	–	–	AA3
A27	DSI_DATA2_P	AC5			

CSI

MPU Pin	Function	OSM Pad	MPU Pin	Function	OSM Pad
B24	DSI_DATA0_N	AB11	E24	DSI_DATA3_N	AB5
A24	DSI_DATA0_P	AB10	F24	DSI_DATA3_P	AB4
B25	DSI_DATA1_N	AC9	B26	DSI_DCLK_N	AB8
A25	DSI_DATA1_P	AC8	A26	DSI_DCLK_P	AB7
B27	DSI_DATA2_N	AC6	–	–	AA3
A27	DSI_DATA2_P	AC5			

POWER

MPU Pin	Function	OSM Pads	Notes
	SYS_RST#	U17	Pullup 10k0
	CAR-RIER_PWR_EN	V17	Pulldown 47k0
AE16	MD_BOOT0	U19	Pullup 1k0
AC16	MD_BOOT1	R18	Pullup 1k0
	PWR_BTN#	AA9	Pull up 10k0(to be done)
		Y17	
		Y19	
		W17	
		U18	
		AA18	
		AB18	
		T17	
		M19	
		Y16	
		Y20	
		Y3	
		C5	
		AA33	
		B29	

4.4 Conversion of MSRZG3E interfaces to OSMEVK baseboard

MPU PIN	OSM Pad	MSRZG3E Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
ETHERNET				
U3	J15	ETH_A_TX_CLK	ETH_A_TXCLK	P1-39
U6	H15	ETH_A_TXD0	ETH_A_TXD0	P1-47
P2	G15	ETH_A_TXD1	ETH_A_TXD1	P1-45
R2	H16	ETH_A_TXD2	ETH_A_TXD2	P1-43
P1	G16	ETH_A_TXD3	ETH_A_TXD3	P1-41
U7	K16	ETH_A_TX_CTL	ETH_A_TXCTL	P1-37
R1	R15	ETH_A_RX_CLK	ETH_A_RXCLK	P1-21
R3	K15	ETH_A_RXD0	ETH_A_RXD0	P1-25
R6	L15	ETH_A_RXD1	ETH_A_RXD1	P1-27
RU	N15	ETH_A_RXD2	ETH_A_RXD2	P1-29
U8	P15	ETH_A_RXD3	ETH_A_RXD3	P1-31
V2	M15	ETH_A_RX_CTL	ETH_A_RXCTL	P1-23
U2	T16	ETH_A_MDC	ETH_A_MDC	P1-11
U9	T15	ETH_A_MDIO	ETH_A_MDIO	P1-9
JTAG				
AC12	N17	JTAG_TCK	JTAG_TCK	P2-18
AD12	N19	JTAG_TMS	JTAG_TMS	P2-16
W12	P17	JTAG_TDI	JTAG_TDI	P2-14
AB12	R17	JTAG_TDO	JTAG_TDO	P2-12
AE12	R19	JTAG_TRST#	JTAG_TRST#	P2-10
CAN				
AE1	AB17	CAN_A_RX	CAN_A_RX	P4-2
AD2	AC17	CAN_A_TX	CAN_A_TX	P41
USB				
AJ17	AC14	USB_OTG_D_P	USB_OTG_D_P	P4-20
AH17	AB13	USB_OTG_D_N	USB_OTG_D_N	P4-22
AJ4	AC16	USB_OTG_VBUS_EN	USB_A_EN	P4-14
AE24	AB14	USB_OTG_ID	USB_OTG_ID	P4-16
AH4	AC15	USB_OTG_OC#	USB_OTG_OC#	P4-12
AJ16	AC22	USB_HOST_D_P	USB_HOST_D_P	P4-32
AH16	AB23	USB_HOST_D_N	USB_HOST_D_N	P4-34
C2	AC20	USB_HOST_VBUS_EN	USB_B_EN	P4-26
B1	AC21	USB_HOST_OC#	USB_HOST_OC#	P4-12
AH2	D22	SCIF_RXD	CONS_RX	P2-48
AH1	D23	SCIF_TXD	CONS_TX	P2-46
Y2	A14	UART_A_RX	UART_A_RX	P2-40
W9	B13	UART_A_TX	UART_A_TX	P2-38
RGB/LCD				
K18	Y7	LCD-R2	P3-50	LCD-R2
F16	AA6	LCD-R3	P3-48	LCD-R3
H16	Y6	LCD-B4	P3-46	LCD-B4
J14	AA5	LCD-R5	P3-44	LCD-R5
F14	Y5	LCD-R6	P3-42	LCD-R6
E12	Y4	LCD-R7	P3-40	LCD-R7
F18	W4	LCD-G2	P3-36	LCD-G2

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Table 2 – continued from previous page

MPU PIN	OSM Pad	MSRZG3E Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
G16	V3	LCD-G3	P3-34	LCD-G3
G14	V4	LCD-G4	P3-32	LCD-G4
B14	U3	LCD-G5	P3-30	LCD-G5
H14	T3	LCD-G6	P3-28	LCD-G6
F12	T4	LCD-G7	P3-26	LCD-G7
E16	R4	LCD-B2	P3-22	LCD-B2
F16	R3	LCD-B3	P3-20	LCD-B3
J18	P3	LCD-B4	P3-18	LCD-B4
A13	N3	LCD-B5	P3-16	LCD-B5
H14	N4	LCD-B6	P3-14	LCD-B6
F12	M3	LCD-B7	P3-12	LCD-B7
A12	M4	LCD_CLK	P3-8	LCD_CLK
B13	L3	LCD_VSYNC	P3-6	LCD_VSYNC
K12	K3	LCD_HSYNC	P3-4	LCD_HSYNC
L12	J4	LCD_DE	P3-2	LCD_DE
DSI				
B24	AB11	DSI_DATA0_N	DSI_DATA0_N	P3_49
A24	AB10	DSI_DATA0_P	DSI_DATA0_P	P3-47
B25	AC9	DSI_DATA1_N	DSI_DATA1_N	P3-43
A25	AC8	DSI_DATA1_P	DSI_DATA1_P	P3-41
B26	AB8	DSI_DCLCK_N	DSI_CLK_N	P3-37
A26	AB7	DSI_DCLCK_P	DSI_CLK_P	P3-35
	AA3	DSI_TE	DSI.TE	P3-31
CSI				
AH25	C1	CSIO_DAT0_N	CSI_DAT0_N	P1-18
AJ26	B1	CSIO_DAT0_P	CSI_DAT0_P	P1-16
AH27	A2	CSIO_DAT1_N	CSI_DAT1_N	P1-12
AJ27	A3	CSIO_DAT1_P	CSI_DAT1_P	P1-10
AH28	B3	CSIO_CLK_N	CSI_CLK_N	P1-6
AJ28	B4	CSIO_CLK_P	CSI_CLK_P	P1-4
SDIO				
E1	F21	SD0_CLK	SDIO_CLK	P2-27
C1	E20	SD0_CMD	SDIO_CMD	P2-25
H8	J21	SD0_CD#	SDIO_CD#	P2-37
E8	D20	SD0_WP	SDIO_WP	GND
G2	G20	SD0_DATA0	SDIO_DAT0	P2-29
J6	G21	SD0_DATA1	SDIO_DAT1	P2-31
F1	H20	SD0_DATA2	SDIO_DAT2	P2-33
F2	H21	SD0_DATA3	SDIO_DAT3	P2-35
AG1	D21	SD0_PWR_EN	SDIO_PWR_EN	P-23
GPIO				
Y1	D17	GPIO_A_0	GPIO_A0	P2-5
W10	E17	GPIO_A_1	GPIO_A1	P2-7
W5	F17	GPIO_A_2	GPIO_A2	P2-9
W2	G17	GPIO_A_3	GPIO_A3	P2-11
W3	H17	GPIO_A_4	GPIO_A4	P2-13
W6	J17	GPIO_A_5	GPIO_A5	P2-15
N8	K17	GPIO_A_6	GPIO_A6	P2-17

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Table 2 – continued from previous page

MPU PIN	OSM Pad	MSRZG3E Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
G3	L17	GPIO_A_7	GPIO_A7	P2-19
ADC				
AH8	M18	ADC_0	ADC_0	P-43
AJ8	N18	ADC_1	ADC_1	P3-45
I2C				
AH5	AA15	I2C_A_CLK	I2C_A_SCL	P4-35
AG10	AA16	I2C_A_DAT	I2C_A_SDA	P4-37
AH3	AA20	I2C_PM_CLK	I2C_B_SCL	P4-38
AF10	AA21	I2C_PM_DAT	I2C_B_SCL	P4-40
SPI				
AA3	U15	SPI_A_SDI	SPI_A_SDI	P4-17
AB2	V15	SPI_A_SDO	SPI_A_SDO	P4-15
AA2	Y15	SDPI_A_CS0#	SDPI_A_CS0#	P4-13
AA1	U16	SPI_A_SCK	SPI_A_SCK	P4-11
VENDOR DEFINED				
–	Y30	SD0_DEV_SEL	SD0_DEV_SEL	GND
AE16	Y29	MD_BOOT2	BOOT_SEL2#	P4-50
POWER/SYSTEM				
–	U17	SYS_RST#	SYS_RST#	P4-29
–	V17	CARRIER_PWR_EN	CARRIER_PWR_EN	P4-31
AE16	U19	MD_BOOT0	BOOT_SEL0#	P4-46
AC14	R18	MD_BOOT1	BOOT_SEL1#	P4-48
–	AA9	PWR_BTN#	PWR_BTN#	P4-44

4.5 SCHEMATICS

Schematics for the MSRZG3E SiP may be obtained on request. Please contact sales@aries-embedded.de. Below the OSM schematics footprint is shown: