MSRZG2UL Hardware Manual

Version: **1.0**

Created on: May 19, 2022

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

Adress:

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	13.09.2022	dk	Initial creation
2.0	06.08.2024	fn	Improving typos
3.0	24.01.2025	fn	Adding the interface conversion via OSMEVK_ADAP_MSRZG2UL
4.0	07.03.2025	fn	Changing pictures of MSRZG2UL

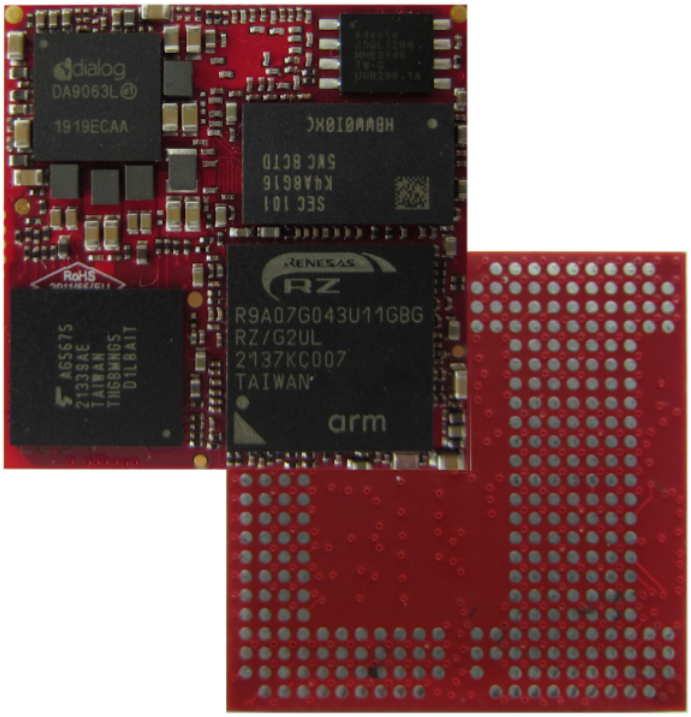
CHAPTER

TWO

OVERVIEW

2.1 MSRZG2UL Microprocessor SiP

The MSRZG2UL is the Open Standard Module compliant System-In-Package based on Renesas RZ Family architecture offering high-performance Cortex-A55/Cortex-M33 core. The MSRZG2UL combines compact design and a wide range of services, bringing low power consumption, thermal efficiency and low-cost to embedded systems.



2.2 Feature Set

- **RZ/G2UL general-purpose microprocessor unit**
  - Single Cortex-A55, up to 1GHz
  - Cortex-M33, up to 200MHz
- 512MB – 4GB DDR4 RAM
- 4GB eMMC NAND Flash
- dual 10/100/1000MBit Ethernet
- USB2.0 Host/OTG
- 2x CAN
- UART, I2C, SPI
- ADC
- display port
- camera interface
- compliant to the SGET OSM standard
- size S, 30x30mm^2,
- pin count: 332
- 0°C..+70°C commercial temperature range
- -40°C..+85°C industrial temperature range

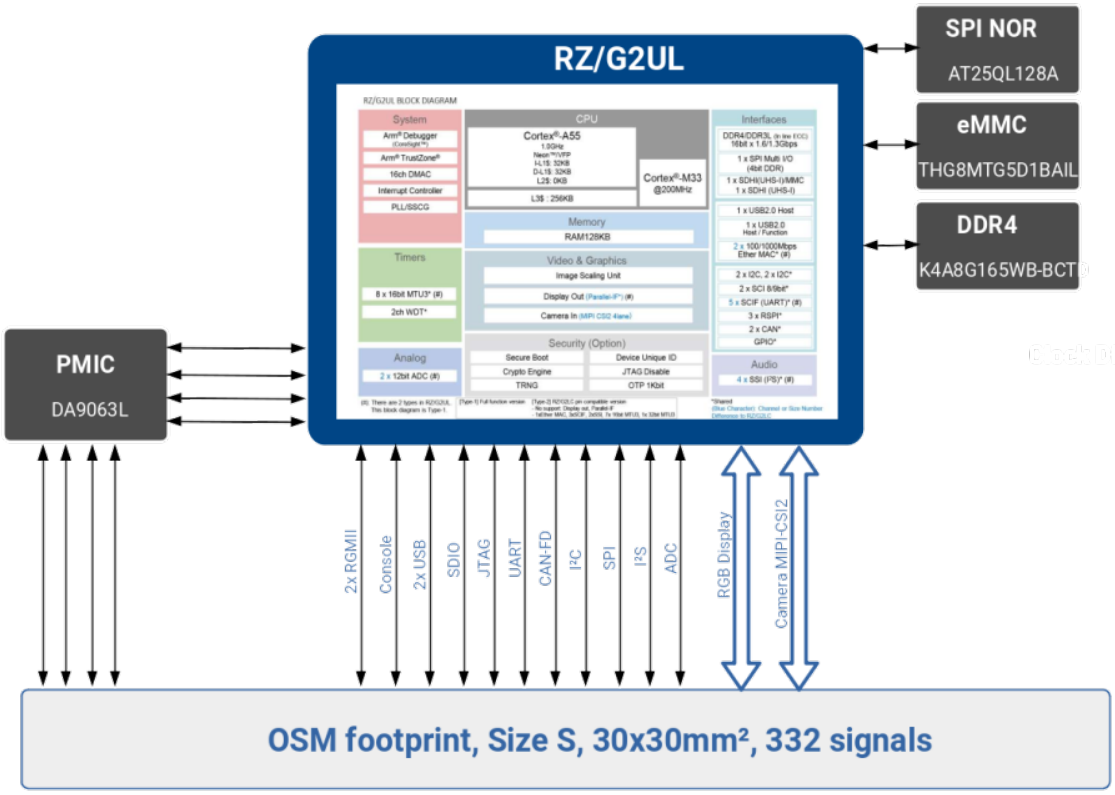
2.3 Order Codes

The MSRZG2UL SiP is available in the following standard configurations:

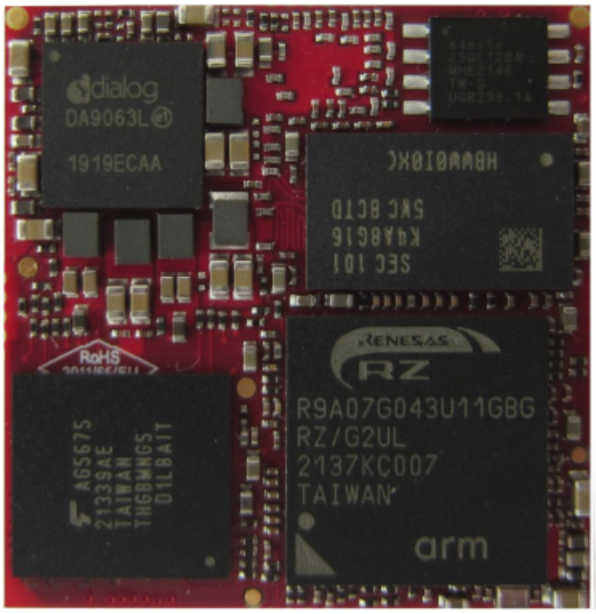
- **MSRZG2UL-A0A**
  - Renesas RZ/G2UL R9A07G043U11GBG
  - 512MB DDR4 RAM
  - no eMMC NAND Flash
  - 128MBit SPI-NOR
  - -25°...+85°C
- **MSRZG2UL-BAA**
  - Renesas RZ/G2UL R9A07G043U11GBG
  - 1GB DDR4 RAM
  - 4GB eMMC
  - 128MBit SPI-NOR
  - -25°...+85°C

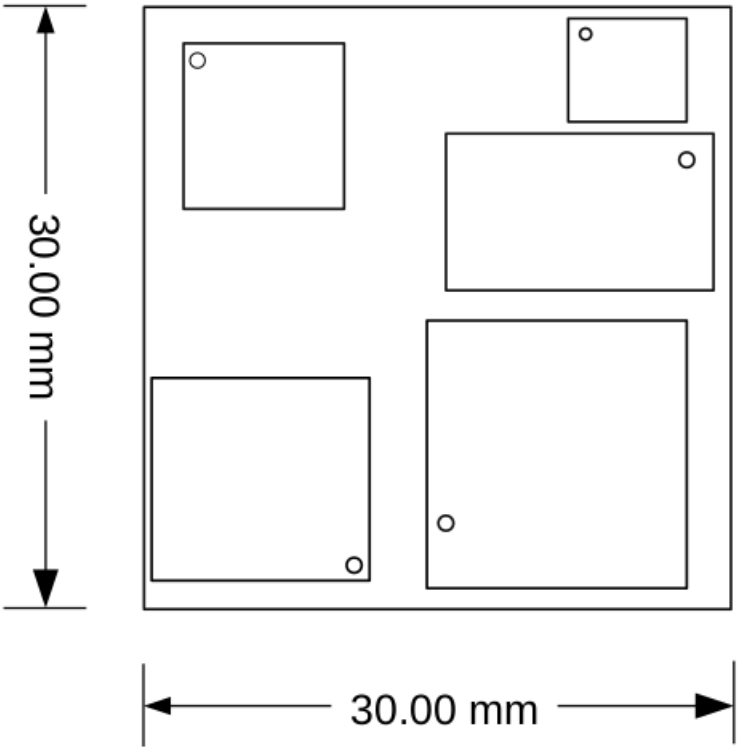
Please contact ARIES Embedded for more information about the availability of other standard products of MSRZG2UL or custom configurations.

2.4 Block Diagram



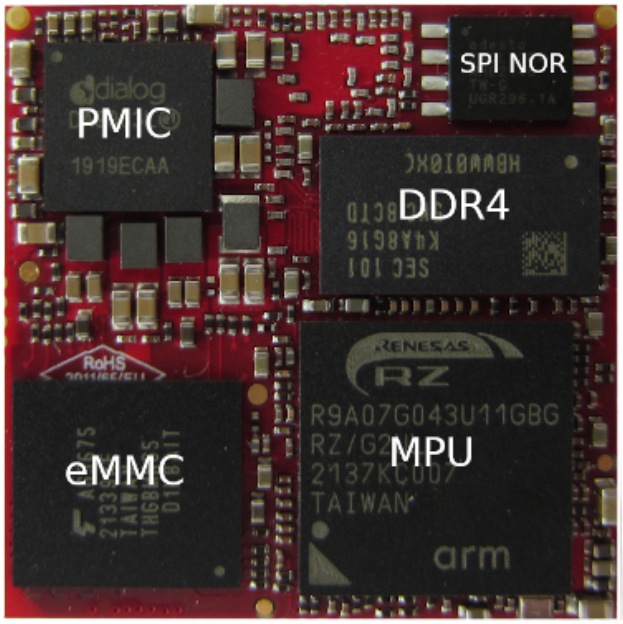
2.5 Dimensions



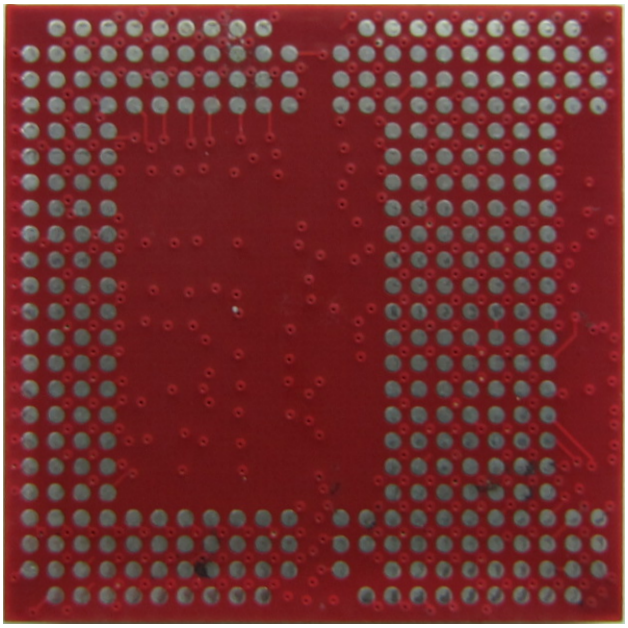


2.6 Part Overview

Assembly Top

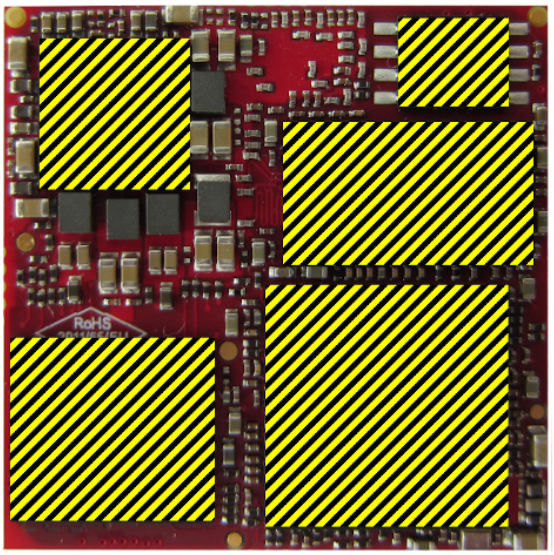


J1 Assembly Bottom



2.7 Handling Recommendations

To avoid mechanical damage to the components populated on MSRZG2UL it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

RESOURCES

3.1 Components

3.1.1 MPU

The R9A07G043U11GBG microprocessor is based on the high-performance Arm Cortex-A55 Single MPCore operating at up to 1.0 GHz and Arm Cortex-M33 Processor 200 MHz. The Cortex-A55 processor includes a 32-Kbyte L1 instruction cache for CPU, a 0-Kbyte level2 cache and 256-Kbyte L3 cache.

Features	R9A07G043U11GBG
Package	BGA Package (13x13mm)
CPU	Arm Cortex-A55 Single MPCore 1.0 GHz Arm Cortex-M33 Processor 200 MHz
On-chip RAM	128 Kbytes (ECC)
DDR4 Memory	512MB – 4GB

For more information about the R9A07G043U11GBG microprocessor please refer to the documentation which is available from Renesas.

3.1.2 DDR4 SDRAM

The MSRZG2UL is equipped with 1 block of Micron MT40A512M16LY-062E DDR4 SDRAM resulting in up to 8 GB of 16bit memory. Device is available in the commercial temperature range -40°C. . . +95°C. The memory interface is clocked at 1.6 GHz using the 1.2V/1.8V SDRAM standard interface.

3.1.2.1 MPU Signals for DDR4

MPU Pin	Function	DDR4 Pin		MPU Pin	Function	DDR4 Pin
G25	DDR_ADDR0	P3		U25	DDR_DQ0	G2
D25	DDR_ADDR1	P7		Y25	DDR_DQ1	F7
D23	DDR_ADDR2	R3		R25	DDR_DQ2	H3
K23	DDR_ADDR3	N7		T25	DDR_DQ3	H7
F23	DDR_ADDR4	N3		W24	DDR_DQ4	H2
E25	DDR_ADDR5	P8		T23	DDR_DQ5	H8
F25	DDR_ADDR6	P2		R24	DDR_DQ6	J3
C25	DDR_ADDR7	R8		T24	DDR_DQ7	J7
C24	DDR_ADDR8	R2		V25	DDR_DQSL_P	G3
B24	DDR_ADDR9	R7		V24	DDR_DQSL_N	F3
H25	DDR_ADDR10	M3		U23	DDR_DML	E7
B25	DDR_ADDR11	T2		AE24	DDR_DQ8	A3
H23	DDR_ADDR12	M7		AD24	DDR_DQ9	B8
A24	DDR_ADDR13	T8		AD25	DDR_DQ10	C3
K25	DDR_WE#	L2		AD23	DDR_DQ11	C7
L24	DDR_CAS#	M8		AA23	DDR_DQ12	C2
N23	DDR_RAS#	L8		AC24	DDR_DQ13	C8
E24	DDR_BA0	N2		W23	DDR_DQ14	D3
P23	DDR_BA1	N8		AA24	DDR_DQ15	D7
J25	DDR_BG0	M2		AB24	DDR_DQSU_P	B7
M24	DDR_ODT0	K3		AB25	DDR_DQSU_N	A7
P25	DDR_CLK_P	K7		Y24	DDR_DMU	E2
P24	DDR_CLK_N	K8		–	GND	F9
M25	DDR_CKE	K2		–	GND	E9
N24	DDR_CSO#	L7		–	–	T7
–	VCC_DDR4	P9		–	GND	M9
–	GND	T3		J24	DDR_ADDR14	L3
B23	DDR_RESET#	P1		–	GND	N9

3.1.3 eMMC Flash

The MSRZG2UL offers 4GB THGBMDG5D1LBAIL Toshiba eMMC Module housed in 153 ball BGA package.This unit is utilized advanced TOSHIBA NAND flash device(s) and controller chip assembled as Multi Chip Module. The eMMC provides a high-speed memory card interface compliant with JEDEC Version 5.0, eliminating the need for users to be concerned about directly controlling Flash Memories.

Function	eMMC Pin
EMMC_D0	A3
EMMC_D1	A4
EMMC_D2	A5
EMMC_D3	B2
EMMC_D4	B3
EMMC_D5	B4
EMMC_D6	B5
EMMC_D7	B6
EMMC_CMD	M5
EMMC_CLK	M6
EMMC_RST	K5

3.1.4 QSPI NOR FLASH

The W25Q128JWSIQ (128M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. The device operates on a single W25Q128JW power supply with current consumption as low as 1 mA active and 1 microA for power down.

Function	QSPI Pin
QSPI_IO0	C7
QSPI_IO1	A5
QSPI_IO2	B7
QSPI_IO3	C6
QSPI_SPCLK	B6
QSPI_SSL	B5

3.1.5 PMIC

Power on the MSRZG2UL is controlled by a DA9063L-00 Dialog Semiconductor fully integrated power management IC designed for productsbased on high integrated application processor designs requiring low power and highefficiency. The DA9063L follows a scalable approach of output currents and rails to supply the entire system and is capable of delivering a total of up to 12 A from its six DC-DC buck converters.

MPU Pin	Function	PMIC Pin	SiP Pads
–	PWR_BTN#	J7	AA9
–	PMIC_TP	D5	D6
–	PMIC_SDA	A7	P16
–	PMIC_SCL	A8	C16
W2	PRST#	D9	–
AA2	PMIC_IRQ#	B7	AA9
–	CAR-RIER_PWR_EN	D3	V17

3.2 I2C

MPU Pin	Function	SiP Pads
A19	I2C_B_SCL	AA20
A20	I2C_B_SDA	AA21
B19	I2C_A_SCL	AA15
B20	I2C_A_SDA	AA16

3.3 JTAG

MPU Pin	Function	SiP Pads
U2	JTAG_TCK/SWDCLK	N17
U1	JTAG_TMS/SWDIO	N19
W1	JTAG_TDI	P17
V2	JTAG_TDO	R17
V1	JTAG_TRST#	R19

3.4 UART

MPU Pin	Function	SiP Pads
AC1	UART_CONS_RX	D22
AC2	UART_CONS_TX	D23
B22	UART_A_RX	A14
A21	UART_A_TX	B13

3.5 Pin Out

3.5.1 Ethernet

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
M2	ET0_TXC	J15		AE18	ET1_TXC	H1
M1	ET0_TX_CTL	K16		AD17	ET1_TX_CTL	J2
K6	ET0_TX_ERR	K19		AE17	ET1_TX_ERR	K17
M6	ET0_CRS	E16		AC16	ET1_COL	E1
M3	ET0_COL	F15		AC15	ET1_CRS	D2
L1	ET0_TXD0	H15		AD16	ET1_TXD0	G1
L2	ET0_TXD1	G15		AE16	ET1_TXD1	F1
K1	ET0_TXD2	H16		AD15	ET1_TXD2	G2
K2	ET0_TXD3	G16		AE15	ET1_TXD3	F2
N3	ET0_RXC	R15		AC17	ET1_RXC	P1
N1	ET0_RX_CTL	M15		AC18	ET1_RX_CTL	L1
N2	ET0_RX_ERR	L16		AD18	ET1_RX_ERR	K2
P2	ET0_RXD0	K15		AE19	ET1_RXD0	J1
R3	ET0_RXD1	L15		AD19	ET1_RXD1	K1
R2	ET0_RXD2	N15		AE20	ET1_RXD2	M1
R1	ET0_RXD3	P15		AD20	ET1_RXD3	N1
T3	ET0_MDC	T16		AC20	ET1_MDC	C6
T2	ET0_MDIO	T15		AE21	ET1_MDIO	C7
P1	ET0_LINKSTA	D19		AC19	ET1_LINKSTA	E19

3.5.2 Display Interface

MPU Pin	Function	SiP Pads
B9	DISP_HSYNC	K3
C9	DISP_DE	J4
B10	DISP0	D17
A10	DISP_CLK	M4
C10	DISP_VSYNC	L3
C11	DISP5	AA5
B11	DISP2	Y7
A11	DISP1	E17
C12	DISP6	Y5
B12	DISP4	Y6
A12	DISP3	AA6
C13	DISP7	Y4
B13	DISP9	G17
A13	DISP8	F17
C14	DISP11	V3
C15	DISP13	U3
B15	DISP16	H17
A15	DISP14	T3
A14	DISP10	W4
B14	DISP12	V4
C16	DISP17	J17
B16	DISP19	R3
A16	DISP18	R4
C17	DISP22	N4
F16	DISP15	T4
A17	DISP20	P3
B17	DISP21	N3
C20	DISP23	M3

3.5.3 Camera Interface

MPU Pin	Function	SiP Pads
AD11	CSI_CLK_P	B4
AE11	CSI_CLK_N	B3
AD12	CSI_DATA0_P	B1
AE12	CSI_DATA0_N	C1
AD10	CSI_DATA1_P	A3
AE10	CSI_DATA1_N	A2
AD13	CSI_DATA2_P	A6
AE13	CSI_DATA2_N	A5
AD9	CSI_DATA3_P	B7
AE9	CSI_DATA3_N	B6

3.5.4 ADC

MPU Pin	Function	SiP Pads
B18	ADC0	M18
A18	ADC1	N18

3.5.5 SDIO

MPU Pin	Function	SiP Pads
H6	SDIO_A_CMD	E20
G2	SDIO_A_CLK	F21
H2	SDIO_A_D0	G20
J3	SDIO_A_D1	G21
J1	SDIO_A_D2	H20
J2	SDIO_A_D3	H21
D3	SDIO_A_CD#	J21
C3	SDIO_A_WP	D20

3.5.6 GPIO

MPU Pin	Function	SiP Pads
B1	GPIO_B_2	F19
C2	GPIO_B_3	G19
AC3	GPIO_A_7	L17
AB3	GPIO_B_5	J19
AB2	GPIO_B_4	H19

3.5.7 USB

MPU Pin	Function	SiP Pads
AD3	USB_A_EN	AC16
AE3	USB_A_OC#	AC15
AD2	USB_A_ID	AB14
AD1	USB_B_EN	AC20
AE2	USB_B_OC#	AC21
AD6	USB_A_D_P	AC14
AE6	USB_A_D_N	AB13
AD8	USB_A_VBUS_IN	AB16
AD5	USB_B_D_P	AC22
AE5	USB_B_D_N	AB23

3.5.8 MSRZG2UL SiP Pads

Connector J1

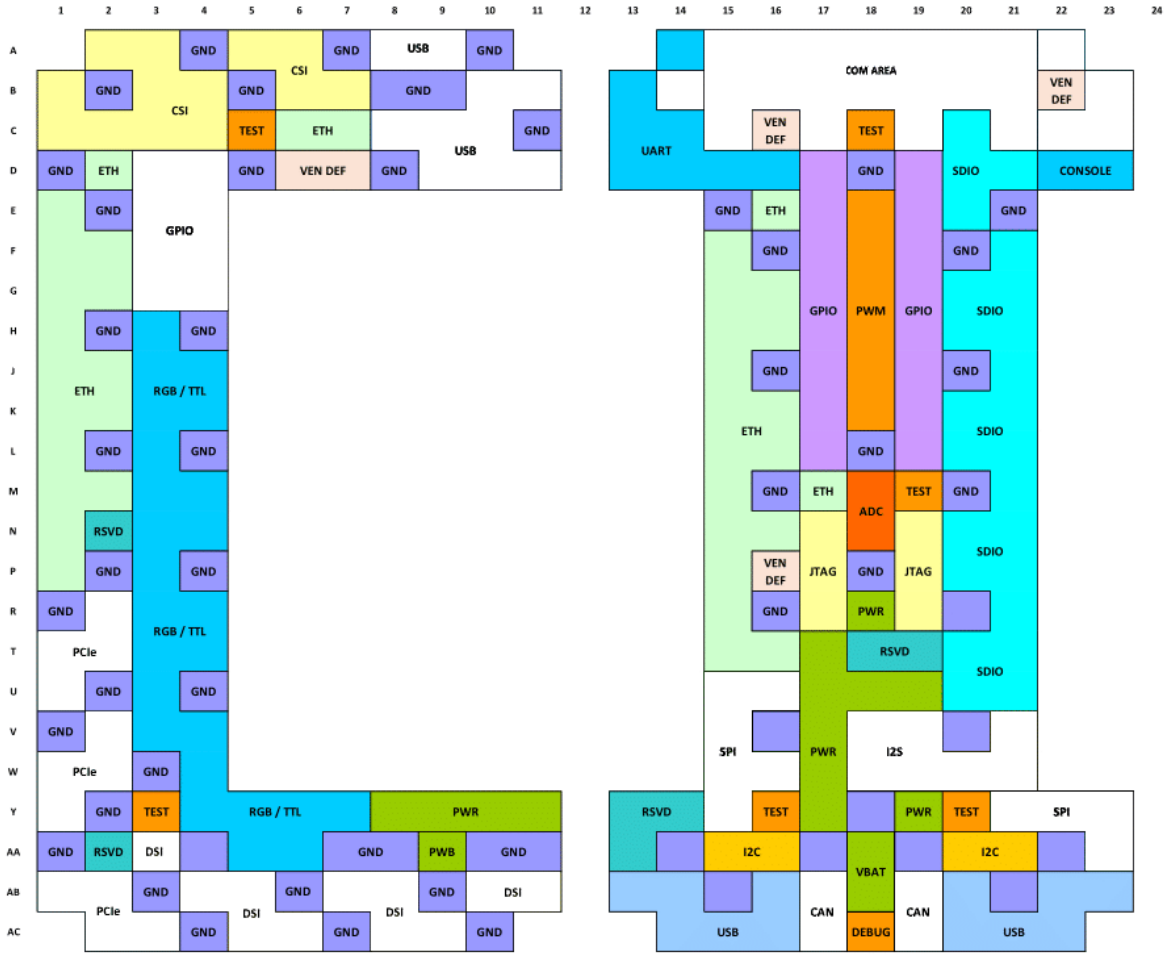


Fig. 1: Contact Overview

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
J1A						
–	–	M19		–	–	B22
–	–	Y16		–	PMIC_SCL	C16
–	–	Y20		–	PMIC_SDA	P16
–	3.3V	Y17		–	–	V21
–	3.3V	Y19		–	–	W21
–	–	AA18		–	–	V19
–	–	AB18		–	–	W19
–	OSM_SYS_RST#	U17		–	–	V18
–	CARRIER_PWR_EN	V17		–	–	W18
–	–	U18		–	–	W20

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Table 1 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	–	W17		AD6	USB_A_D_P	AC14
C5	MD_BOOT1	U19		AE6	USB_A_D_N	AB13
C4	MD_BOOT2	R18		AD2	USB_A_ID	AB14
–	–	T17		AE3	USB_A_OC#	AC15
–	–	U15		AD8	USB_A_VBUS_IN	AB16
–	–	V15		AD3	USB_A_EN	AC16
–	–	W16		AD5	USB_B_D_P	AC22
–	–	W15		AE5	USB_B_D_N	AB23
–	–	Y15		–	–	AB22
–	–	U16		AE2	USB_B_OC#	AC21
–	–	Y22		–	–	AB20
–	–	Y23		AD1	USB_B_EN	AC20
–	–	B19		B19	I2C_A_SCL	AA15
–	–	Y21		B20	I2C_A_SDA	AA16
H6	SDIO_A_CMD	E20		A19	I2C_B_SCL	AA20
G2	SDIO_A_CLK	F21		A20	I2C_B_SDA	AA21
H2	SDIO_A_D0	G20		–	–	AC17
J3	SDIO_A_D1	G21		–	–	AB17
J1	SDIO_A_D2	H20		–	–	AC19
J2	SDIO_A_D3	H21		–	–	AB19
D3	SDIO_A_CD#	J21		B18	ADC0	M18
C3	SDIO_A_WP	D20		A18	ADC1	N18
–	–	D21		–	–	E18
–	VCC_SD	C20		–	–	F18
–	–	K20		–	–	G18
–	–	K21		–	–	H18
–	–	L20		–	–	J18
–	–	L21		–	–	K18
–	–	M21		M3	ET0_CRS	E16
–	–	N20		M6	ET0_COL	F15
–	–	N21		L1	ET0_TXD0	H15
–	–	P20		L2	ET0_TXD1	G15
–	–	P21		K1	ET0_TXD2	H16
–	–	R21		K2	ET0_TXD3	G16
–	–	T21		M1	ET0_TX_CTL	K16
–	–	U20		M2	ET0_TXC	J15
–	–	U21		P2	ET0_RXD0	K15
–	–	T20		R3	ET0_RXD1	L15
AC1	UART_CONS_RX	D22		R2	ET0_RXD2	N15
AC2	UART_CONS_TX	D23		R1	ET0_RXD3	P15
–	–	C22		N2	ET0_RX_ERR	L16
–	–	C23		N1	ET0_RX_CTL	M15
–	–	A22		N3	ET0_RXC	R15
–	–	B23		–	–	N16
–	–	D14		T2	ET0_MDIO	T15
–	–	D13		T3	ET0_MDC	T16
–	–	D15		–	PVDD18	M17
–	–	D16		U2	JTAG_TCK/SWDCLK	N17
B22	UART_A_RX	A14		U1	JTAG_TMS/SWDIO	N19

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Table 1 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
A21	UART_A_TX	B13		W1	JTAG_TDI	P17
–	–	C13		–	–	P19
–	–	C14		V2	JTAG_TDO	R17
B10	DISP0	D17		V1	JTAG_TRST#	R19
A11	DISP1	E17		–	DEBUGEN	AC18
A13	DISP8	F17		–	–	C18
B13	DISP9	G17		–	GND	D18
B15	DISP16	H17		–	GND	E15
C16	DISP17	J17		–	GND	E21
AE17	ET1_TX_ERR	K17		–	GND	F16
AC3	GPIO_A_7	L17		–	GND	F20
P1	ET0_LINKSTA	D19		–	GND	J16
AC19	ET1_LINKSTA	E19		–	GND	J20
B1	GPIO_B_2	F19		–	GND	L18
C2	GPIO_B_3	G19		–	GND	M16
AB2	GPIO_B_4	H19		–	GND	M20
AB3	GPIO_B_5	J19		–	GND	P18
K6	ET0_TX_ERR	K19		–	GND	R16
–	–	L19		–	GND	R20
–	–	V16		–	GND	V20
–	GND	Y18		–	GND	AA14
–	GND	AA17		–	GND	AA19
–	GND	AA22		–	GND	AB15
–	GND	AB21		–	–	–
J1B						
–	–	A16		–	–	A20
–	–	C15		–	–	C17
–	–	C19		–	–	C21
–	–	A15		–	–	A17
–	–	A18		–	–	A19
–	–	A21		–	–	B15
–	–	B16		–	–	B17
–	–	B18		–	–	B19
–	–	B20		–	–	B21
J1C						
A3	5V	Y8		A2	PMIC_TP	D6
D6	5V	Y9		A9	AUDIO_CLK	D7
F5	5V	Y10		–	–	AB1
J6	5V	Y11		–	–	AB2
G5	PWR_BTN#	AA9		–	–	AC2
J5	–	Y3		–	–	AC3
W8	–	C5		–	–	W2
AC15	ET1_CRS	D2		–	–	V2
AC16	ET1_COL	E1		–	–	W1
AD16	ET1_TXD0	G1		–	–	Y1
AE16	ET1_TXD1	F1		–	–	T2
AD15	ET1_TXD2	G2		–	–	U1
AE15	ET1_TXD3	F2		–	–	T1
AD17	ET1_TX_CTL	J2		–	–	R2

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Table 1 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
AE18	ET1_TXC	H1		–	–	D3
AE19	ET1_RXD0	J1		–	–	D4
AD19	ET1_RXD1	K1		–	–	E3
AE20	ET1_RXD2	M1		–	–	E4
AD20	ET1_RXD3	N1		–	–	F3
AD18	ET1_RX_ERR	K2		–	–	F4
AC18	ET1_RX_CTL	L1		–	–	G3
AC17	ET1_RXC	P1		–	–	G4
–	–	M2		–	–	AB10
AE21	ET1_MDIO	C7		–	–	AB11
AC20	ET1_MDC	C6		–	–	AC8
AD12	CSI_DATA0_P	B1		–	–	AC9
AE12	CSI_DATA0_N	C1		–	–	AC5
AD10	CSI_DATA1_P	A3		–	–	AC6
AE10	CSI_DATA1_N	A2		–	–	AB4
AD13	CSI_DATA2_P	A6		–	–	AB5
AE13	CSI_DATA2_N	A5		–	–	AB7
AD9	CSI_DATA3_P	B7		–	–	AB8
AE9	CSI_DATA3_N	B6		–	–	AA3
AD11	CSI_CLK_P	B4		B11	DISP2	Y7
AE11	CSI_CLK_N	B3		A12	DISP3	AA6
–	–	C2		B12	DISP4	Y6
–	–	C3		C11	DISP5	AA5
–	–	C4		C12	DISP6	Y5
–	GND	A4		C13	DISP7	Y4
–	GND	A7		A14	DISP10	W4
–	GND	A10		C14	DISP11	V3
–	GND	B2		B14	DISP12	V4
–	GND	B5		C15	DISP13	U3
–	GND	B8		A15	DISP14	T3
–	GND	B9		F16	DISP15	T4
–	GND	C11		A16	DISP18	R4
–	GND	D1		B16	DISP19	R3
–	GND	D5		A17	DISP20	P3
–	GND	D8		B17	DISP21	N3
–	GND	E2		C17	DISP22	N4
–	GND	H2		C20	DISP23	M3
–	GND	H4		A10	DISP_CLK	M4
–	GND	L2		C10	DISP_VSYNC	L3
–	GND	L4		B9	DISP_HSYNC	K3
–	GND	P2		–	–	K4
–	GND	P4		C9	DISP_DE	J4
–	GND	R1		–	–	J3
–	GND	U2		–	–	H3
–	GND	U4		–	–	D10
–	GND	V1		–	–	D11
–	GND	W3		–	–	D9
–	GND	Y2		–	–	C8
–	GND	AA1		–	–	C10

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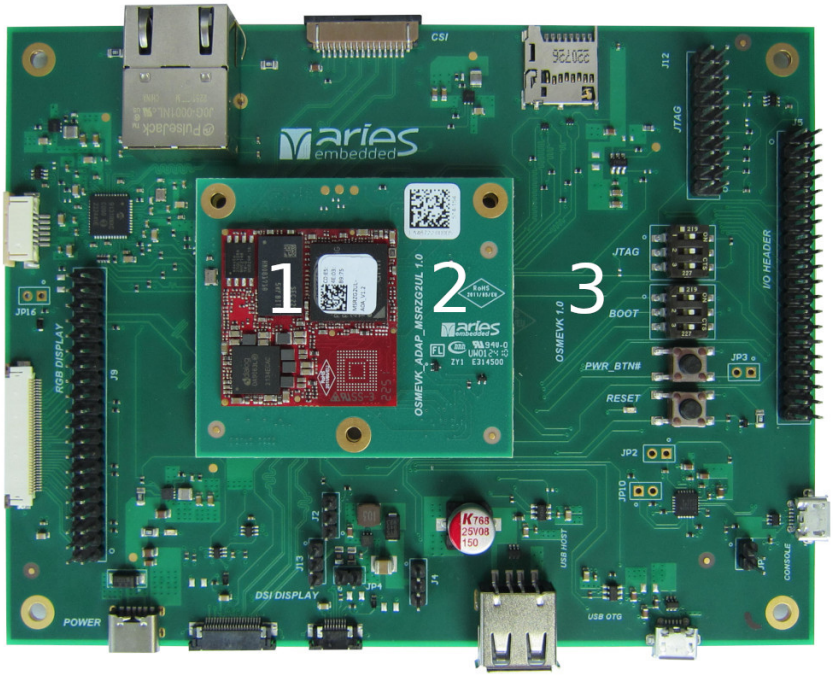
Table 1 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	GND	AA4		–	–	A9
–	GND	AA7		–	–	A8
–	GND	AA8		–	–	B11
–	GND	AA10		–	–	B10
–	GND	AA11		–	GND	AB3
–	GND	AB6		–	GND	AB9
–	GND	AC4		–	GND	AC7
–	GND	AC10		–	–	–

3.6 Conversion of MSRZG2UL interfaces to OSMEVK baseboard

The adapter board OSMEVK_ADAP_MSRZG2UL (**2**) enables the conversion of interfaces and/or voltage levels from the MSRZG2UL module (**1**) to the appropriate value and direction, ensuring compatibility with the SoM functionality on the OSMEVK baseboard (**3**).



CPU Pin	OSM Pin	MSRZG2UL Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
W2	U17	OSM_SYS_RST#	SYS_RST#	P4-29
C5	U19	MD_BOOT1	BOOT_SEL0#	P4-46
C4	R18	MD_BOOT2	BOOT_SEL1#	P4-48
H6	E20	SDIO_A_CMD	SDIO_CMD	P2-25
G2	F21	SDIO_A_CLK	SDIO_CLK	P2-27
H2	G20	SDIO_A_D0	SDIO_DAT0	P2-29
J3	G21	SDIO_A_D1	SDIO_DAT1	P2-31
J1	H20	SDIO_A_D2	SDIO_DAT2	P2-33

continues on next page

Table 2 – continued from previous page

CPU Pin	OSM Pin	MSRZG2UL Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
J2	H21	SDIO_A_D3	SDIO_DAT3	P2-35
D3	J21	SDIO_A_CD#	SDIO_CD#	P2-37
C3	D20	SDIO_A_WP	–	–
AC1	D22	UART_CONS_RX	CONS_RX	P2-48
AC2	D23	UART_CONS_TX	CONS_TX	P2-46
B22	A14	UART_A_RX	UART_A_RX	P2-40
A21	B13	UART_A_TX	UART_A_TX	P2-38
B10	D17	DISP0	GPIO_A0	P2-5
A11	E17	DISP1	GPIO_A1	P2-7
A13	F17	DISP8	GPIO_A2	P2-9
B13	G17	DISP9	GPIO_A3	P2-11
B15	H17	DISP16	GPIO_A4	P2-13
C16	J17	DISP17	GPIO_A5	P2-15
AE17	K17	ET1_TX_ERR	GPIO_A6	P2-17
AC3	L17	GPIO_A_7	GPIO_A7	P2-19
P1	D19	ET0_LINKSTA	–	–
AC19	E19	ET1_LINKSTA	–	–
B1	F19	GPIO_B_2	SDIO_PWR_EN	P2-23
C2	G19	GPIO_B_3	–	–
AB2	H19	GPIO_B_4	–	–
AB3	J19	GPIO_B_5	–	–
K6	K19	ET0_TX_ERR	–	–
AD6	AC14	USB_A_D_P	USB_OTG_D_P	P4-20
AE6	AB13	USB_A_D_N	USB_OTG_D_N	P4-22
AD2	AB14	USB_A_ID	USB_OTG_ID	P4-16
AE3	AC15	USB_A_OC#	USB_OTG_OC#	P4-12
AD8	AB16	USB_A_VBUS_IN	USB_OTG_CARR	P4-3/5/7
AD3	AC16	USB_A_EN	USB_OTG_EN	P4-14
AD5	AC22	USB_B_D_P	USB_HOST_D_P	P4-32
AE5	AB23	USB_B_D_N	USB_HOST_D_N	P4-34
AE2	AC21	USB_B_OC#	USB_HOST_OC#	P4-28
AD1	AC20	USB_B_EN	USB_HOST_EN	P4-26
B19	AA15	I2C_A_SCL	I2C_A_SCL	P4-35
B20	AA16	I2C_A_SDA	I2C_A_SDA	P4-37
A19	AA20	I2C_B_SCL	I2C_B_SCL	P4-38
A20	AA21	I2C_B_SDA	I2C_B_SDA	P4-40
B18	M18	ADC0	ADC_0	P2-43
A18	N18	ADC1	ADC_1	P2-45
M6	E16	ET0_CRS	–	–
M3	F15	ET0_COL	–	–
L1	H15	ET0_TXD0	ETH_A_TXD0	P1-47
L2	G15	ET0_TXD1	ETH_A_TXD1	P1-45
K1	H16	ET0_TXD2	ETH_A_TXD2	P1-43
K2	G16	ET0_TXD3	ETH_A_TXD3	P1-41
M1	K16	ET0_TX_CTL	ETH_A_TXCTL	P1-37
M2	J15	ET0_TXC	ETH_A_TXCLK	P1-39
P2	K15	ET0_RXD0	ETH_A_RXD0	P1-25

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Table 2 – continued from previous page

CPU Pin	OSM Pin	MSRZG2UL Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
R3	L15	ET0_RXD1	ETH_A_RXD1	P1-27
R2	N15	ET0_RXD2	ETH_A_RXD2	P1-29
R1	P15	ET0_RXD3	ETH_A_RXD3	P1-31
N2	L16	ET0_RX_ERR	–	–
N1	M15	ET0_RX_CTL	ETH_A_RXCTL	P1-23
N3	R15	ET0_RXC	ETH_A_RXCLK	P1-21
T2	T15	ET0_MDIO	ETH_A_MDIO	P1-9
T3	T16	ET0_MDC	ETH_A_MDC	P1-11
U2	N17	JTAG_TCK/SWDCLK	JTAG_TCK	P2-18
U1	N19	JTAG_TMS/SWDIO	JTAG_TMS	P2-16
W1	P17	JTAG_TDI	JTAG_TDI	P2-14
V2	R17	JTAG_TDO	JTAG_TDO	P2-12
V1	R19	JTAG_TRST#	JTAG_TRST#	P2-10
Y19	AC18	DEBUGEN	JTAG_DEBUGEN	P2-8
AC15	D2	ET1_CRS	–	–
AC16	E1	ET1_COL	–	–
AD16	G1	ET1_TXD0	–	–
AE16	F1	ET1_TXD1	–	–
AD15	G2	ET1_TXD2	–	–
AE15	F2	ET1_TXD3	–	–
AD17	J2	ET1_TX_CTL	–	–
AE18	H1	ET1_TXC	–	–
AE19	J1	ET1_RXD0	–	–
AD19	K1	ET1_RXD1	–	–
AE20	M1	ET1_RXD2	–	–
AD20	N1	ET1_RXD3	–	–
AD18	K2	ET1_RX_ERR	–	–
AC18	L1	ET1_RX_CTL	–	–
AE21	C7	ET1_MDIO	–	–
AC20	C6	ET1_MDC	–	–
AD12	B1	CSI_DATA0_P	CSI_DATA0_P	P1-16
AE12	C1	CSI_DATA0_N	CSI_DATA0_N	P1-18
AD10	A3	CSI_DATA1_P	CSI_DATA1_P	P1-10
AE10	A2	CSI_DATA1_N	CSI_DATA1_N	P1-12
AD13	A6	CSI_DATA2_P	GND	–
AE13	A5	CSI_DATA2_N	GND	–
AD9	B7	CSI_DATA3_P	GND	–
AE9	B6	CSI_DATA3_N	GND	–
AD11	B4	CSI_CLK_P	CSI_CLK_P	P1-4
AE11	B3	CSI_CLK_N	CSI_CLK_N	P1-6
A9	D7	AUDIO_CLK	AUDIO_CLK	–
B11	Y7	DISP2	RGB_R2	P3-50
A12	AA6	DISP3	RGB_R3	P3-48
B12	Y6	DISP4	RGB_R4	P3-46
C11	AA5	DISP5	RGB_R5	P3-44
C12	Y5	DISP6	RGB_R6	P3-42
C13	Y4	DISP7	RGB_R7	P3-40

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Table 2 – continued from previous page

CPU Pin	OSM Pin	MSRZG2UL Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
A14	W4	DISP10	RGB_G2	P3-36
C14	V3	DISP11	RGB_G3	P3-34
B14	V4	DISP12	RGB_G4	P3-32
C15	U3	DISP13	RGB_G5	P3-30
A15	T3	DISP14	RGB_G6	P3-28
F16	T4	DISP15	RGB_G7	P3-26
A16	R4	DISP18	RGB_B2	P3-22
B16	R3	DISP19	RGB_B3	P3-20
A17	P3	DISP20	RGB_B4	P3-18
B17	N3	DISP21	RGB_B5	P3-16
C17	N4	DISP22	RGB_B6	P3-14
C20	M3	DISP23	RGB_B7	P3-12
A10	M4	DISP_CLK	RGB_CLK	P3-8
C10	L3	DISP_VSYNC	RGB_VSYNC	P3-6
B9	K3	DISP_HSYNC	RGB_HSYNC	P3-4
C9	J4	DISP_DE	RGB_DE	P3-2

3.7 Schematics

Schematics for the MSRZG2UL SiP may be obtained on request.