MSIX93 Hardware Manual

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Created by: ARIES Embedded GmbH

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	09.02.2026	fw/aw	Initial creation

CHAPTER

TWO

OPEN STANDARD MODUL (OSM)

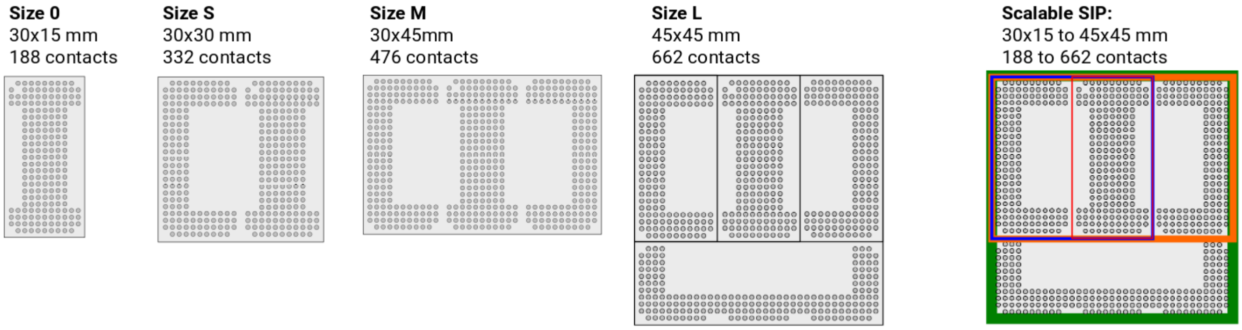
The idea of all Open Standard Modules™ is to create a new, future proof and versatile standard for small-size, low-cost embedded computer modules, combining the following key characteristics:

- Completely machine processible during soldering, assembly and testing
- Pre-tinned LGA package for direct PCB soldering without connector
- Pre-defined soft- and hardware interfaces
- Open-Source in soft- and hardware

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

2.1 Module Sizes and Dimensions

OSM SoMs are highly scalable in size, performance and functionality as they are available in different mechanical sizes and contact count:



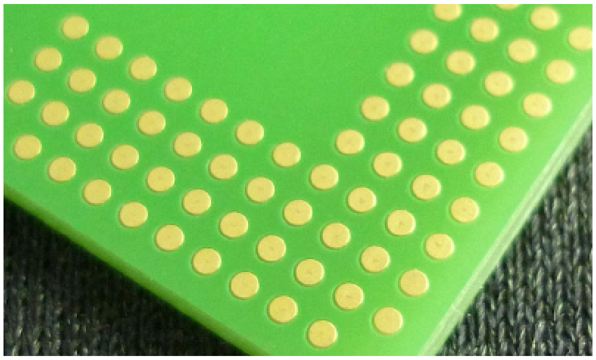
Size	**Metrics**	**Contact Count**	**Colour Outline**
Size-0 – “Zero”	30 mm x 15 mm	188 contacts	red
Size-S – “Small”	30 mm x 30 mm	332 contacts	blue
Size-M – “Medium”	30 mm x 45 mm	476 contacts	orange
Size-L – “Large”	45 mm x 45 mm	662 contacts	green

2.2 Contact Characteristics:

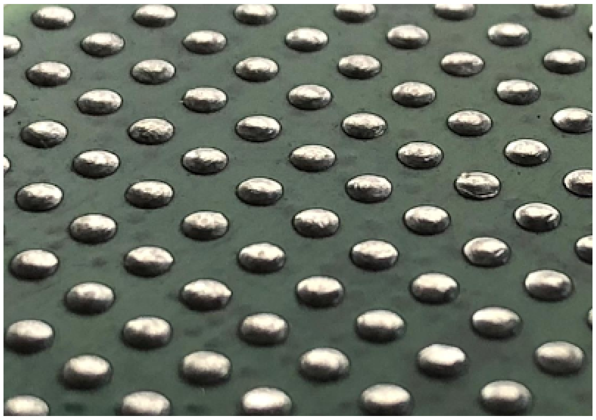
OSM SoMs are available with different contact characteristics:

2.2.1 ENIG-LGA

All OSM-SoMs by ARIES Embedded are using ENIG-LGA contacts on its PCBs:



2.2.2 Fused Tin Grid Array

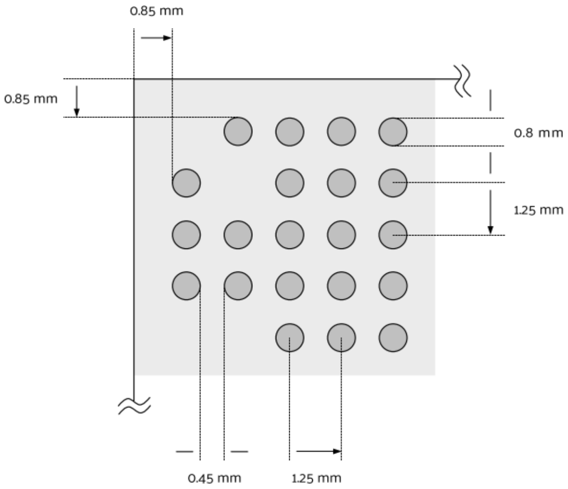


2.2.3 BGA

2.3 Contact Grid

The Contact Grid for the Open Standard Module™ Specification is symmetrically and defines the following dimensions:

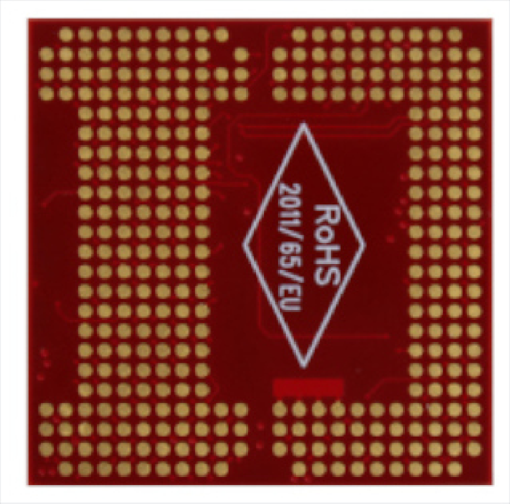
- Contact Diameter: 0.8 mm
- Contact Grid: 1.25 mm
- Contact-to-Contact: 0.45 mm
- Contact-to-Edge: 0.85 mm



2.4 Recommendations for Processing OSM System on Modules

In the following the MSIX93 will be used as a reference.

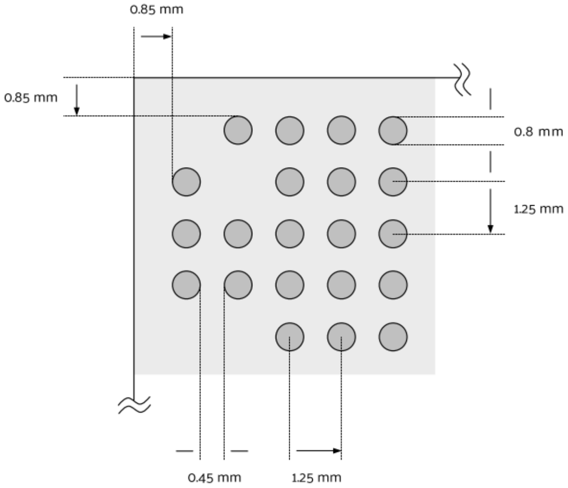
MSIX93 is available as a LGA332 package with round flat pads on the solder side of the SoM:



2.4.1 Design

2.4.1.1 Layout PCB

The connecting pad size of the baseboard layout should be similar to the layout of e.g. the MSRZG3E baseboard. The pad size is defined with 0.8mm, the pitch 1.25mm.



2.4.1.2 Stencil

The stencil should have a with of 120µm. The openings in the stencil should be round shape with a diameter of 0.8mm, accordingly.

2.4.2 Process Recommendation

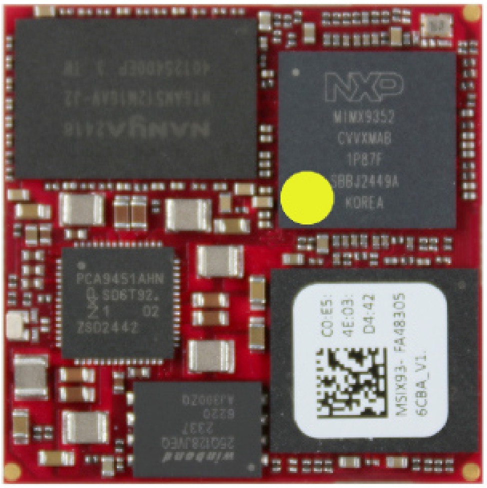
2.4.2.1 Storage

The OSM SoMs are to be handeled as moisture sensitive components. The SoMs shall be stored in suitable vacuum packages with dry packs.

The processing of the SoMs with opened package is limited to 168 hours at a maximum of 30°C and 60% air moisture. In case these values are exceeded and additional drying is necessary, the requirements of J-STD-033 have to be considered.

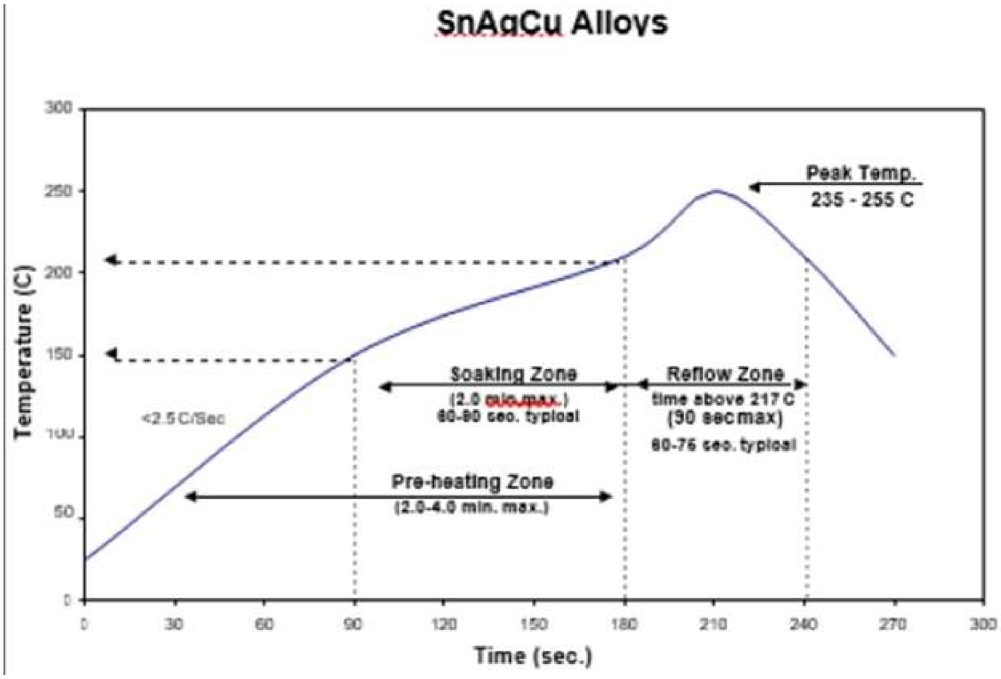
2.4.2.2 Production

For mounting the OSM SoMs the SoMs will be offered to the SMT machine in a tray or a reel. For the pickup of the SoM, using a vacuum nozzle, the SoM should be picked up by using a mechanical point as much as possible in the middle of the SoM, e.g. on the processor as outlined below (yellow marking).



2.4.2.3 Reflow Soldering

The SoM can be soldered in a reflow soldering process, using a standard RoHS profile. Below picture show the recommendation for the solder paste Kester NP545.



2.5 OSM Specification

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

The OSM specification is avaible for download (after registration) under https://sget.org/standards/osm/

2.6 OSM Design Guide

The primary purpose of OSM Design Guide is to serve as a suggestion for developers of OSM Carrier Boards and for OSM Module customers who wish to have a OSM based system developed. The document should also be valuable to FAEs and Product managers to help them understand the OSM Module infrastructure.

The OSM Design Guide is avaible for download (after registration) under https://sget.org/standards/osm/

CHAPTER

THREE

OVERVIEW

3.1 MSIX93 Microprocessor SiP

The MSIX93 is the Open Standard Module compliant System-In-Package based on NXP MSIX93 architecture offering high-performance single/dual CortexA55 cores in combination with a CortexM33 core. The MSXI93 combines compact design and a wide range of services, bringing low power consumption, thermal efficiency and low-cost to embedded systems.

MSIX93 fits to an OSM size S SoM in a size of only 30x30mm. Due to its 332 contacts the SoM offer the CPU almost transparently so that it can be used almost without functional restrictions due to the pin-multiplexing of the CPU.

3.2 Feature Set

- **i.MX93 CPU**
    - single/dual Cortex-A55, up to 1.7GHz
    - Cortex-M33, up to 250MHz
    - Arm Ethos-U65 micro NPU, optional
- 256MB – 2GB LPDDR4 RAM
- 4GB – 64GB eMMC NAND Flash
- 2MBit - 512MBit SPI NOR
- Dual 10/100/1000MBit Ethernet
- USB2.0 Host
- USB2.0 device
- 2x CANFD
- UART, I2C, SPI, ADC
- Hardware Compositor for Blending/Composition, Resize, Color Space Conversion
- LVDS display interface 720p
- MIPI-CSI camera interface 2 lanes
- compliant to the SGET OSM standard
- OSM sizeS, 30x30mm
- 332 contacts
- 0°C..+70°C commercial temperature range
- -40°C..+85°C industrial temperature range

3.3 Order Codes

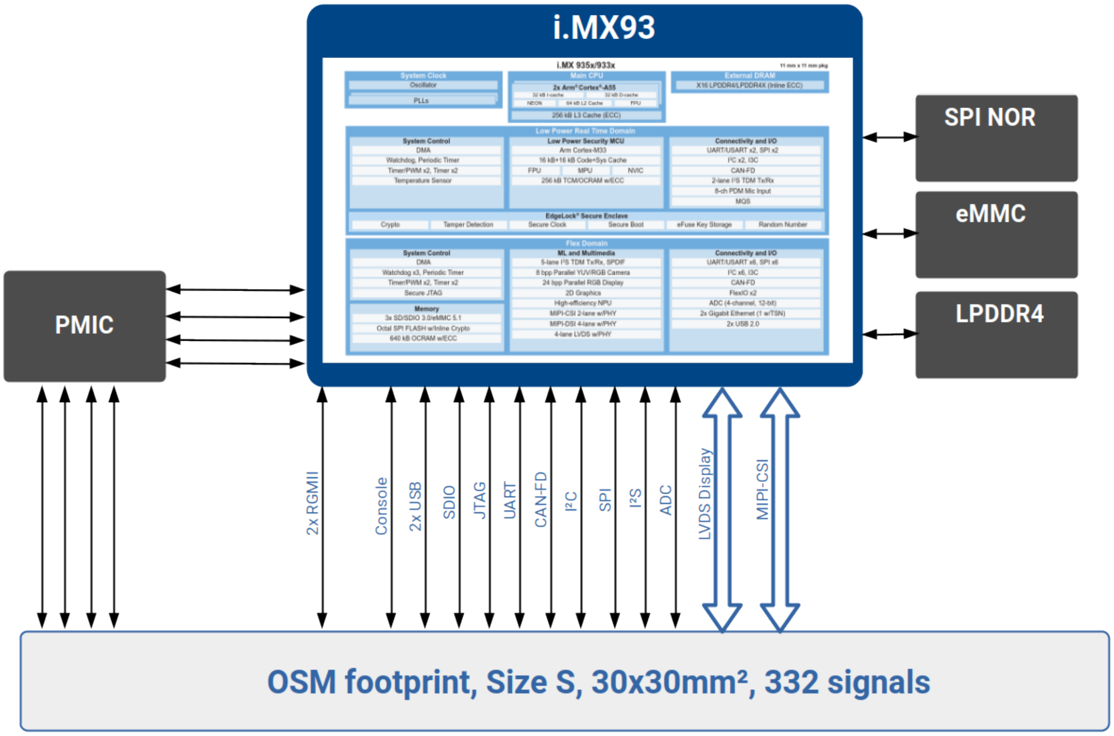
The MSIX93 SoM is available in the following standard configurations:

MSIX93-6CBA

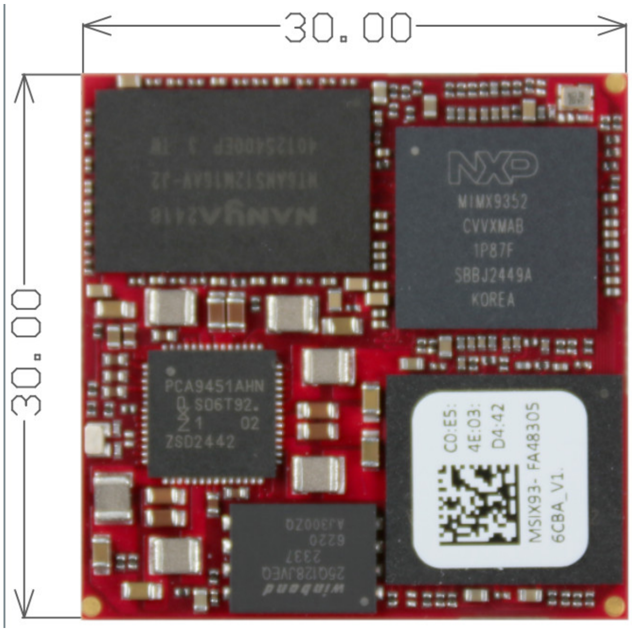
- NXP i.X93 CPU MIMX9352CVVXMAB
- 1GB LPDDR4 RAM
- 8GB eMMC NAND Flash
- 128MBit SPI-NOR
- 0°. . . +70°C

Please contact ARIES Embedded under sales@aries-embeded.de for more information about the availability of other standard products of MSIX93 or custom configurations.

3.4 Block Diagram

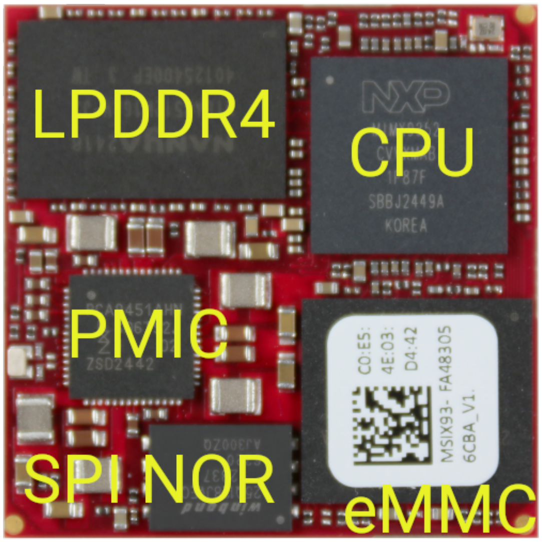


3.5 Dimensions

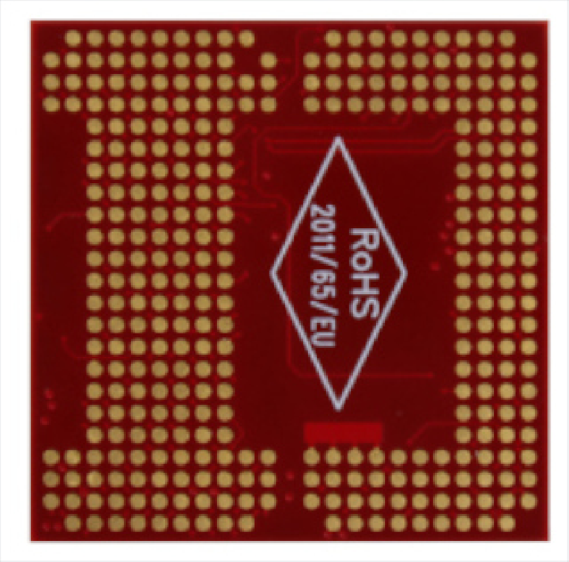


3.6 Part Overview

Assembly Top

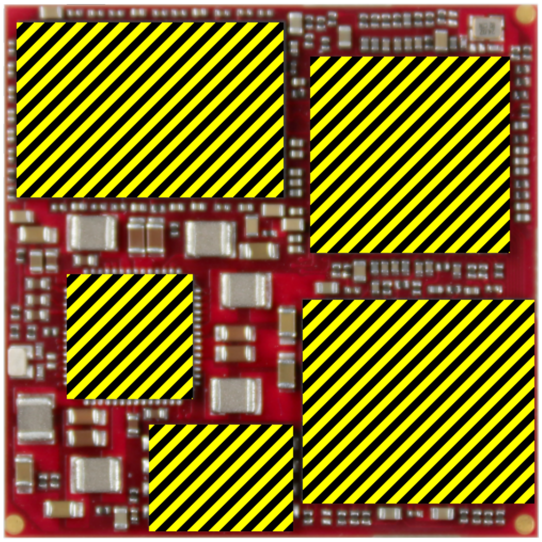


Assembly Bottom



3.7 Handling Recommendations

To avoid mechanical damage to the components populated on MSIX93 it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

FOUR

RESOURCES

4.1 Components

4.1.1 MPU

i.MX 93 applications processors deliver efficient machine learning (ML) acceleration and advanced security with integrated EdgeLock® secure enclave to support energy-efficient edge computing.

The i.MX 93 applications processors are the first in the i.MX portfolio to integrate the scalable Arm Cortex-A55 core, bringing performance and energy efficiency to Linux®-based edge applications and the Arm Ethos™-U65 microNPU, enabling developers to create more capable, cost-effective and energy-efficient ML applications.

Optimizing performance and power efficiency for Industrial, IoT and automotive devices, i.MX 93 processors are built with NXP's innovative Energy Flex architecture. The SoCs offer a rich set of peripherals targeting automotive, industrial and consumer IoT market segments.

For more information about the i.MX93 microprocessor please refer to the documentation which is available from NXP.

4.1.2 LPDDR4 RAM

The MSIX93 is equipped with a NANYA NT6AN512M16AV-J2 LPDDR4 RAM, providing up to 8 Gbit of 16-bit memory. The device is designed for the commercial temperature range of -30°C … +105°C. The memory interface operates at a data rate of up to 4267 Mbps.

4.1.2.1 MPU Signals for LPDDR4

MPU Signal	Function	LPDDR4 Signal		MPU Signal	Function	LPDDR4 Signal	Comment
E4	DRAM_DQ0	N1		H2	CA0_A	H2	
B2	DRAM_DQ1	N2		J2	CA1_A	G1	
E2	DRAM_DQ2	M1		H9	CA2_A	F2	
F2	DRAM_DQ3	M2		H10	CA3_A	E1	
F4	DRAM_DQ4	K1		H11	CA4_A	E2	
C2	DRAM_DQ5	K2		J11	CA5_A	D1	
C4	DRAM_DQ6	J1		J8	CK_A#	G4	
B4	DRAM_DQ7	J2		J9	CK_A	G5	
F11	DRAM_DQ8	V1		J4	CKE_A	H1	
C11	DRAM_DQ9	V2		H4	CS_A	F1	
E11	DRAM_DQ10	U2		C3	DMI0_A	L2	
B11	DRAM_DQ11	U1		C10	DMI1_A	T2	
F9	DRAM_DQ12	R1		T11	DRAM_RESET_N	D2	Pulldown GND 10k
E9	DRAM_DQ13	R2					
C9	DRAM_DQ14	P2					
B9	DRAM_DQ15	P1					
D3	DRAM_DQS0_T	N4					
E3	DRAM_DQS0_C	L4					
D10	DRAM_DQS1_T	R4					
E10	DRAM_DQS1_C	R5					

4.1.3 SPI-NOR Flash

MSIX93 features a SPI-NOR device in a range of 128MBit to 512MBit.

Device	Capacity
W25Q128JVEIQ	128MBit
W25Q256JVEIQ	256MBit
W25Q512JVEIQ	512MBit

The SPI-NOR flash device uses the following connections:

MPU Pin	Function	SPI-NOR Pin
U16	CS#	1
V14	IO1	2
U14	IO2	3
	GND	4
T16	IO0	5
V16	CLK	6
T14	IO3	7
	VCC	7

4.1.4 eMMC Flash

The MSIX93 supports one eMMC NAND Flash in the range of 4-64 GByte. The eMMC provides a high-speed memory card interface compliant with JEDEC Version 5.0, eliminating the need for users to be concerned about directly controlling Flash Memories.

MPU Pin	Function	eMMC Pin
AA12	SDMMC1_CMD	M5
Y16	SDMMC1_D7	B6
Y15	SDMMC1_D6	B5
Y14	SDMMC1_D5	B4
Y13	SDMMC1_D4	B3
AA13	SDMMC1_D3	B2
AA16	SDMMC1_D2	A5
AA15	SDMMC1_D1	A4
AA14	SDMMC1_D0	A3
Y12	STROBE	H5
Y11	SDMMC1_CK	M6
–	NRST#	K5

The signal NRST# of the eMMC is tied via 10k pull-up to 1.8V.

4.1.5 PMIC

The power management on the MSIX93 SoM is provided by a NXP PCA9451A fully integrated power management IC.

The PCA9451A is a single chip power management IC (PMIC) designed to support i.MX 93x family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5 V adapter non-portable applications. The device provides six high efficiency step-down regulators, three LDOs, one 400 mA load switch, 2-channel level translator and 32.768 kHz crystal oscillator driver.

Three buck regulators support dynamic voltage scaling (DVS)1 along with programmable ramping up and down time. The buck regulators support remote sense to compensate IR drop to load from buck regulator, allowing better performance to meet the demand for accuracy in critical supply rails. This device is characterized across -40 °C to 105 °C ambient temperature range, making it a good option for the industrial, extended industrial and consumer markets.

The MSIX93 supports a supply voltage range of 2.85V to 5.5V. This range fully includes the OSM standard supply voltage of 5V (+/-5%).

PMIC connections

MPU Pin	Function	PMIC Pin	OSM Pad	Notes
	SYS_RST#	–	U17	10k pull-up 1.8V
A17	ON_REQ	39		
B18	STBY_REQ	40		
D21	SDA	42		
D20	SCL	41		
J18	WDOG#	28		100k pull-up 1.8V
A16	POR#	9	Y14	
E16	CLK32K_OUT	7		
AA17	SD2_RST#	12		Reset SD-card

4.2 Interfaces

4.2.1 I2C

When using MSIX93 in conformity to the OSM standard two I2C interfaces are available:

MPU Pin	Function	SiP Pads	Notes
C20	I2C1_SCL	AA15	2k2 pullup to VCC
C21	I2C1_SDA	AA16	2k2 pullup to VCC
Y21	I2C3_SCL	AA20	2k2 pullup to VCC
W20	I2C3_SDA	AA21	2k2 pullup to VCC

4.2.2 I2S

When using MSIX93 in conformity to the OSM standard one I2S interface will be available:

As of april 2026 I2S has not yet been implemented.

MPU Pin	Function	OSM Pad
-/-	I2S_MCLK	V18
-/-	I2S_A_LRCLK	W18
-/-	I2S_A_BITCLK	W20
-/-	I2S_A_DATA_IN	V21
-/-	I2S_A_DATA_OUT	W21
-/-	I2S_B_LRCLK	T18
-/-	I2S_B_BITCLK	T19
-/-	I2S_B_DATA_IN	V19
-/-	I2S_B_DATA_OUT	W19

4.2.3 SPI

When using MSIX93 in conformity to the OSM standard three SPI interface are available:

MPU Pin	Function	OSM Pad
U21	SPI_A_CS1#	K17
V20	SPI_B_CS1#	L17
J20	SPI_A_SDI_(IO1)	U15
K20	SPI_A_SDO_(IO0)	V15
J21	SPI_A_CS0#	Y15
K21	SPI_A_SCK	U16
N21	SPI_B_SDI	Y22
P20	SPI_B_SDO	Y23
N20	SPI_B_CS0#	AA23
P21	SPI_B_SCK	Y21

4.2.4 JTAG

MPU Pin	Function	OSM Pad
Y1	JTAG_TCK(SWCLK)	N17
W2	JTAG_TMS(SWDIO)	N19
W1	JTAG_TDI	P17
Y2	JTAG_TDO(SWO)	R17

4.2.5 UART

4.2.5.1 UART

MPU Pin	Function	OSM Pad
E20	UART_CON_RX	D22
E21	UART_CON_TX	D23
L18	UART_A_RX	A14
L17	UART_A_TX	B13
L21	UART_A_RTS	C13
L20	UART_A_CTS	C14
F20	UART_B_RX	D14
F21	UART_B_TX	D13

4.2.6 TIMER/PWM

MPU Pin	Function	OSM Pad
U20	PWM_0/DISP_BL_PWM	E18

4.2.7 Ethernet

MPU Pin	Function	OSM Pad
ETHERNET A		
AA10	ETH_MDIO	T15
AA11	ETH_MDC	T16
AA7	ETH1_A(R)(G)MII_RX_CLK	R15
Y8	ETH_A(R)(G)MII_RX_DV(ER)	M16
AA8	ETH_A(S)(R)(G)MII_RXD0	K15
Y9	ETH_A(S)(R)(G)MII_RXD1	L15
AA9	ETH_A(R)(G)MII_RXD2	N15
Y10	ETH_A(R)(G)MII_RXD3	P15
V10	ETH_A(R)(G)MII_TX_EN(ER)	K16
U10	ETHA_A(R)(G)MII_TX_CLK	J15
T10	ETH_A(S)(R)(G)MII_TXD3	G16
V8	ETH_A(S)(R)(G)MII_TXD2	H16
U8	ETH_A(S)(R)(G)MII_TXD1	G15
T8	ETH_A(S)(R)(G)MII_TXD0	H15
ETHERNET B		
C7	ETH_B_MDIO	AA6
C6	ETH_B_MDC	Y7
P1	ETH_B(R)(G)MII_RX_CLK	AA3
L1	ETH_B(R)(G)MII_RX_DV(ER)	Y4
J1	ETH_B(S)(R)(G)MII_RXD0	AA4
K1	ETH_B(S)(R)(G)MII_RXD1	Y5
M1	ETH_B(R)(G)MII_RXD2	AA5
N1	ETH_B(R)(G)MII_RXD3	Y6
J2	ETH_B(R)(G)MII_TX_EN(ER)	V6
H1	ETH_B(R)(G)MII_TX_CLK	U6
F2	ETH_B(S)(R)(G)MII_TXD3	T10
G2	ETH_B(S)(R)(G)MII_TXD2	V8
F1	ETH_B(S)(R)(G)MII_TXD1	U8
G1	ETH_A(S)(R)(G)MII_TXD0	T8

4.2.8 CAN

MPU Pin	Function	OSM Pad
G17	CAN_A_TX	AC17
J17	CAN_A_RX	AB17
V21	CAN_B_TX	AC19
W21	CAN_B_RX	AB19

4.2.9 USB

MPU Pin	Function	OSM Pad
B14	USB_A_D_P	AC14
A14	USB_A_D_N	AB13
AA2	USB_A_EN	AC16
C11	USB_A_ID	AB14
F12	USB_A_VBUS	AB16
B15	USB_B_D_P	AC22
A15	USB_B_D_N	AB23
V4	USB_B_EN	AC20
C11	USB_B_ID	AB22
E14	USB_B_VBUS	AB20

4.2.10 DISPLAY-LVDS

MPU Pin	Function	OSM Pad
A5	DSI_DATA0_N	AB11
B5	DSI_DATA0_P	AB10
A4	DSI_DATA1_N	AC9
B4	DSI_DATA1_P	AC8
A2	DSI_DATA2_N	AC6
B2	DSI_DATA2_P	AC5
B1	DSI_DATA3_N	AB5
C1	DSI_DATA3_P	AB4
A3	DSI_CLOCK_N	AB8
B3	DSI_CLOCK_P	AB7

4.2.10.1 LVDS availability on OSMEVK

The LVDS signals of the i.MX93 CPU are converted to RGB signals on the adapter board for use of RGB-TFT on the OSMEVK. For further reference, refer to the OSMEVK Manual .

4.2.11 SD-CARD

MPU Pin	Function	OSM Pad
AA19	SD2_CLK	F21
Y19	SD2_CMD	E20
Y18	SD2_DATA0	G20
AA18	SD2_DATA1	G21
Y20	SD2_DATA2	H20
AA20	SD2_DATA3	H21
Y17	SD2_CD#	J21

4.2.12 GPIO

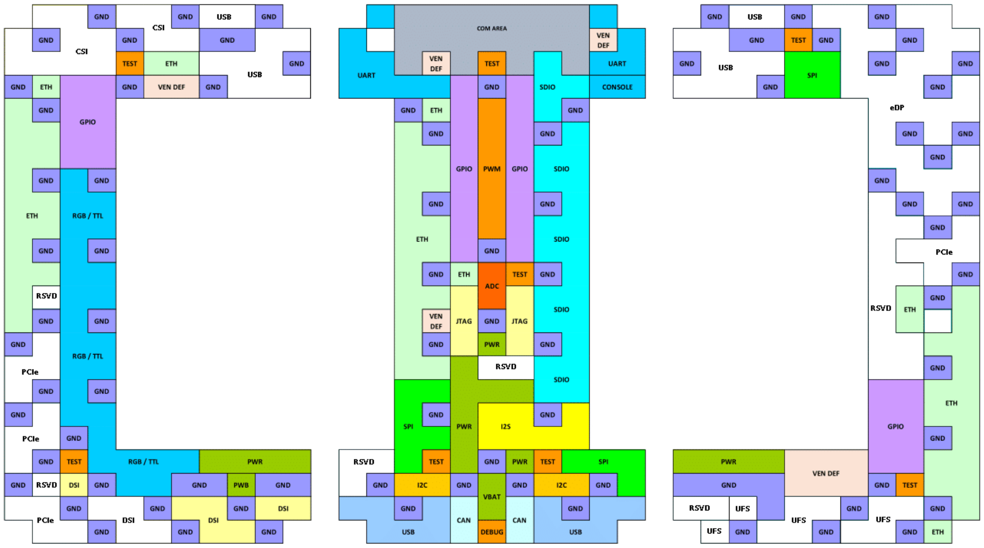
MPU Pin	Function	OSM Pad
M20	GPIO_A_0	D17
M21	GPIO_A_1	E17
N17	GPIO_A_2	F17
N18	GPIO_A_3	G17
R21	GPIO_A_4	H17
R20	GPIO_A_5	J17
U21	GPIO_A_6	K17
V20	GPIO_A_7	L17
R18	GPIO_B_0	D19
R17	GPIO_B_1	E19
T20	GPIO_B_2	F19
T21	GPIO_B_3	G19
U18	GPIO_B_4	H19
G18	GPIO_B_5	J19
G20	GPIO_B_6	K19
H20	GPIO_B_7	L19

4.2.13 ADC

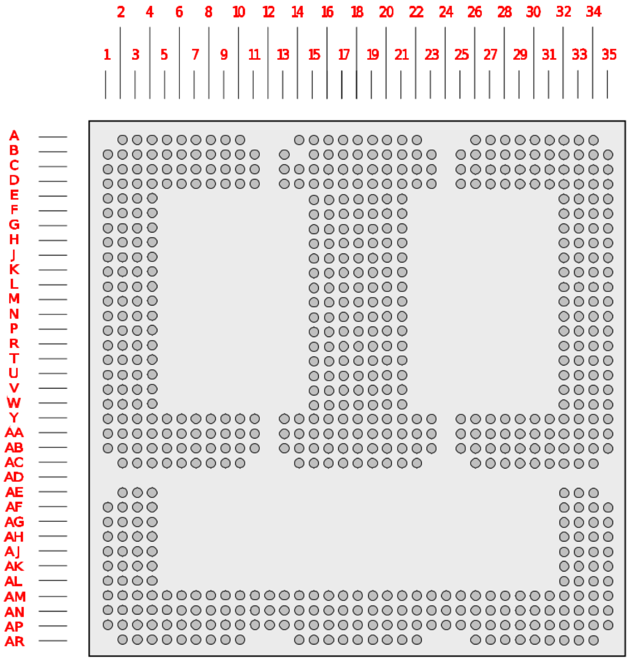
MPU Pin	Function	OSM Pad
B19	ADC_IN0	M18
A20	ADC_IN1	N18
B20	ADC_IN2	B22
B21	ADC_IN3	C16

4.2.14 MSIX93 SiP Pads

4.2.14.1 Contact Groups



4.2.14.2 Contact Grid Numbering



4.2.14.3 Contact Table

MPU Pin	Function	OSM Pad		MPU Pin	Function	OSM Pad
ETHERNET						
U10	ETH1_TXC	AA8		U6	ETH2_TXC	U12
T8	ETH1_TXD0	Y9		T8	ETH2_TXD0	V12
U8	ETH1_TXD1	AA9		U8	ETH2_TXD1	V10
V8	ETH1_TXD2	Y10		V8	ETH2_TXD2	U10
T10	ETH1_TXD3	Y8		T10	ETH2_TXD3	AA10
V10	ETH1_TX_CTL	AA7		V6	ETH2_TX_CTL	AA11
AA7	ETH1_RXC	AA4		AA3	ETH2_RXC	T8
AA8	ETH1_RXD0	Y5		AA4	ETH2_RXD0	U8
Y9	ETH1_RXD1	AA5		Y5	ETH2_RXD1	V8
AA9	ETH1_RXD2	Y6		AA5	ETH2_RXD2	T10
Y10	ETH1_RXD3	Y4		Y6	ETH2_RXD3	V6
Y8	ETH1_RX_CTL	AA3		Y4	ETH2_RX_CTL	U6
AA11	ETH1_MDC	W11		Y7	ETH2_MDC	AA6
AA10	ETH1_MDIO	T12		AA4	ETH2_MDIO	Y7
USB						
B14	USB_A_D_P	AC14		E14	USB_B_VBUS	AB20
AB13	USB_A_D_N	AB13				D10
AA2	USB_A_EN	AC16				D11
C11	USB_A_ID	AB14				C10
		AC15				D9
F12	USB_A_VBUS	AB16				C8
B15	USB_B_D_P	AC22				C9
A15	USB_B_D_N	AB23				A9
V4	USB_B_EN	AC20				A8
AB22	USB_B_ID	AB22				B11
		AC21				B10
SDIO						
AA19	SDIO_A_CLK	F21				T21
Y19	SDIO_A_CMD	E20				U20
Y17	SDIO_A_CD#	J21				L20
		D20				L21
Y18	SDIO_A_D0	G20				M21
AA18	SDIO_A_D1	G21				N20
Y20	SDIO_A_D2	H20				N21
AA20	SDIO_A_D3	H21				P20
		D21				P21
		C20				R21
		K20				U21
		K21				T20
UART						
E20	UART_CON_RX	D22		F21	UART_B_TX	D13
E21	UART_CON_TX	D23				D15
L18	UART_A_RX	A14				D16
L17	UART_A_TX	B13				A22
L21	UART_A_RTS	C13				B23

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Table 2 – continued from previous page

MPU Pin	Function	OSM Pad		MPU Pin	Function	OSM Pad
L20	UART_A_CTS	C14				C22
F20	UART_B_RX	D14				C23
SPI						
U21	SPI_A_CS1#	K17		J21	SPI_A_CS0#	Y15
V20	SPI_B_CS1#	L17		K21	SPI_A_SCK	U16
J20	SPI_A_SDI _(IO1)	U15		N21	SPI_B_SDI	Y22
K20	SPI_A_SDO _(IO0)	V15		P20	SPI_B_SDO	Y23
		W16		N20	SPI_B_CS0#	AA23
		W15		P21	SPI_B_SCK	Y21
I2C						
C20	I2C_A_SCL	AA15		Y21	I2C_B_SCL	AA20
C21	I2C_A_SDA	AA16		W20	I2C_B_SDA	AA21
I2S						
		V18				T18
		W18				T19
		W20				V19
		V21				W19
		W21		–	–	–
GPIO						
	GPIO_A_0	D17			GPIO_B_4	H19
	GPIO_A_1	E17			GPIO_B_5	J19
	GPIO_A_2	F17			GPIO_B_6	K19
	GPIO_A_3	G17			GPIO_B_7	L19
	GPIO_A_4	H17				D3
	GPIO_A_5	J17				DD4
	GPIO_A_6	K17				E3
	GPIO_A_7	L17				E4
	GPIO_B_0	D19			GPIO_C_4	F3
	GPIO_B_1	E19				F4
	GPIO_B_2	F19			GPIO_C_6	G3
	GPIO_B_3	G19				G4
ADC						
B19	ADC_0	M18		B20	ADC_2	B22
A20	ADC_1	N18		B21	ADC_3	C16
PWM						
U20	PWM_0	E18				H18
		F18				J18
		G18				K18
VENDOR DEFINED PINS						
B20	ADC_IN2	B22		G21	BOOT-STRAP-2	D6
B21	ADC_IN3	C16		H21	BOOT-STRAP-3	D7
COM						
	COM_AREA_1	A15			COM_AREA_10	B17
	COM_AREA_2	A16			COM_AREA_11	B18
	COM_AREA_3	A17			COM_AREA_12	B19
	COM_AREA_4	A18			COM_AREA_13	B20
	COM_AREA_5	A19			COM_AREA_14	B21
	COM_AREA_6	A20			COM_AREA_15	C15

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Table 2 – continued from previous page

MPU Pin	Function	OSM Pad		MPU Pin	Function	OSM Pad
	COM_AREA_7	A21			COM_AREA_16	C17
	COM_AREA_8	B15			COM_AREA_17	C19
	COM_AREA_9	B16			COM_AREA_18	C21
CONFIG						
	DEBUG_EN	AC18			TEST_GENERIC	C18
JTAG						
Y1	JTAG_TCK(SWLCK)	N17		W1	JTAG_TDI	P17
		P19		Y2	JTAG_TDO(SWO)	R17
W2	JTAG_TMS(SWDIO)	N19				R19
RGB						
		Y7				R3
		AA6				P3
		Y6				N3
		AA5				N4
		Y5				M3
		Y4				M4
		W4				L3
		V3				K3
		V4				K4
		U3				J4
		T3				J3
		T4				H3
		R4				
MIPI-DSI						
		AB11				AC5
		AB10				AB5
		AC9				AB4
		AC8				AB8
		AC6				AB7
MIPI-CSI						
A11	CSI_A _DATA0_N	C1				B6
B11	CSI_A _DATA0_P	B1				B7
A10	CSI_A _DATA1_N	A2		D10	CSI_A_CLOCK_N	B3
B10	CSI_A| A3 _DATA1_P			E10	CSI_A_CLOCK_P	B4
		A5		C21	CSI_A_TX_N	C3
		A6		C20	CSI_A_TX_P	C4
PCIe						
	PCIe_A_HSI0_P	AB1			PCIe_REFLCK_P	W1
	PCIe_A_HSI0_N	AB2			PCIe_REFLCK_N	Y1
	PCIe_A_HSO0_P	AC2			PCIe_WAKE#	T2
	PCIe_A_HSO0_N	AC3			PCIe_SMDAT	U1
	PCIe_A_PERST#	V2			PCIe_SMCLK	T1
	PCIe_CLKREQ#	W2			PCIe_SM _ALERT#	R2
PWR						
	VCC_IN_5V	Y17				T17
		Y19				M19
		W17				Y16
	VCC_OUT_IO	U18				Y20

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Table 2 – continued from previous page

MPU Pin	Function	OSM Pad		MPU Pin	Function	OSM Pad
		AA18				Y8
		AB18				Y9
	RESET_IN#	U17				Y10
A16	RESET_OUT#	Y14				Y11
	CARRIER _PWR_EN	V17				Y3
		Y13				C5
E21	BOOT_SEL0#	U19		A19	PWR_BTN#	AA9
F21	BOOT_SEL1#	R18				
GND						
–	GND	D18		–	GND	R16
–	GND	E15		–	GND	R20
–	GND	E21		–	GND	V16
–	GND	F16		–	GND	V20
–	GND	F20		–	GND	Y18
–	GND	J16		–	GND	AA14
–	GND	J20		–	GND	AA17
–	GND	L18		–	GND	AA19
–	GND	M16		–	GND	AA22
–	GND	M20		–	GND	AB15
–	GND	P18		–	GND	AB21
–	GND	A4		–	GND	R1
–	GND	A7		–	GND	U2
–	GND	A10		–	GND	U4
–	GND	B2		–	GND	V1
–	GND	B5		–	GND	W3
–	GND	B8		–	GND	Y2
–	GND	B9		–	GND	AA1
–	GND	C11		–	GND	AA4
–	GND	D1		–	GND	AA7
–	GND	D5		–	GND	AA8
–	GND	D8		–	GND	AA10
–	GND	E2		–	GND	AA11
–	GND	H2		–	GND	AB3
–	GND	H4		–	GND	AB6
–	GND	L2		–	GND	AB9
–	GND	L4		–	GND	AC4
–	GND	P2		–	GND	AC7
–	GND	P4		–	GND	AC10
RESERVED						
		AA13				AA2
		N2				

4.3 Conversion of MSIX93 interfaces to OSMEVK baseboard

The adapter board OSMEVK_ADAP_MSIX93 (**2**) enables the conversion of interfaces and/or voltage levels from the MSIX93 module (**1**) to the appropriate value and direction, ensuring compatibility with the SoM functionality on the OSMEVK baseboard (**3**).

MPU Pin	OSM Pad	MSIX93 Function	OSM_ADAP Function	OSMEVK Connector Pin
ETHERNET				
AA10	T15	ETH_MDIO	ETH_A_MDIO	P1-9
AA11	T16	ETH_MDC	ETH_A_MDC	P1-11
			ETH_PHY_CLK	P1-15
AA7	R15	ETH1_A(R)(G)MII_RX_CLK	ETH_A_RXCLK	P1-21
Y8	M16	ETH_A(R)(G)MII_RX_DV(ER)	ETH_A_RXCTL	P1-23
AA8	K15	ETH_A(S)(R)(G)MII_RXD0	ETH_A_RXD0	P1-25
Y9	L15	ETH_A(S)(R)(G)MII_RXD1	ETH_A_RXD1	P1-27
AA9	N15	ETH_A(R)(G)MII_RXD2	ETH_A_RXD2	P1-29
Y10	P15	ETH_A(R)(G)MII_RXD3	ETH_A_RXD3	P1-31
V10	K16	ETH_A(R)(G)MII_TX_EN(ER)	ETH_A_TXCTL	P1-37
U10	J15	ETHA_A(R)(G)MII_TX_CLK	ETH_A_TXCLK	P1-39
T10	G16	ETH_A(S)(R)(G)MII_TXD3	ETH_A_TXD3	P1-41
V8	H16	ETH_A(S)(R)(G)MII_TXD2	ETH_A_TXD2	P1-43
U8	G15	ETH_A(S)(R)(G)MII_TXD1	ETH_A_TXD1	P1-45
T8	H15	ETH_A(S)(R)(G)MII_TXD0	ETH_A_TXD0	P1-47
CAN				
G17	AC17	CAN_A_TX	CAN_A_TX	P4-1
J17	AB17	CAN_A_RX	CAN_A_RX	P4-2
V21	AC19	CAN_B_TX	CAN_B_TX	
W21	AB19	CAN_B_RX	CAN_B_RX	
USB				
B14	AC14	USB_A_D_P	USB_A_D_P	P4-20
A14	AB13	USB_A_D_N	USB_A_D_N	P4-22
AA2	AC16	USB_A_EN	USB_A_EN	P4-14
C11	AB14	USB_A_ID	USB_A_ID	P4-16
	AC15	USB_A_OC#	USB_A_OC#	P4-12
F12	AB16	USB_A_VBUS	USB_A_VBUS	P4-4, P4-6, P4-8
B15	AC22	USB_B_D_P	USB_B_D_P	P4-32
A15	AB23	USB_B_D_N	USB_B_D_N	P4-34
V4	AC20	USB_B_EN	USB_B_EN	P4-26
C11	AB22	USB_B_ID	USB_B_ID	
	AC21	USB_B_OC#	USB_B_OC#	P4-28
E14	AB20	USB_B_VBUS	USB_B_VBUS	
SDIO				
AA19	F21	SDIO_A_CLK	SDIO_A_CLK	P2-27
Y19	E20	SDIO_A_CMD	SDIO_A_CMD	P2-25
AA17	J21	SDIO_A_CD#	SDIO_A_CD#	P2-37
	D20	SDIO_A_WP	SDIO_A_WP	GND
Y18	G20	SDIO_A_D0	SDIO_A_D0	P2-29
AA18	G21	SDIO_A_D1	SDIO_A_D1	P2-31

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MPU Pin	OSM Pad	MSIX93 Function	OSM_ADAP Function	OSMEVK Connector Pin
Y20	H20	SDIO_A_D2	SDIO_A_D2	P2-33
AA20	H21	SDIO_A_D3	SDIO_A_D3	P2-35
	D21	SDIO_A_D_PWR_EN	SDIO_A_D_PWR_EN	P23
	C20	SDIO_A_D_IOPWR	SDIO_A_D_IOPWR	
UART				
E20	D22	UART_CON_RX	CONS_RX	P2-48
E21	D23	UART_CON_TX	CONS_TX	P2-46
L18	A14	UART_A_RX	UART_A_RX	P2-38
L17	B13	UART_A_TX	UART_A_TX	P2-40
SPI				
J20	U15	SPI_A_SDI_(IO1)	SPI_A_SDI	P4-17
K20	V15	SPI_A_SDO_(IO0) | SPI_A_SDO		P4-15
J21	Y15	SPI_A_CS0# | SPI_A_CS0#		P4-13
K21	U16	SPI_A_SCK | SPI_A_SCK		P4-11
I2C				
C20	AA15	I2C_A_SCL	I2C_A_SCL	P4-35
C21	AA16	I2C_A_SDA	I2C_A_SDA	P4-37
Y21	AA20	I2C_B_SCL	I2C_B_SCL	P4-38
W20	AA21	I2C_B_SDA	I2C_B_SDA	P4-40
GPIO				
M20	D17	GPIO_A_0	GPIO_A_0	P2-5
M21	E17	GPIO_A_1	GPIO_A_1	P2-7
N17	F17	GPIO_A_2	GPIO_A_2	P2-9
N18	G17	GPIO_A_3	GPIO_A_3	P2-11
R21	H17	GPIO_A_4	GPIO_A_4	P2-13
R20	J17	GPIO_A_5	GPIO_A_5	P2-15
U21	K17	GPIO_A_6	GPIO_A_6	P2-17
V20	L17	GPIO_A_7	GPIO_A_7	P2-19
ADC				
B19	M18	ADC_0	ADC_0	P2-43
A20	N18	ADC_1	ADC_1	P2-45
VENDOR-DEFINED				
F12	P16	USB_A_VBUS	USB_A_VBUS	P4-4, P4-6, P4-8
G21	D6	BOOT-STRAP-2	BOOT_SEL2#	P4-50
F21	D7	BOOT-STRAP-1	BOOT_SEL1#	P4-48
F21	Y30	BOOT-STRAP-1	BOOT_SEL1#	P4-48
G21	Y31	BOOT-STRAP-2	BOOT_SEL2#	P4-50
JTAG				
Y1	N17	JTAG_TCK(SWLCK)	JTAG_TCK	P2-18
W2	N19	JTAG_TMS(SWDIO)	JTAG_TMS	P2-16
W1	P17	JTAG_TDI	JTAG_TDI	P2-14
Y2	R17	JTAG_TDO(SWO)	JTAG_TDO	P2-12
PWR				
	U17	RESET_IN#	RESET_IN#	P4-29
A16	Y14	RESET_OUT#	RESET_OUT#	P4-29
	V17	CARRIER_PWR_EN	CARRIER_PWR_EN	P4-31

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MPU Pin	OSM Pad	MSIX93 Function	OSM_ADAP Function	OSMEVK Connector Pin
E21	U19	BOOT_SEL#0	BOOT_SEL#0	P4-46
F21	R18	BOOT_SEL#1	BOOT_SEL#1	P4-48
A19	AA9	PWR_BTN#	PWR_BTN#	P4-44

CPU Pin	OSM Pin	MSMP1 Function	OS-MEVK_ADAP Function	OSMEVK Connector Pin
COM				
M3	A15	PD14 (GPIO/FMC_AD0)	–	–
L1	A16	PD15 (GPIO/FMC_AD1)	–	–
C10	A17	PD0 (GPIO/FMC_AD2/I2C5_SDA)	–	–
B10	A18	PD1 (GPIO/FMC_AD3/I2C5_SCL)	–	–
W10	A19	PE7 (GPIO/FMC_AD4/QSPI_BK2_IO0)	–	–
Y12	A20	PE8 (GPIO/FMC_AD5/QSPI_BK2_IO1)	–	–
W11	A21	PE9 (GPIO/FMC_AD6/QSPI_BK2_IO2)	–	–
W14	B15	PE10 (GPIO/FMC_AD7/QSPI_BK2_IO3)	–	–
AB9	B16	PD11 (GPIO/FMC_CLE)	–	–
W12	B17	PD12 (GPIO/FMC_ALE/TIM4_CH1)	–	–
L3	B18	PD6 (GPIO/FMC_NWAIT)	–	–
A9	B19	PD5 (GPIO/FMC_NWE)	–	–
W15	B20	PG9 (GPIO/FMC_NCE)	–	–
N2	C15	PC13 (RTC_OUT1)	–	–
F3	C17	LCD_R0	–	–
L4	C19	LCD_G0	–	–
B8	C21	LCD_B0	–	–

4.4 Schematics

Schematics for the MSIX93 SiP may be obtained on request. Please contact sales@aries-embedded.de.