MRZG2LS/MRZV2LS Hardware Manual

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	20.04.2023	wa	Initial creation
1.1	28.01.2024	aw	Added pinout for edge connector

CHAPTER

TWO

OVERVIEW

2.1 MRZG2LS and MRZV2LS

The MRZG2LS and MRZV2LS are SMARC V2.1 compliant System-on-Modules based on Renesas RZ Family architecture. They offer high-performance for embedded systems.The SMARC Modules are used as building blocks for portable and stationary embedded systems. The modular approach allows for the following;

- Scalability
- Fast time to market
- Upgradability
- Low costs
- Low power and
- Small physical size.

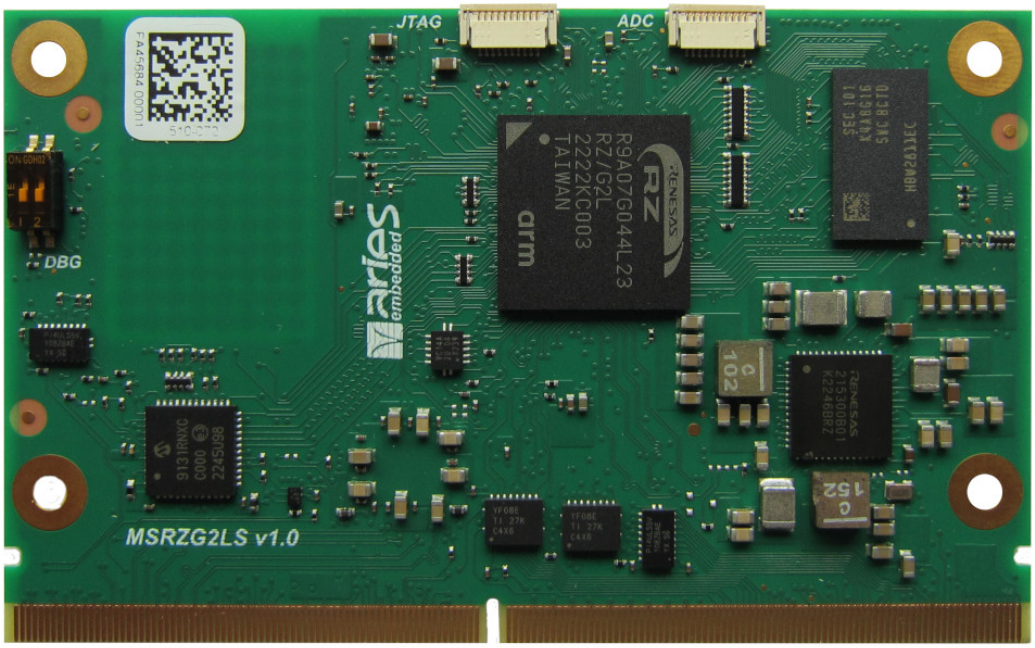
The RZ family has comprehesive development tools which also provides an ideal environment for development of embedded Linux applications.Thus simplifying the software development process and integration.

The RZ/G2L microprocessor includes a Cortex®-A55 (1.2 GHz) CPU, 16-bit DDR3L / DDR4 interface, 3D graphics engine with Arm Mali-G31 and video codec (H.264). It also has many interfaces such as camera input, display output, USB 2.0, and Gigabit-Ethernet, making it ideal for applications such as entry-class industrial human-machine interfaces (HMIs) and embedded devices with video capabilities.

RZ/V2L is equipped with a Cortex®-A55 (1.2GHz) CPU and built-in AI accelerator “DRP-AI” for vision, which is Renesas’ original technology. “DRP-AI” is configured with DRP and AI-MAC. It also has a 16-bit DDR3L/DDR4 interface and a built-in 3D graphics engine with Arm Mali-G31 and video codec (H.264).

The DRP-AI’s excellent power efficiency eliminates the need for heat dissipation measures such as heat sinks or cooling fans. AI can be implemented cost efficiently not only in consumer electronics and industrial equipment but also in a wide range of applications such as point-of-sale (POS) terminals for retail. Also, the DRP-AI provides both real-time AI inference and image processing functions with the capabilities essential for camera support such as color correction and noise reduction. This enables customers to implement AI-based vision applications without requiring an external image signal processor (ISP).

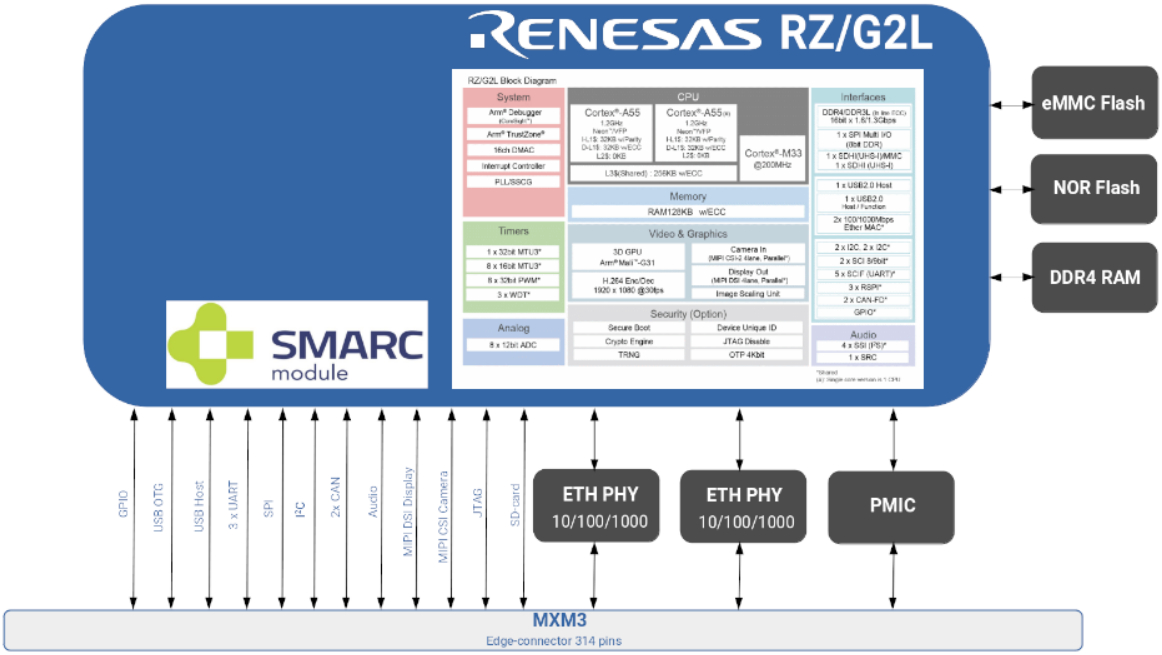
In summary both RZ/G2L and RZ/V2L microprocessors offer versatile and powerful solution for various embedded systems, with high performance offerings, advanced security features as well as low consumption of power.


JTAG
ADC
DBG
MSRZG2LS v1.0

2.2 Feature Set

- Single or Dual Cortex-A55, up to 1GHz
- optional AI accelerator; DRP-AI on MRZV2L
- 3D Graphics engine (Arm Mali-G31)
- Video Codec (H.264)
- Cortex-M33
- 512MB – 4GB DDR4 RAM
- SPI NOR
- 4GB-64GB eMMC NAND Flash
- dual 10/100/1000MBit Ethernet with PHY
- USB2.0 Host/OTG
- 2x CAN
- UART, I2C, SPI
- ADC
- Camera interface MIPI-CSI
- Display interface MIPI-DSI
- compliant to the SGET SMARC 2.1 standard
- commercial (0°C...+70°C) / industrial (-40°C...+85°C) temperature range

2.3 Block Diagram



2.4 Order Codes

The difference between the MRZG2LS and MRZV2LS is the microprocessor used. The connector used in with the RZ/V2L is pin-compatible with RZ/G2L. Therefore both function the same. Their key features are listed below:

MRZG2LS-BAA

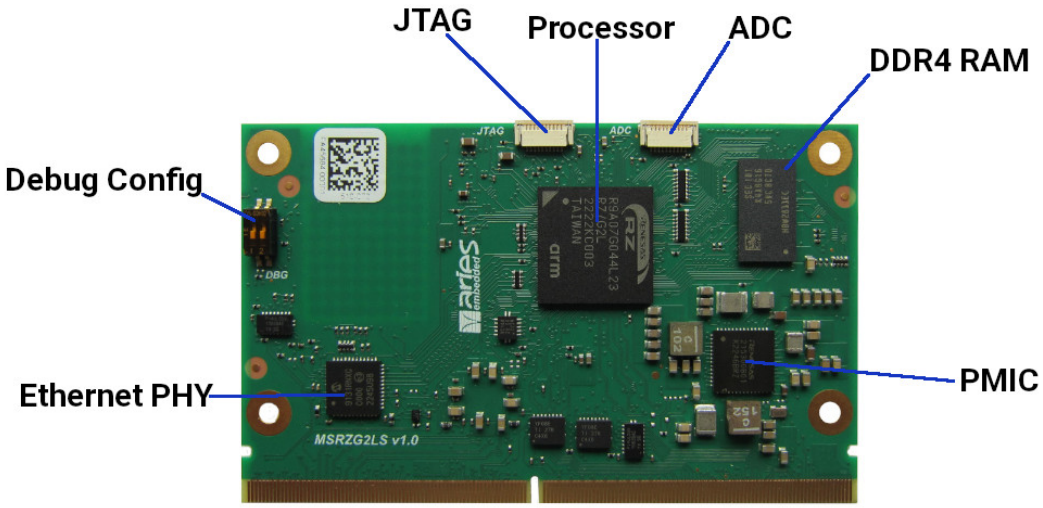
- Renesas RZ/G2L R9A07G044L23GBG#BC0
- 1GB DDR4 RAM
- 4GB eMMC
- 128MBit SPI-NOR
- 2x KSZ9131 PHY
- -25°...+85°C

MRZV2LS-BAA

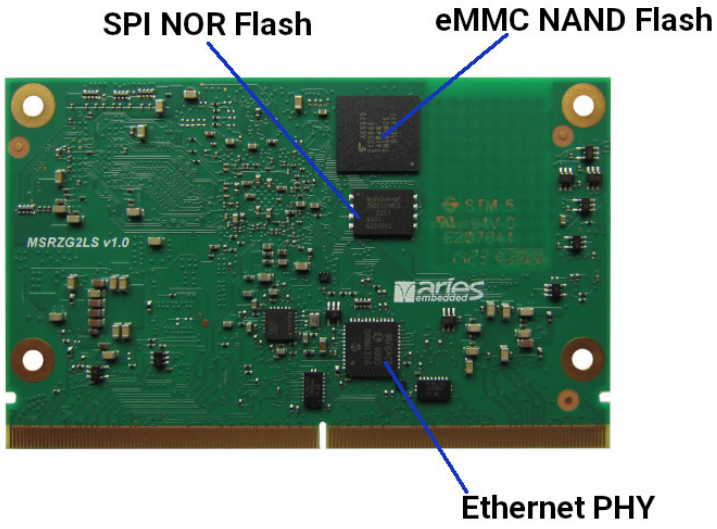
- Renesas RZ/V2L R9A07G044L23GBG#BC0
- 1GB DDR4 RAM
- 4GB eMMC
- 128MBit SPI-NOR
- 2x KSZ9131 PHY
- -25°...+85°C

2.5 Part Locations

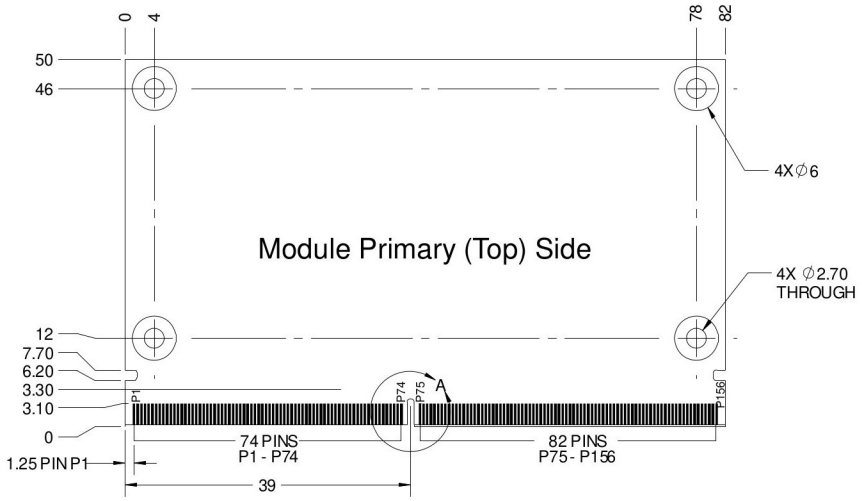
Assembly Top

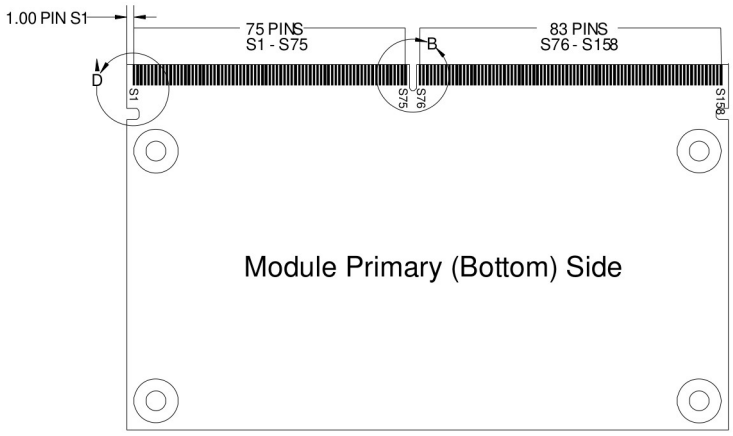


Assembly Bottom



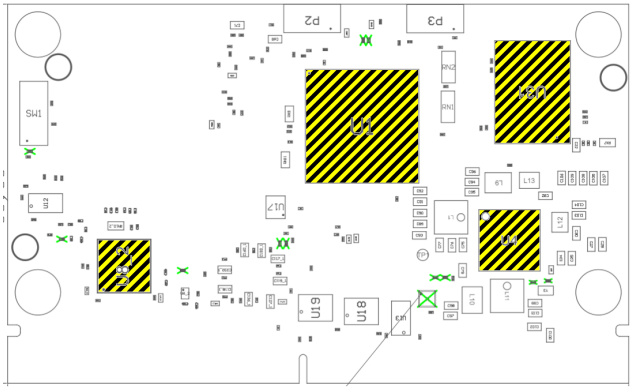
2.6 Mechanical Information





Handling Recommendation

To avoid mechanical damage to the components populated on SoM it is strongly recommended **not** to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



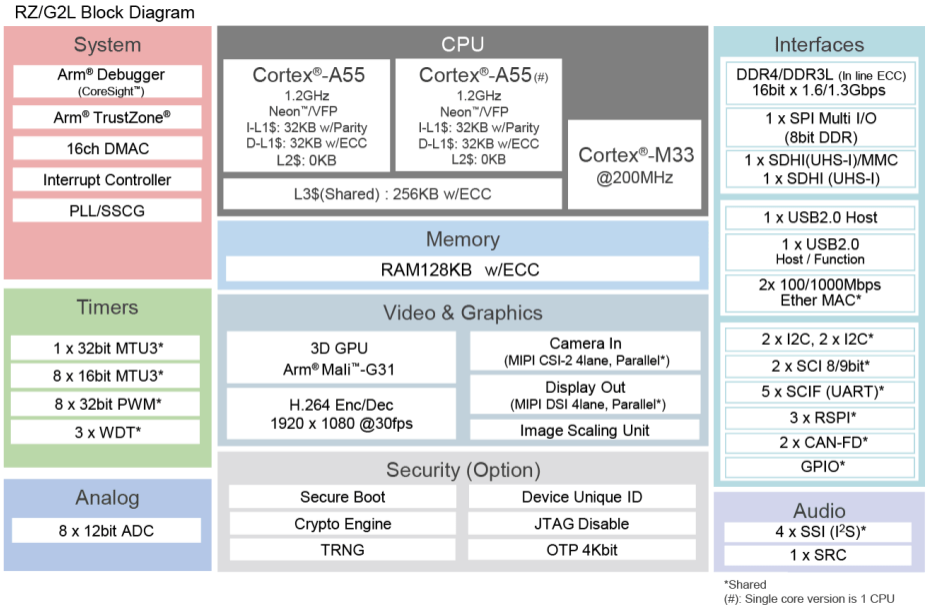
CHAPTER

THREE

RESOURCES

3.1 MPU

The RZ/G2L microprocessor includes a Cortex®-A55 (1.2 GHz) CPU, 16-bit DDR3L / DDR4 interface, 3D graphics engine with Arm Mali-G31 and video codec (H.264). It also has many interfaces such as camera input, display output, USB 2.0, and Gbit-Ether, making it ideal for applications such as entry-class industrial human-machine interfaces (HMIs) and embedded devices with video capabilities. The RZ/G2L is also package-compatible and pin-compatible with the RZ/V2L embedded with AI accelerator.



Feature Set

- Cortex-A55 (Dual or Single)
- Cortex-M33
- AI accelerator, DRP-AI (available on MSRZV2L)
- 3D Graphics engine (Arm Mali-G31)
- Video Codec (H.264)
- Camera interface (MIPI-CSI or Parallel-IF)
- Display interface (MIPI-DSI or Parallel-IF)
- USB2.0 interface 2ch,SD interface 2ch
- CAN interface (CAN-FD)
- Giga bit Ethernet 2ch
- Memory error detection / correction (ECC)
- DDR4 or DDR3L Memory interface

For more information about the RZ/G2L and RZ/V2L MCU please refer to the documentation which is available from Renesas.

3.1.1 MPU Derivatives

Depending on the targeted MPU the following derivatives are populated on MRZG2LS:

MPU Family	Derivative	Comment
RZ/G2L	R9A07G044L23GBG#BC0, dual CortexA55@1.2GHz, CortexM33@200MHz	
RZ/G2L	R9A07G044L27GBG#BCO, dual CortexA55@1.2GHz, CortexM33@200MHz	with security features
RZ/V2L	R9A07G054L23GBG#BC0, dual CortexA55@1.2GHz, CortexM33@200MHz	AI Accelerator “DRP-AI”

3.2 Boot Configuration

The MRZG2LS supports the following boot modes:

BOOT_SEL2#/ Pin P125	BOOT_SEL1#/ Pin P124	BOOT_SEL0#/ Pin P123	Boot Source
Float	GND	Float	Serial Boot through SCIF
Float	Float	GND	SoM eMMC NAND Flash
Float	Float	Float	SoM SPI NOR

3.3 Power Managment IC

The RZG2LS SoM hosts a RAA215300 as power management device. The RAA215300 is a high-performance, low-cost 9-channel PMIC designed for 32-bit and 64-bit MCU and MPU applications. It supports DDR3, DDR3L, DDR4, and LPDDR4 memory power interfaces. The internally compensated regulators, built-in Real-Time Clock (RTC), 32kHz crystal oscillator, and coin cell battery charger provide a highly integrated, small footprint power solution ideal for System-On-Module (SOM) applications. The spread spectrum feature and ultrasonic mode provide an effective solution for noise-sensitive RF and audio applications.

3.4 Programmable Clock Generator

The RZG2LS SoM hosts a 5P35023 programmable clock generator. The 5P35023 is a VersaClock programmable clock generator and is designed for low power, consumer, and high performance PCI Express applications. The 5P35023 device is a three PLL architecture design, and each PLL is individually programmable and allowing for up to five unique frequency outputs. The 5P35023 has built-in unique features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshot Reduction Technology (ORT) and Extreme Low Power DCO. An internal OTP memory allows the user to store the configuration in the device without programming after power up, then program the 5P35023 again through the I2C interface.

3.5 DDR4 SDRAM

By default the MRZG2LS SoM is populated 16bit wide with a 8GBit DDR4 SDRAM component K4A8G165WB-BITD.

MPU Signals for DDR4

MPU Pin	Function	DDR4 Pin		MPU Pin	Function	DDR4 Pin
G29	DDR_ADDR0	P3		V28	DDR_DQ0	G2
M27	DDR_ADDR1	P7		AB29	DDR_DQ1	F7
F28	DDR_ADDR2	R3		U28	DDR_DQ2	H3
F29	DDR_ADDR3	N7		AB28	DDR_DQ3	H7
L29	DDR_ADDR4	N3		V27	DDR_DQ4	H2
D29	DDR_ADDR5	P8		W28	DDR_DQ5	H8
L28	DDR_ADDR6	P2		U27	DDR_DQ6	J3
C28	DDR_ADDR7	R8		V29	DDR_DQ7	J7
H28	DDR_ADDR8	R2		AA29	DDR_DQSO_P	G3
E28	DDR_ADDR9	R7		Y28	DDR_DQS0_N	F3
R29	DDR_ADDR10	M3		W29	DDR_DM0	E7
K28	DDR_ADDR11	T2		AF28	DDR_DQ8	A3
P29	DDR_ADDR12	M7		AD29	DDR_DQ9	B8
E29	DDR_ADDR13	T8		AD28	DDR_DQ10	C3
J28	DDR_WE_N	L2		AE29	DDR_DQ11	C7
K29	DDR_CAS_N	M8		AH29	DDR_DQ12	C2
J29	DDR_RAS_N	L8		AE28	DDR_DQ13	C8
H27	DDR_BA0	N2		AF29	DDR_DQ14	D3
M28	DDR_BA1	N8		AG29	DDR_DQ15	D7

continues on next page

Table 1 – continued from previous page

MPU Pin	Function	DDR4 Pin		MPU Pin	Function	DDR4 Pin
–	DDR_BG0	M2		AC26	DDR_DQS1_P	B7
N29	DDR_ODT0	K3		AC27	DDR_DQS1_N	A7
T29	DDR_CLK_P	K7		AC29	DDR_DM1	E2
T28	DDR_CLK_N	K8		–	GND	F9
N28	DDR_CKE	K2		–	GND	E9
P28	DDR_CSO_N	L7		–	–	T7
–	1V2_DDR4	P9		–	GND	M9
–	GND	T3				
B23	DDR_RESET_N	P1				
	DDR_ADDR14	L3				
–	GND	N9				

3.6 SD-card Interfaces

3.6.1 MPU Signals for eMMC NAND Flash

MRZG2LS supports a 4GByte to 64GByte eMMC NAND Flash. The eMMC device is a bootable device.

The following table provides the connections MPU to eMMC NAND flash:

MPU Pin	Function	eMMC Pin	Remarks
G2	SD0_DATA0	A3	47k Pull-up
H4	SD0_DATA1	A4	
G3	SD0_DATA2	A5	
G4	SD0_DATA3	B2	
E1	SD0_DATA4	B3	
D1	SD0_DATA5	B4	
E2	SD0_DATA6	B5	
D12	SD0_DATA7	B6	
F2	SD0_CMD	M5	47k Pull-up
F1	SD0_CLK	M6	
C1	SD0_RST#	K5	47k Pull-up

3.6.2 MPU Signals for SD-card Interface

MRZG2LS supports a SD-card interface on the SMARC connector. The SD-card interface is **NOT** a bootable device.

The following SD-card interface signals are provided to the SMARC connector:

MPU Pin	Function	Connector P1 Pin	Remarks
H3	SD1_CLK	P36	47k Pull-up
J2	SD1_CMD	P34	47k Pull-up
H1	SD1_DATA0	P39	47k Pull-up
H2	SD1_DATA1	P40	47k Pull-up
K2	SD1_DATA2	P41	47k Pull-up
J1	SD1_DATA3	P42	47k Pull-up
B1	SD1_CD#	P35	10k Pull-up
B2	SD1_WP	P33	10k Pull-up
B16	SD1_PWREN	P37	

3.7 SPI and QSPI

3.7.1 SPI

The following SPI signals are provided to the SMARC connector:

MPU Pin	MPU Function	Connector P1 Pin
A19	SPI1_CLK	P56
F17	SPI1_MOSI	P58
D18	SPI1_MISO	P57
B19	SPI1_SSL	P54

3.7.2 QSPI

The following QSPI signals are provided to the SMARC connector:

MPU Pin	MPU Function	Comment
C7	QSPI1_IO0	n.c.
D7	QSPI1_IO1	n.c.
A6	QSPI1_IO2	n.c.
D8	QSPI1_IO3	n.c.
B7	QSPI1_SPCLK	n.c.
C8	QSPI1_SSL	n.c.
B5	QSPI1_WP#	n.c.
A5	QSPI_RESET#	10k pull-up
B6	QSPI_INT#	10k pull-up

3.7.3 QSPI NOR FLASH

MPU Signals for SPI NOR FLASH

MRZG2LS supports a 128MBit to 512MBit QSPI NOR Flash. The SPI NOR device is a bootable device.

The following table provides the connections MPU to SPI-NOR flash:

MPU Pin	MPU Function		NOR Flash Pin	NOR Flash Function
A3	QSPI0_IO0		5	IO0/DI
B3	QSPI0_IO1		2	IO1/D0
A4	QSPI0_IO2		3	IO2/WP#
B4	QSPI0_IO3		7	IO3/HOLD#
C4	QSPI0_CLK		6	CLK
A2	QSPI0_CS#		1	CS#

3.8 I2C

MPU Signals for I2C

MPU Pin	Function	Connector P1 Pin	Remarks
B24	RZ_I2C0.CLK	S1	2k20 Pull-up
A25	RZ_I2C0.DAT	S2	2k20 Pull-up
C23	RZ_I2C1.CLK	S139	2k20 Pull-up
A24	RZ_I2C1.DAT	S140	2k20 Pull-up
D3	RZ_I2C3.CLK	S48	2k20 Pull-up
C2	RZ_I2C3.DAT	S49	2k20 Pull-up

3.9 I2S

MPU Signals for I2S

MPU Pin	Function	Connector P1 Pin
	AUDIO_MCK	S38
B9	I2S0_SDIN	S41
A9	I2S0_SDOUT	S40
D12	I2S0_LRCK	S39
A8	I2S0_CK	S42
B10	I2S2_CK	S53
D13	I2S2_SDIN	S52
C12	I2S2_SDOUT	S51
A10	I2S2_LRCK	S50

3.10 Ethernet

On the MRZG2LS SoM no/one/two Ethernet PHYs type Microchip KSZ9131RNXC can be populated.

3.10.1 Ethernet 1

MPU Signals to Ethernet PHY1

MPU Pin	Function	PHY1 Pin
N1	ETH1_TXCLK	24
N2	ETH1_TX_CTL	25
M1	ETH1_TXD0	19
M2	ETH1_TXD1	20
L1	ETH1_TXD2	21
L2	ETH1_TXD3	22
P2	ETH1_RXCLK	35
P1	ETH1_RX_CTL	33
R2	ETH1_RXD0	32
R1	ETH1_RXD1	31
T2	ETH1_RXD2	28
T1	ETH1_RXD3	27
U2	ETH1_MDC	36
U1	ETH1_MDIO	37

Ethernet PHY1 to Connector P1 (314 pins Edge Connector)

PHY1 Pin	Function	Connector P1 Pin
2	TXRXP_A	P30
3	TXRXM_A	P29
	LINK100#	P21
5	TXRXP_B	P27
6	TXRXM_B	P26
	LINK1000#	P22
7	TXRXP_C	P24
8	TXRXM_C	P23
	LINK_ACT#	P25
10	TXRXP_D	P20
11	TXRXM_D	P19

3.10.2 Ethernet 2

MPU Signals to Ethernet PHY2

MPU Pin	Function	PHY2 Pin
AB2	ETH2_TXCLK	24
Y1	ETH2_TX_CTL	25
AB1	ETH2_TXD0	19
AA2	ETH2_TXD1	20
AA1	ETH2_TXD2	21
Y2	ETH2_TXD3	22
AC1	ETH2_RXCLK	35
AC2	ETH2_RX_CTL	33
AC3	ETH2_RXD0	32
AC4	ETH2_RXD1	31
AB4	ETH2_RXD2	28
AB3	ETH2_RXD3	27
W2	ETH2_MDC	36
W1	ETH2_MDIO	37

Ethernet PHY2 to Connector P1 (314 pins Edge Connector)

PHY2 Pin	Function	Connector P1 Pin
2	TXRXP_A	S17
3	TXRXM_A	S18
	LINK100#	S19
5	TXRXP_B	S20
6	TXRXM_B	S21
	LINK1000#	S22
7	TXRXP_C	S23
8	TXRXM_C	S24
	LINK_ACT#	S31
10	TXRXP_D	S26
11	TXRXM_D	S27

3.11 CAN

MPU Signals for CAN

MRZG2LS supports the 2 native CAN interfaces of the MPU as follows:

MPU Pin	Function	Connector P1 Pin
AH22	CAN0_TX	P143
AG22	CAN0_RX	P144
AE23	CAN1_TX	P145
AF23	CAN1_RX	P146

3.12 USB Interfaces

The MRZG2LS SoM supports 2 USB interfaces, USB0 and USB1.

3.12.1 Interface USB0

Interface USB0 functions as USB2.0 OTG interface.

MPU Signals for USB0

MPU Pin	Function	Connector P1 Pin
AH9	USB0.D_P	P60
AJ8	USB0.D_N	P61
AJ5	USB0.EN_OC#	P62
AH10	USB0_VBUS_DET	P63
AH4	USB0.OTG_ID	P64

3.12.2 Interface USB1

Interface USB1 functions as USB2.0 interface.

MPU Signals for USB1

MPU Pin	Function	Connector P1 Pin
AH8	USB1.D_P	P65
AJ7	USB1.D_N	P66
AH4	USB1.EN_OC#	P67

3.13 MIPI

3.13.1 MIP-CSI

The MRZG2LS supports a 4 lane wide MIPI-CSI interface:

MPU Pin	Function	Connector P1 Pin
AG13	CSI.CLK_P	P3
AG12	CSI.CLK_N	P4
AJ13	CSI.DATA0_P	P7
AH13	CSI.DATA0_N	P8
AJ12	CSI.DATA1_P	P10
AH12	CSI.DATA1_N	P11
AJ14	CSI.DATA2_P	P13
AH14	CSI.DATA2_N	P14
AJ11	CSI.DATA3_P	P16
AH11	CSI.DATA3_N	P17

3.13.2 MIP-DSI

The MRZG2LS supports a 4 lane wide MIPI-DSI interface:

MPU Pin	Function	Connector P1 Pin
AG17	DSI.CLK_P	P3
AG18	DSI.CLK_N	P4
AH16	DSI.DATA0_P	P7
AJ16	DSI.DATA0_N	P8
AH17	DSI.DATA1_P	P10
AJ17	DSI.DATA1_N	P11
AH15	DSI.DATA2_P	P13
AJ15	DSI.DATA2_N	P14
AH18	DSI.DATA3_P	P16
AJ18	DSI.DATA3_N	P17

3.14 JTAG

The JTAG signals of the CPU are routed to the fpc-connector P2, type 10051922-1010EHLF (Amphenol) and comply to the following pinout:

MPU Pin	Function	Connector/ Pin	Remarks
	VDD_JTAG	1	1.8V
AF2	TRST#	2	10k Pull-up
AD2	TMS	3	10k Pull-up
AE2	TDO	4	
AF1	TDI	5	10k Pull-up
AE1	TCK	6	10k Pull-up
A26	n.c.	7	
AF3	RESET_IN#	8	Connected to CPU Reset and PHY Reset
	n.c.	9	
	GND	10	

3.15 DIP Switch SW1 for JTAG Configuration

SW1 configures the JTAG interface as decribed below:

DIP Switch Contact	Status	Voltage	Function	MPU Pin
1-4	open	pull up 10k	DEBUGEN	AE18
	closed	GND		
2-3	open	pull up 10k	TRST#	AF2
	closed	GND		

For mass production the SW1 will not be populated but be replaced by the desired fixed pull-up/pull-down resistor configurations instead.

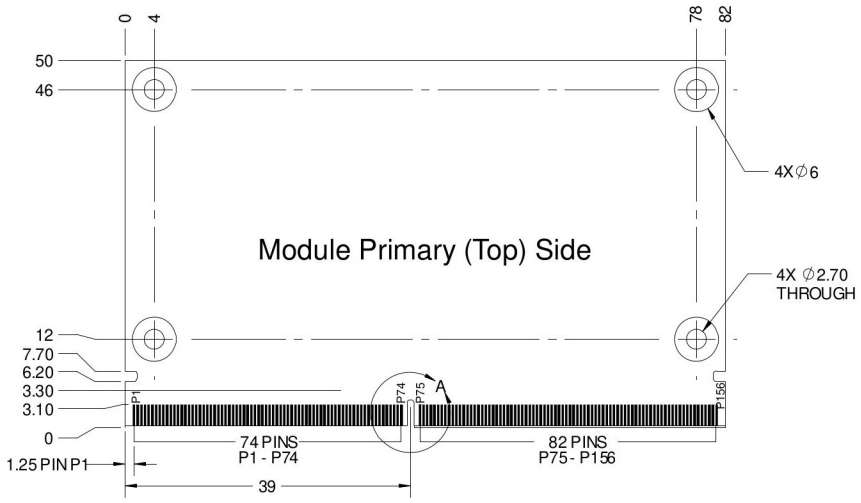
3.16 A/D-Converter (ADC)

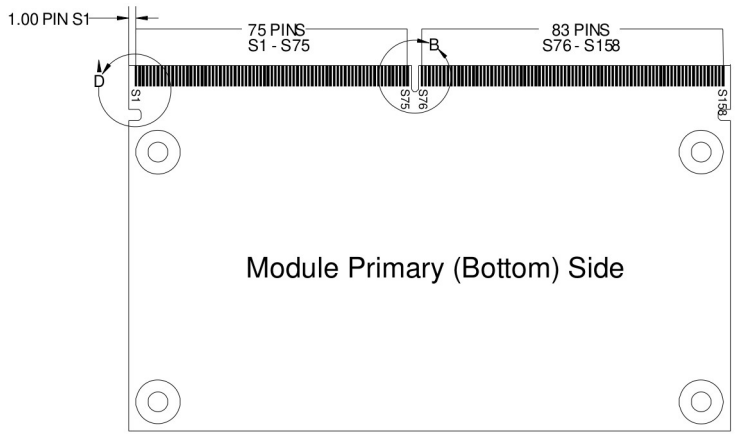
The ADC signals of the CPU are routed to the fpc-connector P3, type 10051922-1010EHLF (Amphenol) and comply to the following pinout:

MPU Pin	Function	Connector P3/ Pin	Remarks
A28	ADC_CH0	3	47k Pull-down, optional, not populated
B27	ADC_CH1	7	47k Pull-down, optional, not populated
B28	ADC_CH2	4	47k Pull-down, optional, not populated
A27	ADC_CH3	5	47k Pull-down, optional, not populated
C26	ADC_CH4	9	47k Pull-down, optional, not populated
B26	ADC_CH5	8	47k Pull-down, optional, not populated
A26	ADC_CH6	–	GND
B25	ADC_CH7	–	GND

3.17 P1 - 314 Pins Edge Connector

3.17.1 Pin Numbering





3.17.2 Top Side

Connector/Pin	Function	Device/ Pin	Remarks
P1	SMB_ALERT#		n.c.
P2	GND		
P3	CSI1_CK+	MPU AG13	
P4	CSI1_CK-	MPU AG12	
P5	GBE1_SDP		n.c.
P6	GBE0_SDP		n.c.
P7	CSI1_RX0+	MPU AJ13	
P8	CSI1_RX0-	MPU AH13	
P9	GND		
P10	CSI1_RX1+	MPU AJ12	
P11	CSI1_RX1-	MPU AH12	
P12	GND		
P13	CSI1_RX2+	MPU AJ14	
P14	CSI1_RX2-	MPU AH14	
P15	GND		
P16	CSI1_RX3+	MPU AJ11	
P17	CSI1_RX3-	MPU AH11	
P18	GND		
P19	GBE0_MDI3-	PHY1 11	
P20	GBE0_MDI3+	PHY1 10	
P21	GBE0_LINK100#	PHY1 15	
P22	GBE0_LINK1000#	PHY1 15	
P23	GBE0_MDI2-	PHY1 8	
P24	GBE0_MDI2+	PHY1 7	
P25	GBE0_LINK_ACT#	PHY1 17	
P26	GBE0_MDI1-	PHY1 6	
P27	GBE0_MDI1+	PHY1 5	
P28	GBE0_CTREF		n.c.
P29	GBE0_MDI0-	PHY1 3	
P30	GBE0_MDI0+	PHY1 2	
P31	SPI0_CS1#		n.c.
P32	GND		
P33	SDIO_WP	MPU B2	10k pull up
P34	SDIO_CMD	MPU J2	47k pull up
P35	SDIO_CD#	MPU B1	10k pull up
P36	SDIO_CK	MPU H3	47k pull up
P37	SDIO_PWR_EN	MPU B16	
P38	GND		
P39	SDIO_D0	MPU H1	47k pull up
P40	SDIO_D1	MPU H2	47k pull up
P41	SDIO_D2	MPU K2	47k pull up
P42	SDIO_D3	MPU J1	47k pull up
P43	SPI0_CS0#		n.c.
P44	SPI0_CK		n.c.
P45	SPI0_DIN		n.c.
P46	SPI0_DO		n.c.
P47	GND		

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Table 2 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
P48	SATA_TX+		n.c.
P49	SATA_TX-		n.c.
P50	GND		
P51	SATA_RX+		n.c.
P52	SATA_RX-		n.c.
P53	GND		
P54	SPI1_CS0#	MPU B19	
P55	SPI1_CS1#		n.c.
P56	SPI1_CK	MPU A19	
P57	SPI1_DIN	MPU D18	
P58	SPI1_DO	MPU F17	
P59	GND		
P60	USB0+	MPU AH9	
P61	USB0-	MPU AJ8	
P62	USB0_EN_OC#	MPU AJ5	
P63	USB0_VBUS_DET	MPU AH10	
P64	USB0_OTG_ID	MPU AH4	
P65	USB1+	MPU AH8	
P66	USB1-	MPU AJ8	
P67	USB1_EN_OC#	MPU AH4	
P68	GND		
P69	USB2+		n.c.
P70	USB2-		n.c.
P71	USB2_EN_OC#		n.c.
P72	RSVD		n.c.
P73	RSVD		n.c.
P74	USB3_EN_OC#		n.c.
P75	PCIE_A_RST#		n.c.
P76	USB4_EN_OC#		n.c.
P77	PCIE_B_CKREQ#		n.c.
P78	PCIE_A_CKREQ#		n.c.
P79	GND		
P80	PCIE_C_REFCK+		n.c.
P81	PCIE_C_REFCK-		n.c.
P82	GND		
P83	PCIE_A_REFCK+		n.c.
P84	PCIE_A_REFCK-		n.c.
P85	GND		
P86	PCIE_A_RX+		n.c.
P87	PCIE_A_RX-		n.c.
P88	GND		
P89	PCIE_A_TX+		n.c.
P90	PCIE_A_TX-		n.c.
P91	GND		
P92	HDMI_D2+		n.c.
P93	HDMI_D2-		n.c.
P94	GND		
P95	HDMI_D1+		n.c.
P96	HDMI_D1-		n.c.

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Table 2 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
P97	GND		
P98	HDMI_D0+		n.c.
P99	HDMI_D0-		n.c.
P100	GND		
P101	HDMI_CK+		n.c.
P102	HDMI_CK-		n.c.
P103	GND		
P104	HDMI_HPD		n.c.
P105	HDMI_CTRL_CK		n.c.
P106	HDMI_CRL_DAT		n.c.
P107	DP1_AUX_SEL		n.c.
P108	GPIO0	MPU A14	
P109	GPIO1	MPU B13	
P110	GPIO2	MPU A13	
P111	GPIO3	MPU A17	
P112	GPIO4	MPU B18	
P113	GPIO5	MPU E18	
P114	GPIO6	MPU E17	
P115	GPIO7	MPU D17	
P116	GPIO8	MPU AJ3	
P117	GPIO9	MPU AH3	
P118	GPIO10	MPU B14	
P119	GPIO11	MPU AH5	
P120	GND		
P121	I2C_PM_CK		n.c.
P122	I2C_PM_DAT		n.c.
P123	BOOT_SEL.0#		boot mode configuration
P124	BOOT_SEL.1#		boot mode configuration
P125	BOOT_SEL.2#		boot mode configuration
P126	RESET_OUT#	MPU AF3 PMIC pin 54 PHY pin 42 P2 pin8	
P127	RESET_IN#	PMIC pin 45	
P128	POWER_BTN#	PMIC pin 52	
P129	SER0_TX	MPU B22	
P130	SER0_RX	MPU A23	
P131	SER0_RTS#	MPU B23	
P132	SER0_CTS#	MPU C22	
P133	GND		
P134	SER1_TX	MPU C17	
P135	SER1_RX	MPU B17	
P136	SER2_TX		n.c.
P137	SER2_RX		n.c.
P138	SER2_RTS#		n.c.
P139	SER2_CTS#		n.c.
P140	SER3TX	MPU A15	
P141	SER3_RX	MPU B15	
P142	GND		

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Table 2 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
P143	CAN0_TX	MPU AH22	
P144	CAN0_RX	MPU AG22	
P145	CAN1_TX	MPU AE23	
P146	CAN1_RX	MPU AF23	
P147	VDD_IN		
P148	VDD_IN		
P149	VDD_IN		
P150	VDD_IN		
P151	VDD_IN		
P152	VDD_IN		
P153	VDD_IN		
P154	VDD_IN		
P155	VDD_IN		
P156	VDD_IN		

3.17.3 Bottom Side

Connector/Pin	Function	Device/ Pin	Remarks
S1	I2C_CAM1_CK	MPU B24	
S2	I2C_CAM1_DAT	MPU A25	
S3	GND		
S4	RSVD		n.c.
S5	I2C_CAM0_CK		n.c.
S6	CAM_MCK		n.c.
S7	I2C_CAM_DAT		n.c.
S8	CSI0_CK+		n.c.
S9	CSI0_CK-		n.c.
S10	GND		
S11	CSI0_RX0+		n.c.
S12	CSI0_RX0-		n.c.
S13	GND		
S14	CSI0_RX1+		n.c.
S15	CSI0_RX1-		n.c.
S16	GND		
S17	GBE1_MDIO+	PHY2 2	
S18	GBE1_MDIO-	PHY2 3	
S19	GBE1_LINK100#	PHY2 15	
S20	GBE1_MDI1+	PHY2 5	
S21	GBE1_MDI1-	PHY2 6	
S22	GBE1_LINK1000#	PHY2 15	
S23	GBE1_MDI2+	PHY2 7	
S24	GBE1_MDI2-	PHY2 8	
S25	GND		
S26	GBE1_MDI3+	PHY2 10	
S27	GBE1_MDI3-	PHY2 11	
S28	GBE1_CTREF		n.c.
S29	PCIE_D_TX+		n.c.
S30	PCIE_D_TX-		n.c.
S31	GBE1_LINK_ACT#		n.c.
S32	PCIE_D_RX+		n.c.
S33	PCIE_D_RX-		n.c.
S34	GND		
S35	USB4+		n.c.
S36	USB4-		n.c.
S37	USB3_VBUS_DET		n.c.
S38	AUDIO_MCK	Clock Chip pin 12	
S39	I2S0_LRCK	MPU D12	
S40	I2S0_SDOUT	MPU A9	
S41	I2S0_SDIN	MPU B9	
S42	I2S0_CK	MPU A8	
S43	ESPI_ALERT0#		n.c.
S44	ESPI_ALERT1#		n.c.
S45	MDIO_CLK		n.c.
S46	MDIO_DAT		n.c.
S47	GND		

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Table 3 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
S48	I2C_GP_CK	MPU D3	
S49	I2C_GP_DAT	MPU C2	
S50	I2S2_LRCK	MPU A10	
S51	I2S2_SDOUT	MPU C12	
S52	I2S2_SDIN	MPU D13	
S53	I2S2_CK	MPU B10	
S54	SATA_ACT#		n.c.
S55	USB5_EN_OC#		n.c.
S56	QSPI_IO_2		n.c.
S57	QSPI_IO_3		n.c.
S58	ESPI_RESET#		n.c.
S59	USB5+		n.c.
S60	USB5-		n.c.
S61	GND		
S62	USB3_SSTX+		n.c.
S63	USB3_SSTX-		n.c.
S64	GND		
S65	USB3_SSRX+		n.c.
S66	USB3_SSRX-		n.c.
S67	GND		
S68	USB3+		n.c.
S69	USB3-		n.c.
S70	GND		
S71	USB2_SSTX+		n.c.
S72	USB2_SSTX-		n.c.
S73	GND		
S74	USB2_SSRX+		n.c.
S75	USB2_SSRX-		n.c.
S76	PCIE_B_RST#		n.c.
S77	PCIE_C_RST#		n.c.
S78	PCIE_C_RX+		n.c.
S79	PCIE_C_RX-		n.c.
S80	GND		
S81	PCIE_C_TX+		n.c.
S82	PCIE_C_TX-		n.c.
S83	GND		
S84	PCIE_B_REFCK+		n.c.
S85	PCIE_B_REFCK-		n.c.
S86	GND		
S87	PCIE_B_RX+		n.c.
S88	PCIE_B_RX-		n.c.
S89	GND		
S90	PCIE_B_TX+		n.c.
S91	PCIE_B_TX-		n.c.
S92	GND		
S93	HDMI_D2-		n.c.
S94	DP0_LANE0-		n.c.
S95	HDMI_D1+		n.c.
S96	HDMI_D1-		n.c.

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Table 3 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
S97	DP0_LANE1-		n.c.
S98	HDMI_D0+		n.c.
S99	HDMI_D0-		n.c.
S100	DP0_LANE2-		n.c.
S101	GND		
S102	HDMI_CK-		n.c.
S103	DP0_LANE3-		n.c.
S104	HDMI_HPD		n.c.
S105	HDMI_CTRL_CK		n.c.
S106	HDMI_CTRL_DA		n.c.
S107	LCD1_BKLT_EN		n.c.
S108	LVDS1_CK+		n.c.
S109	LVDS1_CK-		n.c.
S110	GND		
S111	LVDS1_0+		n.c.
S112	LVDS1_0-		n.c.
S113	eDP1_HPD		n.c.
S114	LVDS1_1+		n.c.
S115	LVDS1_1-		n.c.
S116	LCD1_VDD_EN		n.c.
S117	LVDS1_2+		n.c.
S118	LVDS1_2-		n.c.
S119	GND		
S120	LVDS1_3+		n.c.
S121	LVDS1_3-		n.c.
S122	LCD1_BKLT_PWM		n.c.
S123	GPIO13	MPU A21	
S124	GND		
S125	DSI0_D0+	MPU AH16	
S126	DSI0_D0-	MPU AJ16	
S127	LCD0_BKLT_EN		n.c.
S128	DSI0_D1+	MPU AH17	
S129	DSI0_D1-	MPU AJ17	
S130	GND		
S131	DSI0_D2+	MPU AH15	
S132	DSI0_D2-	MPU AJ15	
S133	LCD0_VDD_EN		n.c.
S134	DSI0_CLK+	MPU AG17	
S135	DSI0_CLK-	MPU AG18	
S136	GND		
S137	DSI0_D3+	MPU AH18	
S138	DSI0_D3-	MPU AJ18	
S139	I2C_LCD_CK	MPU C23	
S140	I2C_LCD_DAT	MPU A24	
S141	LCD0_BKLT_PWM		n.c.
S142	GPIO12	MPU AJ3	
S143	GND		
S144	eDP0_HPD		n.c.
S145	WDT_TIME_OUT#		n.c.

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Table 3 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
S146	PCIE_WAKE#		n.c.
S147	VDD_RTC		
S148	LID#		n.c.
S149	SLEEP#		n.c.
S150	VIN_PWR_BAD#	PMIC 47	
S151	CHARGING#		n.c.
S152	CHARGER_PRSNT#		n.c.
S153	CARRIER_STBY#	PMIC 56	
S154	CARRIER_PWR_ON		
S155	FORCE_RECOV#		n.c.
S156	BATLOW#		n.c.
S157	TEST#		n.c.
S158	GND		

3.18 Schematics

Schematics for the MRZG2LS and MRZV2LS may be obtained on request. Please contact sales@aries-embedded.de for more information.