MRZG2LSEVK Hardware Manual

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Created by: ARIES Embedded GmbH

CONTENTS:

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

Adress:

ARIES Embedded GmbH

Schöngeisinger Str. 84

D-82256 Fürstenfedbruck

Germany

Phone:

+49 (0) 8141/36 367-0

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	24.01.2024	aw	Initial creation

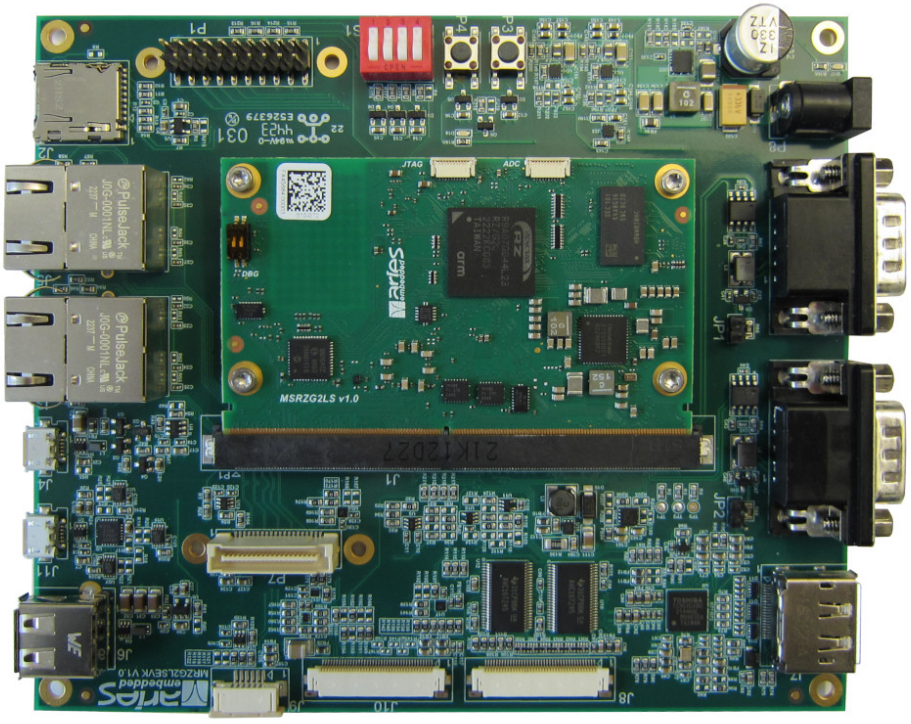
CHAPTER

TWO

OVERVIEW

2.1 MRZG2LSEVK - Evaluation Kit for MRZG2LS

The MRZG2LSEVK baseboard supports a quick start-up of new projects, using the MRZG2LS or MRZV2LS SMARC SoMs by ARIES Embedded. The baseboard can be used for getting in touch and first experience with the new CPU architecture, can be used as a reference platform to develop and try out software as well as it can be used to easily implement prototype setups.



2.2 Feature Set

- **MRZG2LS System on Module**
  - Single or Dual Cortex-A55, up to 1.2GHz
  - 512MB – 4GB DDR4 RAM
  - SPI NOR
  - 4GB-64GB eMMC NAND Flash
  - compliant to the SGET SMARC 2.1 standard
- **or MRZV2LS System on Module**
  - Single or Dual Cortex-A55, up to 1.2GHz
  - AI accelerator; DRP-A
  - 512MB – 4GB DDR4 RAM
  - SPI NOR
  - 4GB-64GB eMMC NAND Flash
  - compliant to the SGET SMARC 2.1 standard
- 2x Ethernet on RJ45
- 2x CAN on DSub9
- MIPI-DSI via converter on Display Port connector
- MIPI-CSI on connector
- USB2.0 OTG on USB micro AB
- USB2.0 Host on USB A
- console via converter on USB micro AB
- UART, I2C, SPI on pin header
- SD-card on µSD-card slot
- 0°C..+70°C commercial temperature range
- -40°C..+85°C industrial temperature range

2.3 Order Codes

The MRZG2LSEVK is available in the following standard configurations:

MRZG2LSEVK-AAB

- **MRZG2LS-AAB SoM featuring**
  - Renesas RZ/G2L R9A07G044L23GBG#BC0
  - 1GB DDR4 RAM
  - 4GB eMMC
  - 128MBit SPI-NOR
  - 2x KSZ9131 PHY 10/100/1000MBit
  - -25°...+85°C
- MRZG2LSEVK baseboard
- power supply

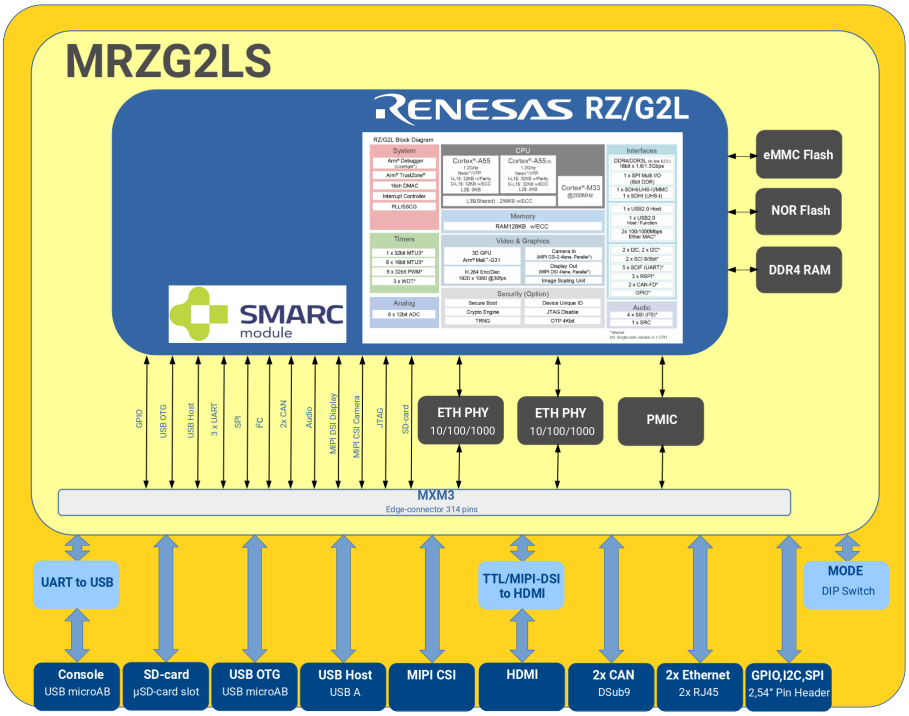
MRZV2LSEVK-AAB

- **MRZV2LS-AAB SoM featuring**
  - Renesas RZ/V2L R9A07G054L23GBG#BC0
  - 1GB DDR4 RAM
  - 4GB eMMC
  - 128MBit SPI-NOR
  - 2x KSZ9131 PHY PHY 10/100/1000MBit
  - -25°...+85°C
- MRZG2LSEVK baseboard
- power supply

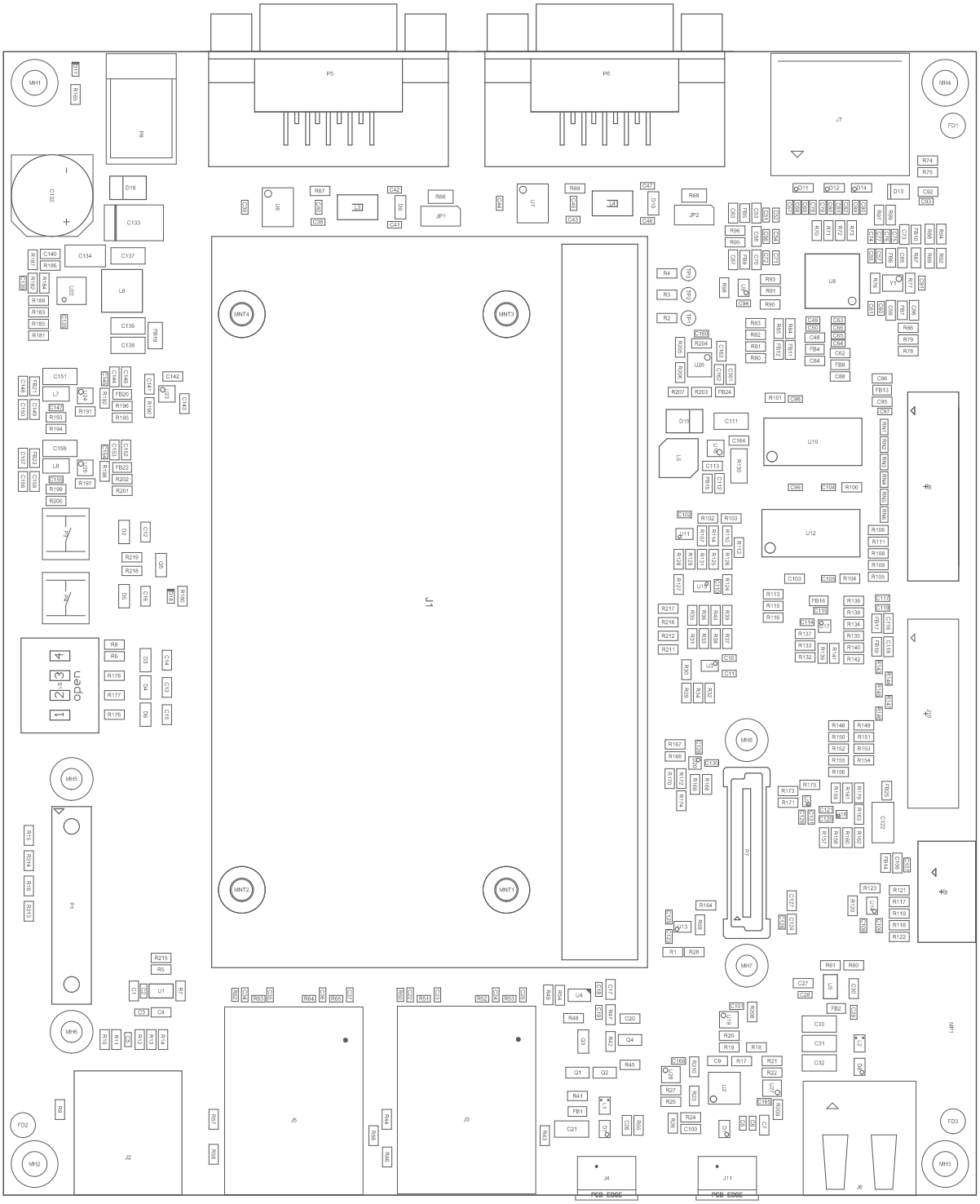
Please contact ARIES Embedded under email sales@aries-embedded.de for more information about the availability of other standard products or custom configurations.

2.4 Block Diagram

The following block diagram shows the MRZG2LSEVK with a mounted MRZG2LS SoM.



2.5 Part Overview



A more detailed and searchable document on the parts overview can be made available on request under email sales@aries-embedded.de.

2.6 Handling Recommendations

To avoid mechanical damage to the components populated on MRZG2LS and MRZG2LSEVK it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components.

CHAPTER

THREE

RESOURCES

3.1 Connector J1 - 314 Pins Edge Connector

3.1.1 Connector Part Number

The MRZG2LSEVK is equipped with a 314 pins edge connector. The following connector is used on the MRZG2LSEVK and can be delivered by ARIES Embedded in mass production quantities:

Part-Number	Manufacturer	Board-to-Board Distance	Plating	Package Unit
91781-31428-001	ACES	2,7mm	30µ" gold	400 pcs/reel

Please request the full connector specification or request a quote for the connector via email to sales@aries-eembedded.de.

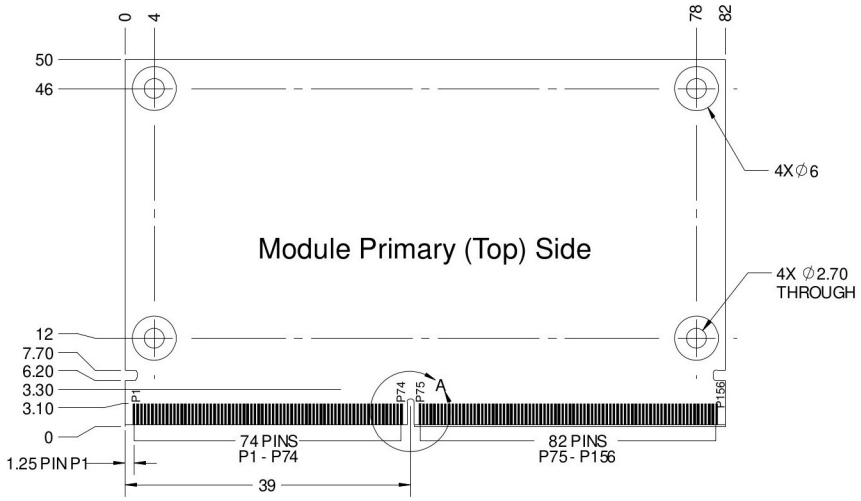
3.1.2 Standoffs

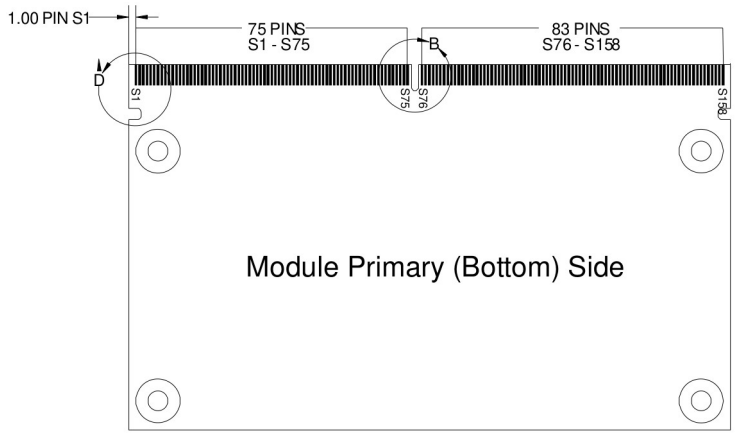
To keep the MRZG2LS SoM board mechanically fixed on the MRZG2LSEVK baseboard it will be plugged in to connector J1 and fixed with screws onto standoffs that are soldered to the baseboard. The recommended standoff provides the following features:

Part-Number	Manufacturer	Board-to-Board Distance	Thread Size	Package Unit
9774027151R	Würth Elektronik	2,7mm	M2.5	450 pcs/reel

Please request the full standoff specification or request a quote for the connector via email to sales@aries-eembedded.de.

3.1.3 Pin Numbering





3.1.4 Pin Out

The following pin out table shows the connections on the MRZG2LS or MRZV2LS CPU SoM that is inserted into connector J1.

3.1.4.1 Top Side

Connector/Pin	Function	Device/ Pin	Remarks
P1	SMB_ALERT#		n.c.
P2	GND		
P3	CSI1_CK+	MPU AG13	
P4	CSI1_CK-	MPU AG12	
P5	GBE1_SDP		n.c.
P6	GBE0_SDP		n.c.
P7	CSI1_RX0+	MPU AJ13	
P8	CSI1_RX0-	MPU AH13	
P9	GND		
P10	CSI1_RX1+	MPU AJ12	
P11	CSI1_RX1-	MPU AH12	
P12	GND		
P13	CSI1_RX2+	MPU AJ14	
P14	CSI1_RX2-	MPU AH14	
P15	GND		
P16	CSI1_RX3+	MPU AJ11	
P17	CSI1_RX3-	MPU AH11	
P18	GND		
P19	GBE0_MDI3-	PHY1 11	
P20	GBE0_MDI3+	PHY1 10	
P21	GBE0_LINK100#	PHY1 15	
P22	GBE0_LINK1000#	PHY1 15	
P23	GBE0_MDI2-	PHY1 8	
P24	GBE0_MDI2+	PHY1 7	
P25	GBE0_LINK_ACT#	PHY1 17	
P26	GBE0_MDI1-	PHY1 6	
P27	GBE0_MDI1+	PHY1 5	
P28	GBE0_CTREF		n.c.
P29	GBE0_MDI0-	PHY1 3	
P30	GBE0_MDI0+	PHY1 2	
P31	SPI0_CS1#		n.c.
P32	GND		
P33	SDIO_WP	MPU B2	10k pull up
P34	SDIO_CMD	MPU J2	47k pull up
P35	SDIO_CD#	MPU B1	10k pull up
P36	SDIO_CK	MPU H3	47k pull up
P37	SDIO_PWR_EN	MPU B16	
P38	GND		
P39	SDIO_D0	MPU H1	47k pull up
P40	SDIO_D1	MPU H2	47k pull up
P41	SDIO_D2	MPU K2	47k pull up
P42	SDIO_D3	MPU J1	47k pull up

continues on next page

Table 1 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
P43	SPI0_CS0#		n.c.
P44	SPI0_CK		n.c.
P45	SPI0_DIN		n.c.
P46	SPI0_DO		n.c.
P47	GND		
P48	SATA_TX+		n.c.
P49	SATA_TX-		n.c.
P50	GND		
P51	SATA_RX+		n.c.
P52	SATA_RX-		n.c.
P53	GND		
P54	SPI1_CS0#	MPU B19	
P55	SPI1_CS1#		n.c.
P56	SPI1_CK	MPU A19	
P57	SPI1_DIN	MPU D18	
P58	SPI1_DO	MPU F17	
P59	GND		
P60	USB0+	MPU AH9	
P61	USB0-	MPU AJ8	
P62	USB0_EN_OC#	MPU AJ5	
P63	USB0_VBUS_DET	MPU AH10	
P64	USB0_OTG_ID	MPU AH4	
P65	USB1+	MPU AH8	
P66	USB1-	MPU AJ8	
P67	USB1_EN_OC#	MPU AH4	
P68	GND		
P69	USB2+		n.c.
P70	USB2-		n.c.
P71	USB2_EN_OC#		n.c.
P72	RSVD		n.c.
P73	RSVD		n.c.
P74	USB3_EN_OC#		n.c.
P75	PCIE_A_RST#		n.c.
P76	USB4_EN_OC#		n.c.
P77	PCIE_B_CKREQ#		n.c.
P78	PCIE_A_CKREQ#		n.c.
P79	GND		
P80	PCIE_C_REFCK+		n.c.
P81	PCIE_C_REFCK-		n.c.
P82	GND		
P83	PCIE_A_REFCK+		n.c.
P84	PCIE_A_REFCK-		n.c.
P85	GND		
P86	PCIE_A_RX+		n.c.
P87	PCIE_A_RX-		n.c.
P88	GND		
P89	PCIE_A_TX+		n.c.
P90	PCIE_A_TX-		n.c.
P91	GND		

continues on next page

Table 1 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
P92	HDMI_D2+		n.c.
P93	HDMI_D2-		n.c.
P94	GND		
P95	HDMI_D1+		n.c.
P96	HDMI_D1-		n.c.
P97	GND		
P98	HDMI_D0+		n.c.
P99	HDMI_D0-		n.c.
P100	GND		
P101	HDMI_CK+		n.c.
P102	HDMI_CK-		n.c.
P103	GND		
P104	HDMI_HPD		n.c.
P105	HDMI_CTRL_CK		n.c.
P106	HDMI_CRL_DAT		n.c.
P107	DP1_AUX_SEL		n.c.
P108	GPIO0	MPU A14	
P109	GPIO1	MPU B13	
P110	GPIO2	MPU A13	
P111	GPIO3	MPU A17	
P112	GPIO4	MPU B18	
P113	GPIO5	MPU E18	
P114	GPIO6	MPU E17	
P115	GPIO7	MPU D17	
P116	GPIO8	MPU AJ3	
P117	GPIO9	MPU AH3	
P118	GPIO10	MPU B14	
P119	GPIO11	MPU AH5	
P120	GND		
P121	I2C_PM_CK		n.c.
P122	I2C_PM_DAT		n.c.
P123	BOOT_SEL.0#		boot mode configuration
P124	BOOT_SEL.1#		boot mode configuration
P125	BOOT_SEL.2#		boot mode configuration
P126	RESET_OUT#	MPU AF3 PMIC pin 54 PHY pin 42 P2 pin8	
P127	RESET_IN#	PMIC pin 45	
P128	POWER_BTN#	PMIC pin 52	
P129	SER0_TX	MPU B22	
P130	SER0_RX	MPU A23	
P131	SER0_RTS#	MPU B23	
P132	SER0_CTS#	MPU C22	
P133	GND		
P134	SER1_TX	MPU C17	
P135	SER1_RX	MPU B17	
P136	SER2_TX		n.c.
P137	SER2_RX		n.c.

continues on next page

Table 1 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
P138	SER2_RTS#		n.c.
P139	SER2_CTS#		n.c.
P140	SER3TX	MPU A15	
P141	SER3_RX	MPU B15	
P142	GND		
P143	CAN0_TX	MPU AH22	
P144	CAN0_RX	MPU AG22	
P145	CAN1_TX	MPU AE23	
P146	CAN1_RX	MPU AF23	
P147	VDD_IN		
P148	VDD_IN		
P149	VDD_IN		
P150	VDD_IN		
P151	VDD_IN		
P152	VDD_IN		
P153	VDD_IN		
P154	VDD_IN		
P155	VDD_IN		
P156	VDD_IN		

3.1.4.2 Bottom Side

Connector/Pin	Function	Device/ Pin	Remarks
S1	I2C_CAM1_CK	MPU B24	
S2	I2C_CAM1_DAT	MPU A25	
S3	GND		
S4	RSVD		n.c.
S5	I2C_CAM0_CK		n.c.
S6	CAM_MCK		n.c.
S7	I2C_CAM_DAT		n.c.
S8	CSI0_CK+		n.c.
S9	CSI0_CK-		n.c.
S10	GND		
S11	CSI0_RX0+		n.c.
S12	CSI0_RX0-		n.c.
S13	GND		
S14	CSI0_RX1+		n.c.
S15	CSI0_RX1-		n.c.
S16	GND		
S17	GBE1_MDIO+	PHY2 2	
S18	GBE1_MDIO-	PHY2 3	
S19	GBE1_LINK100#	PHY2 15	
S20	GBE1_MDI1+	PHY2 5	
S21	GBE1_MDI1-	PHY2 6	
S22	GBE1_LINK1000#	PHY2 15	
S23	GBE1_MDI2+	PHY2 7	
S24	GBE1_MDI2-	PHY2 8	
S25	GND		
S26	GBE1_MDI3+	PHY2 10	
S27	GBE1_MDI3-	PHY2 11	
S28	GBE1_CTREF		n.c.
S29	PCIE_D_TX+		n.c.
S30	PCIE_D_TX-		n.c.
S31	GBE1_LINK_ACT#		n.c.
S32	PCIE_D_RX+		n.c.
S33	PCIE_D_RX-		n.c.
S34	GND		
S35	USB4+		n.c.
S36	USB4-		n.c.
S37	USB3_VBUS_DET		n.c.
S38	AUDIO_MCK	Clock Chip pin 12	
S39	I2S0_LRCK	MPU D12	
S40	I2S0_SDOUT	MPU A9	
S41	I2S0_SDIN	MPU B9	
S42	I2S0_CK	MPU A8	
S43	ESPI_ALERT0#		n.c.
S44	ESPI_ALERT1#		n.c.
S45	MDIO_CLK		n.c.
S46	MDIO_DAT		n.c.
S47	GND		

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Table 2 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
S48	I2C_GP_CK	MPU D3	
S49	I2C_GP_DAT	MPU C2	
S50	I2S2_LRCK	MPU A10	
S51	I2S2_SDOUT	MPU C12	
S52	I2S2_SDIN	MPU D13	
S53	I2S2_CK	MPU B10	
S54	SATA_ACT#		n.c.
S55	USB5_EN_OC#		n.c.
S56	QSPI_IO_2		n.c.
S57	QSPI_IO_3		n.c.
S58	ESPI_RESET#		n.c.
S59	USB5+		n.c.
S60	USB5-		n.c.
S61	GND		
S62	USB3_SSTX+		n.c.
S63	USB3_SSTX-		n.c.
S64	GND		
S65	USB3_SSRX+		n.c.
S66	USB3_SSRX-		n.c.
S67	GND		
S68	USB3+		n.c.
S69	USB3-		n.c.
S70	GND		
S71	USB2_SSTX+		n.c.
S72	USB2_SSTX-		n.c.
S73	GND		
S74	USB2_SSRX+		n.c.
S75	USB2_SSRX-		n.c.
S76	PCIE_B_RST#		n.c.
S77	PCIE_C_RST#		n.c.
S78	PCIE_C_RX+		n.c.
S79	PCIE_C_RX-		n.c.
S80	GND		
S81	PCIE_C_TX+		n.c.
S82	PCIE_C_TX-		n.c.
S83	GND		
S84	PCIE_B_REFCK+		n.c.
S85	PCIE_B_REFCK-		n.c.
S86	GND		
S87	PCIE_B_RX+		n.c.
S88	PCIE_B_RX-		n.c.
S89	GND		
S90	PCIE_B_TX+		n.c.
S91	PCIE_B_TX-		n.c.
S92	GND		
S93	HDMI_D2-		n.c.
S94	DP0_LANE0-		n.c.
S95	HDMI_D1+		n.c.
S96	HDMI_D1-		n.c.

continues on next page

Table 2 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
S97	DP0_LANE1-		n.c.
S98	HDMI_D0+		n.c.
S99	HDMI_D0-		n.c.
S100	DP0_LANE2-		n.c.
S101	GND		
S102	HDMI_CK-		n.c.
S103	DP0_LANE3-		n.c.
S104	HDMI_HPD		n.c.
S105	HDMI_CTRL_CK		n.c.
S106	HDMI_CTRL_DA		n.c.
S107	LCD1_BKLT_EN		n.c.
S108	LVDS1_CK+		n.c.
S109	LVDS1_CK-		n.c.
S110	GND		
S111	LVDS1_0+		n.c.
S112	LVDS1_0-		n.c.
S113	eDP1_HPD		n.c.
S114	LVDS1_1+		n.c.
S115	LVDS1_1-		n.c.
S116	LCD1_VDD_EN		n.c.
S117	LVDS1_2+		n.c.
S118	LVDS1_2-		n.c.
S119	GND		
S120	LVDS1_3+		n.c.
S121	LVDS1_3-		n.c.
S122	LCD1_BKLT_PWM		n.c.
S123	GPIO13	MPU A21	
S124	GND		
S125	DSI0_D0+	MPU AH16	
S126	DSI0_D0-	MPU AJ16	
S127	LCD0_BKLT_EN		n.c.
S128	DSI0_D1+	MPU AH17	
S129	DSI0_D1-	MPU AJ17	
S130	GND		
S131	DSI0_D2+	MPU AH15	
S132	DSI0_D2-	MPU AJ15	
S133	LCD0_VDD_EN		n.c.
S134	DSI0_CLK+	MPU AG17	
S135	DSI0_CLK-	MPU AG18	
S136	GND		
S137	DSI0_D3+	MPU AH18	
S138	DSI0_D3-	MPU AJ18	
S139	I2C_LCD_CK	MPU C23	
S140	I2C_LCD_DAT	MPU A24	
S141	LCD0_BKLT_PWM		n.c.
S142	GPIO12	MPU AJ3	
S143	GND		
S144	eDP0_HPD		n.c.
S145	WDT_TIME_OUT#		n.c.

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Table 2 – continued from previous page

Connector/Pin	Function	Device/ Pin	Remarks
S146	PCIE_WAKE#		n.c.
S147	VDD_RTC		
S148	LID#		n.c.
S149	SLEEP#		n.c.
S150	VIN_PWR_BAD#	PMIC 47	
S151	CHARGING#		n.c.
S152	CHARGER_PRSNT#		n.c.
S153	CARRIER_STBY#	PMIC 56	
S154	CARRIER_PWR_ON		
S155	FORCE_RECOV#		n.c.
S156	BATLOW#		n.c.
S157	TEST#		n.c.
S158	GND		

3.2 Ethernet

Both Ethernet channels of the RZ/G2L CPU are routed to an Ethernet PHY, accordingly. The PHY signals are avilable on RJ45 connectors.

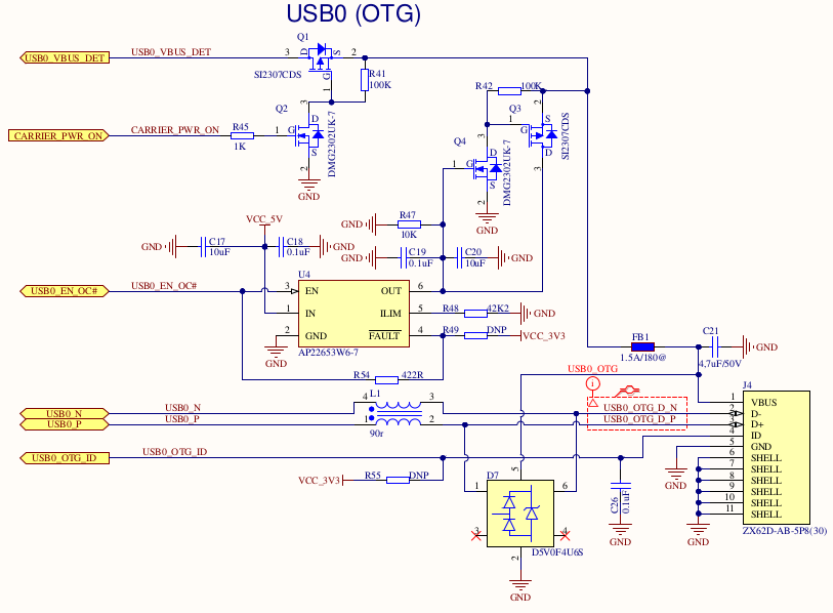
Ethernet0 is available on connector J3.

Ethernet1 is available on connector J5.

3.3 USB

3.3.1 USB0 (OTG)

The USB0 interface is available as USB2.0 OTG interface on connector J4 and connected to the following curcuitry:

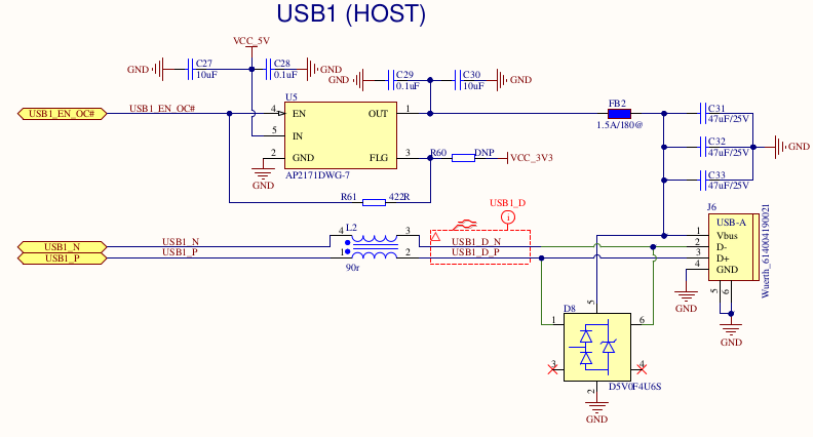


The USB0 interface makes use of the following signals:

Signal	J1 Pin
USB0_VBUS_DET	P63
USB0_EN_OC#	P62
USB0_N	P61
USB0_P	P60
USB0_OTG_ID	P64
CARRIER_PWR_ON	S154

3.3.2 USB1 (Host)

The USB1 interface is available as USB2.0 host interface on connector J6 and connected to the following curcuitry:

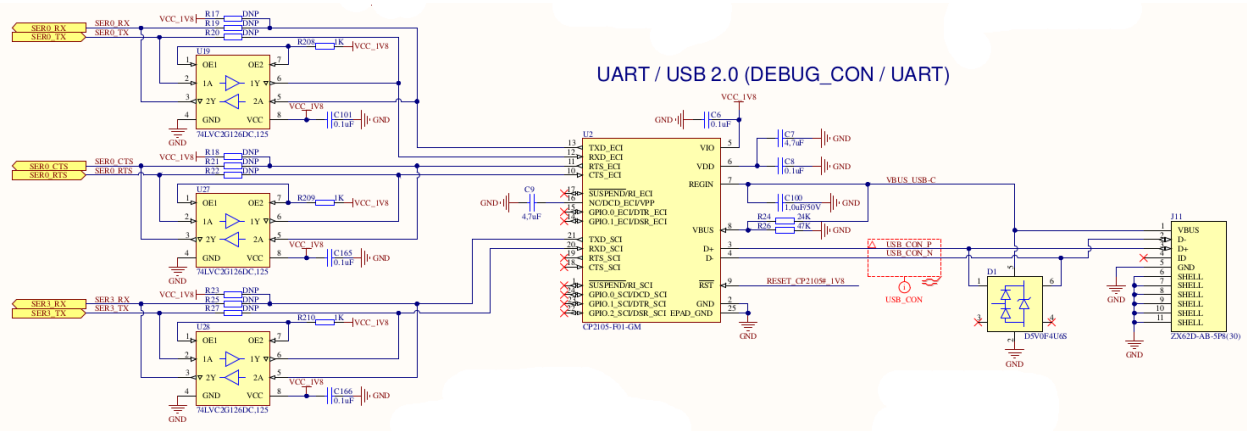


The USB0 interface makes use of the following signals:

Signal	J1 Pin
USB1_EN_OC#	P67
USB1_N	P66
USB1_P	P65

3.4 UART

UART0 and UART3 of the MRZG2LS are routed to a CP2105 device. UART3 acts as debug UART while UART0 is connected with RTS/CTS signals.

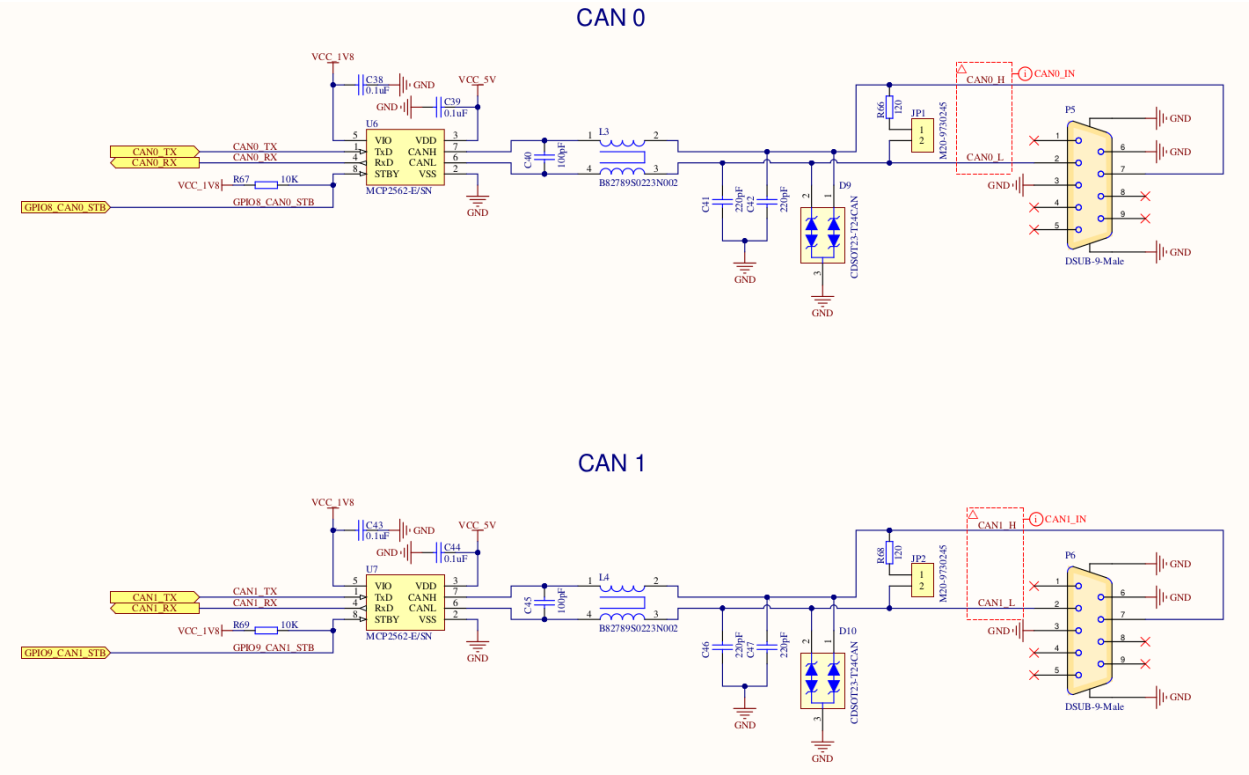


3.5 JTAG

The JTAG interface of the MRZG2LS is available on a FPC-connector on the SoM itself and not routed to the baseboard, accordingly. For more information please refer to the MRZG2LS hardware manual.

3.6 CAN

The CAN0 and CAN1 interfaces of are available on DUB9 connectors P5 and P6.



The CPU signals are connected to a MCP2562-E CAN transceiver and can optionally be terminated with an impedance of 60Ohms. The signals are connected as follows:

3.6.1 CAN0

SoM Signal	MCP2562-E signal	P5 Pin	Remark
CAN0_TX P143	1	n.c.	
n.c.	2	n.c.	GND
n.c.	3	n.c.	5V
CAN0_RX P144	4	n.c.	
n.c.	5	n.c.	1.8V
n.c.	6	CANL	
n.c.	7	CANH	
GPIO8_CAN0_STB P116	8	n.c.	10k pullup

The 60 Ohm termination of the CAN0 interface can be activated by closing jumper JP1.

3.6.2 CAN1

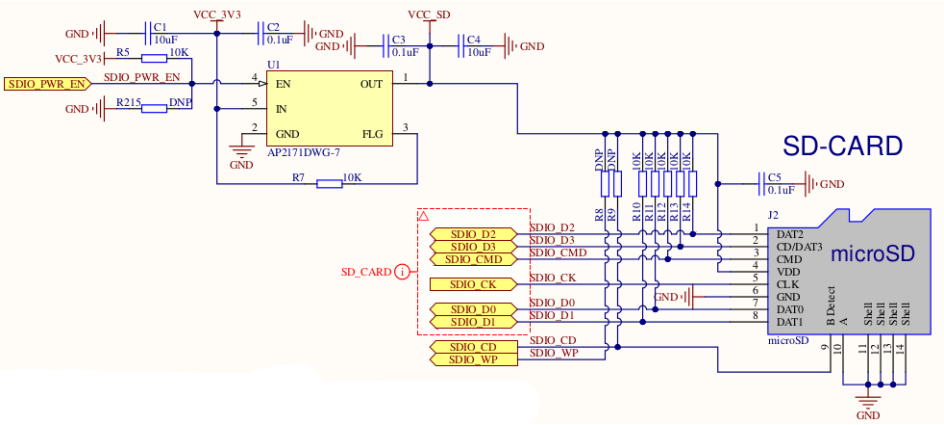
SoM Signal	MCP2562-E signal	P6 Pin	Remark
CAN1_TX P145	1	n.c.	
n.c.	2	n.c.	GND
n.c.	3	n.c.	5V
CAN1_RX P146	4	n.c.	
n.c.	5	n.c.	1.8V
n.c.	6	CANL	
n.c.	7	CANH	
GPIO9_CAN1_STB P117	8	n.c.	10k pullup

The 60 Ohm termination of the CAN1 interface can be activated by closing jumper JP2.

3.7 SD-card

The MSRZG2LSEVK supports a µSD-card slot on connector J2. The interface is connected as follows:

SoM Signal	J1 Pin	Remark
SDIO_CK	P36	
SDIO_CMD	P34	pullup 10k
SDIO_CD	P35	
SDIO_WP	P33	
SDIO_D0	P39	pullup 10k
SDIO_D1	P40	pullup 10k
SDIO_D2	P41	pullup 10k
SDIO_D3	P42	pullup 10k



3.8 Miscellaneous Signals

Connector P1 hosts various signals on a 2.54” pin header:

P1 Pin	Signal Name	J1 Pin	Remark
1	n.a.	n.c.	VCC 1.8V
2	n.a.	n.c.	VCC3V3
3	RE-SET_OUT#	P126	
4	I2C_GP_CK	S48	
5	SER1_TX	P134	33R serial
6	I2C_GP_DAT	S49	
7	SER1_RX	P135	33R serial 10k pullup 1V8
8	GPIO_0	P108	
9	SPI_CS1#	P55	
10	GPIO_4	P112	
11	SPI_DIN	P57	pull down GND
12	GPIO_6	P114	
13	SPI_DO	P58	
14	GPIO_7	P115	
15	SPI_CS0#	P54	
16	GPIO_10	P118	
17	SPI_DO	P58	
18	GPIO_11	P119	
19	n.a.	n.c.	GND
20	n.a.	n.c.	GND

3.9 Reset Button

Switch P4 provides a push button which, if pressed and active, resets the CPU SoM. Closing P4 pulls signal RESET_IN# contact P127 of the 314 pins edge connector P1 to GND.

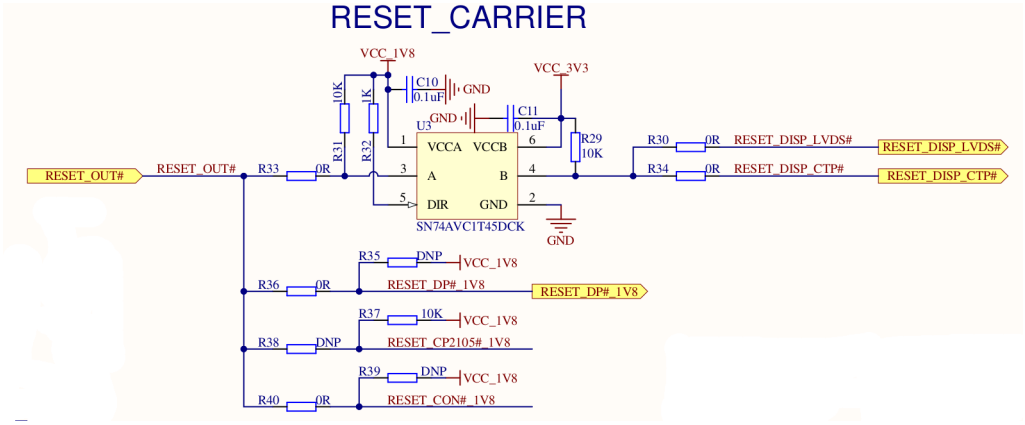
With inactive reset state the LED D18 is set to active, having and active reset state the LED is set to inactive.

3.10 Power Button

Switch P3 acts a power button to start an inactive CPU SoM, depending on the configuration of the CPU SoM. Closing P3 pulls signal POWER_BTN# contact P128 of the 314 pins edge connector P1 to GND.

3.11 Baseboard reset

The signal RESET_OUT#, referenced to contact P126 of the 314 pins edge connector P1 resets the baseboard.



Signal	Component/Pin	Remarks
RESET_OUT#	U8 Pin J9	display brige
	J10 Pin 29	LVDS display connector
	J9 Pin 6	touch panel connector
	U2 Pin 9	USB to serial bridge
	P1 Pin 3	SD-card connector

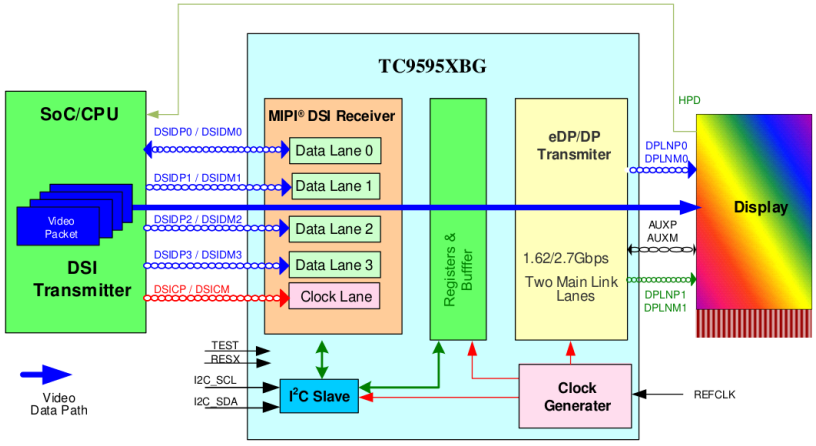
3.12 DSI Display Subsystem

3.12.1 TC9595 DSI Converter U8

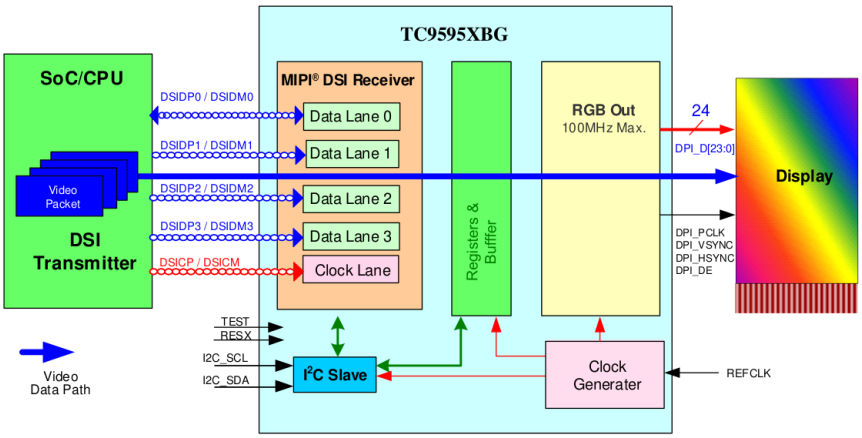
The DSI/DPI to DisplayPort converter (TC9595XBG) is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI ® DSI or DPI link to drive DisplayPort display panels. TC9595XBG also supports audio streaming from the host via I2S interface to the Display panels. TC9595XBG provides a low power bridge solution to efficiently translate MIPI ® DSI or DPI transfers to DisplayPort TM transfers. As the DisplayPort TM uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC9595XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort TM interface and also to connect to existing panels over longer distance using DisplayPort TM adaptors at far-end.

The RZ/G2L CPU supports a MIPI-DSI interface on the MRZG2LS SoM and offers the following functional modes:

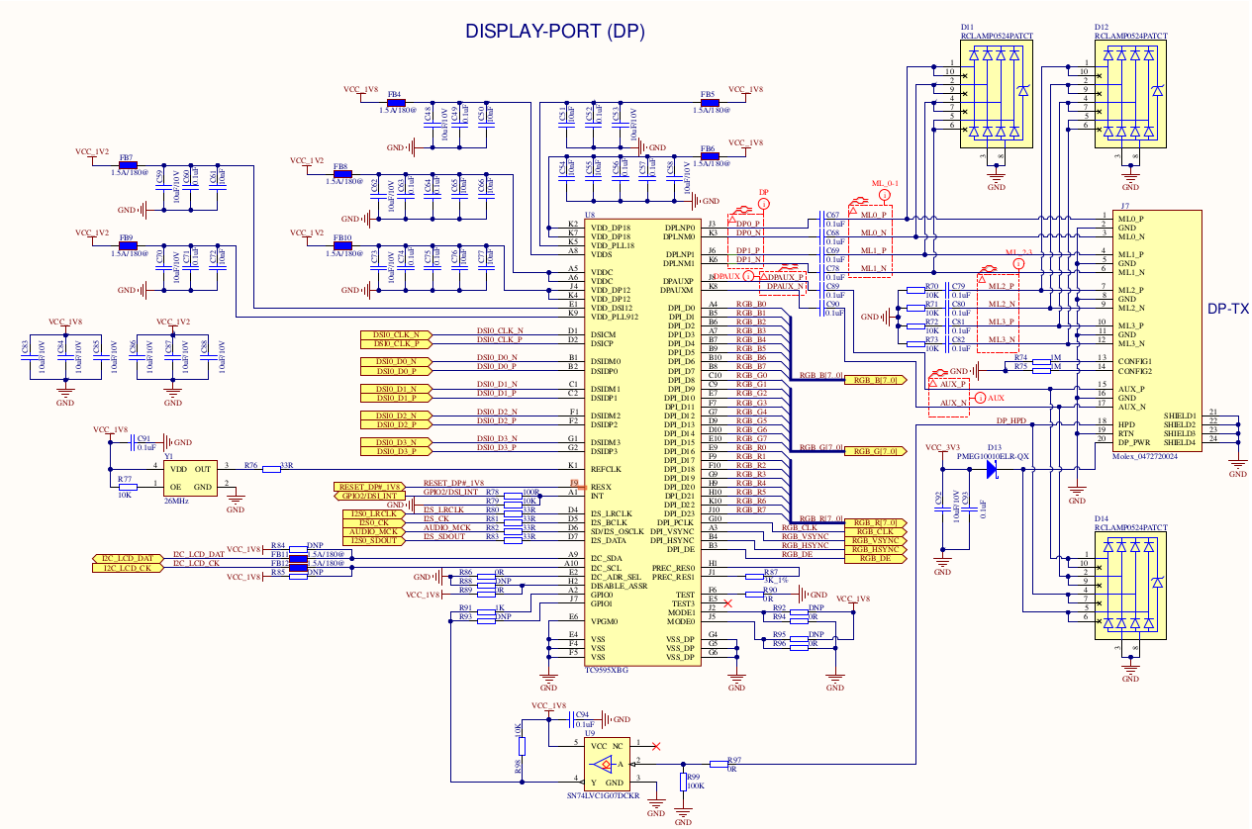
MIPI-DSI to Display Port



MIPI-DSI to RGB



On the MRZG2LSEVK the U8 DSI converter is connected as follows:



Signals direction from the CPU

Signal/P1 Pin	TC9595BGX U8 Signal	Device/Pin	Remark
DSI0_CLK_N/S135	D1		
DSI0_CLK_P/S134	D2		
DSI0_D0_N/S126	B1		
DSI0_D0_P/S125	B2		
DSI0_D1_N/S129	C1		
DSI0_D1_P/S128	C2		
DSI0_D2_N/S132	F1		
DSI0_D2_P/S131	F1		
DSI0_D3_N/S138	G1		
DSI0_D3_P/S137	G2		
	K1	Y1/3	26MHz ref.clock
RESET_OUT#/P126	J9		
GPIO2/DSI_INT	A1		pull down 10k
I2S0_LRCLK/S39	D4		
I2S0_CK/S42	D5		
AUDIO_MCK/S38	D6		
I2S0_SDOUT/S40	D7		
I2C_LCD_DAT/S140	A9	J9/4 J10/7	via voltage translator
I2C_LCD_CK/S139	A10	J9/6 J10/6	via voltage translator
	I2C_ADR_SEL/E2		GND
	DISABLE_ASSR/H2		1.8V
	GPIO_0/A2	J7/18	
	VPGM0/E6		GND
	VPGM0/E6		GND

Signals direction to the display interface

Signal/P1 Pin	TC9595BGX U8 Signal	Device/Pin	Remark
	DPLNP0/J3	J7/1	
	DPLNM0/K3	J7/3	
	DPLNP1/J6	J7/4	
	DPLNM1/K6	J7/6	
	DPAUXP/J8	J7/15	
	DPAUXM/K6	J7/17	
	DPID0/A4	J8/21	RGB B
	DPID1/B5	J8/22	RGB B
	DPID2/B6	J8/23	RGB B
	DPID3/A7	J8/24	RGB B
	DPID4/B7	J8/25	RGB B
	DPID5/B9	J8/26	RGB B
	DPID6/B10	J8/27	RGB B
	DPID7/B8	J8/28	RGB B
	DPID8/C10	J8/13	RGB G
	DPID9/C9	J8/14	RGB G
	DPID10/E7	J8/15	RGB G
	DPID11/F7	J8/16	RGB G
	DPID12/G7	J8/17	RGB G
	DPID13/D9	J8/18	RGB G
	DPID14/D10	J8/19	RGB G
	DPID15/E10	J8/20	RGB G
	DPID16/E9	J8/5	RGB R
	DPID17/F9	J8/6	RGB R
	DPID18/F10	J8/7	RGB R
	DPID19/G9	J8/8	RGB R
	DPID20/H9	J8/9	RGB R
	DPID21/H10	J8/10	RGB R
	DPID22/K10	J8/11	RGB R
	DPID23/J10	J8/12	RGB R
	DPI_PCLK/G10	J8/30	
	DPI_VSYNC/A3	J8/33	
	DPI_HSYNC/B4	J8/32	
	DPI_DE/B3	J8/34	

3.12.2 Display Port Connector J7

The MRZG2LSEVK hosts a Display Port interface on connector J7 type Molex 0472720024. J7 is connected to the TC9595 DSI Converter U8.

3.12.3 RGB-Display Connector J8

TC9595BGX U8 Signal	J8 Pin	Remark
	1	Pin1 LED-K of backlight driver TPS61165DRV
	2	Pin4 LED-A of backlight driver TPS61165DRV
	3	GND
	4	3V3
DPID16/E9	5	RGB R
DPID17/F9	6	RGB R
DPID18/F10	7	RGB R
DPID19/G9	8	RGB R
DPID20/H9	9	RGB R
DPID21/H10	10	RGB R
DPID22/K10	11	RGB R
DPID23/J10	12	RGB R
DPID8/C10	13	RGB G
DPID9/C9	14	RGB G
DPID10/E7	15	RGB G
DPID11/F7	16	RGB G
DPID12/G7	17	RGB G
DPID13/D9	18	RGB G
DPID14/D10	19	RGB G
DPID15/E10	20	RGB G
DPID0/A4	21	RGB B
DPID1/B5	22	RGB B
DPID2/B6	23	RGB B
DPID3/A7	24	RGB B
DPID4/B7	25	RGB B
DPID5/B9	26	RGB B
DPID6/B10	27	RGB B
DPID7/B8	28	RGB B
DPI_PCLK/G10	30	
DPI_HSYNC/B4	32	
DPI_VSYNC/A3	33	
DPI_DE/B3	34	
	35	n.c.
	36	GND
	37	n.c.
	38	n.c.
	39	n.c.
	40	n.c.

3.13 Touch Screen Connector J9

TC9595BGX U8 Signal	J9 Pin	Remark
	1	3V3
	2	GND
I2C_SCL/A10	3	
I2C_SAD/A9	4	
	5	GPIO13/CTP_INT# /P1 S123
	6	RESET_OUT#/P1 P126

3.14 LVDS-Display Connector J10

The MRZG2LSEVK hosts a LVDS-display interface to be used with SMARC SoMs other than the MRZG2LS. The interface is available on connector J10 and provides the following signals:

J10 Pin	Connector P1 Contact/ Signal	TC9595BGX U8 Signal
1	GND	
2	3V3	
3	3V3	
4	3V3	
5	GND	
6		I2C_SCL/A10
7		I2C_SDA/A9
8	LVDS1_D0_N/S112	
9	LVDS1_D0_P/S111	
10	GND	
11	LVDS1_D1_N/S115	
12	LVDS1_D1_P/S114	
13	GND	
14	LVDS1_D2_N/S118	
15	LVDS1_D2_P/S119	
16	GND	
17	LVDS1_CK_N/S109	
18	LVDS1_CK_P/S108	
19	GND	
20	LVDS1_D3_N/S121	
21	LVDS1_D3_P/S120	
22	GND	
23	GND	
24	GND	
25	GND	
26	GND	
27	3V3	
28	GND	
29	RESET_OUT#/P126	
30	3V3	10k pull up
31	GND	
32	GND	
33	GND	
34	GND	
35	LCD1_BKLT_PWM/S122	
36	LCD1_BKLT_EN/S107	
37	GND	
38		
39		
40		

3.15 Camera Interface P7

The MRZG2LSEVK provides the MIPI-CSI2 camera interface of the RZ/G2L CPU on connector P7, type Amphenol 61083-044402LF:

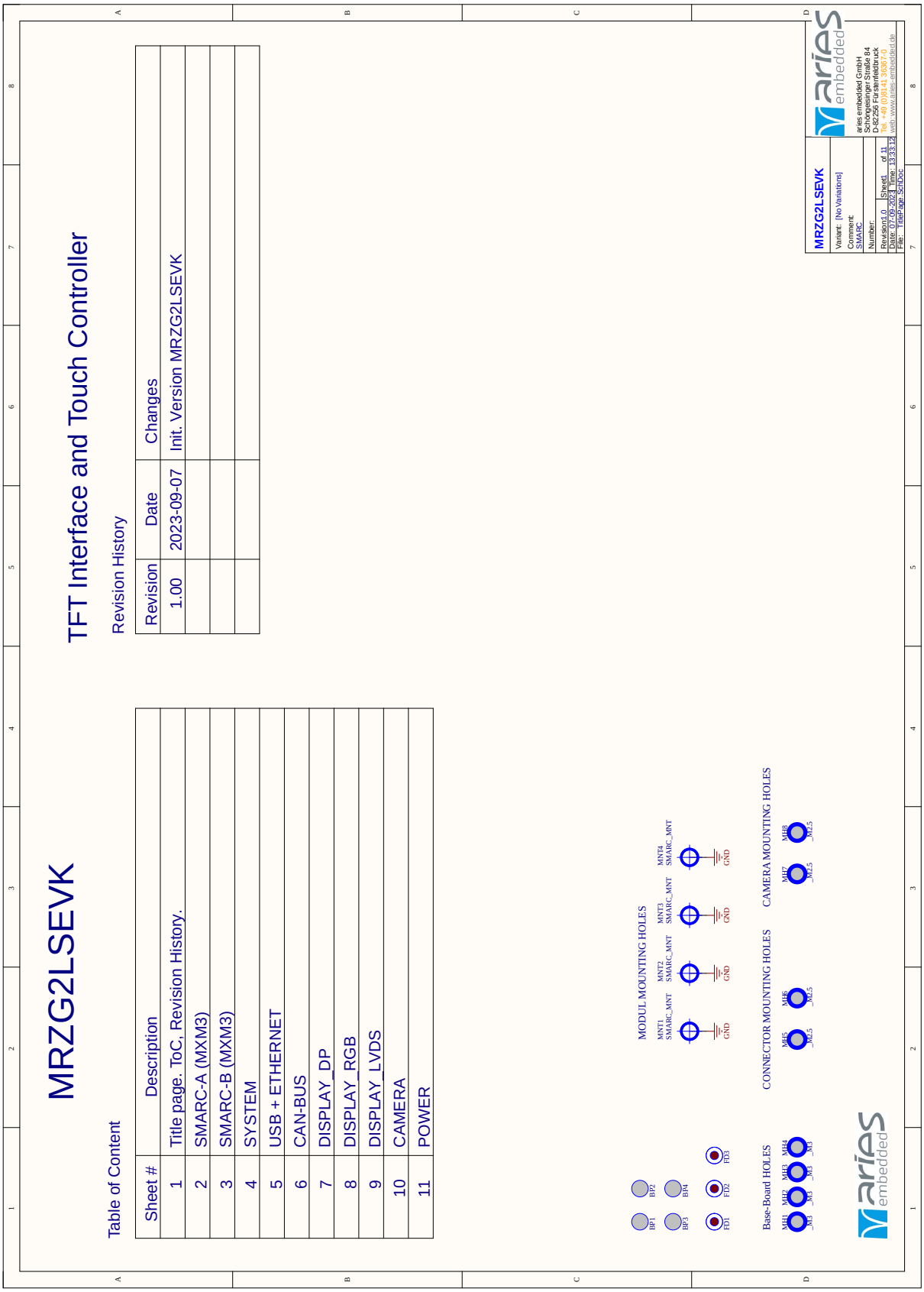
P7 Pin	Connector P1 Contact/ Signal	Remarks
1		3V3
2		3V3
3	CAM_MCK/S6	
4		5V
5		GND
6		GND
7	CSI1_CK_P/P3	
8		n.c.
9	CSI1_CK_N/P4	
10		n.c.
11		GND
12		GND
13	CSI1_RX0_P/P7	
14		n.c.
15	CSI1_RX0_N/P8	
16		n.c.
17		GND
18		GND
19	CSI1_RX1_P/P10	
20		n.c.
21	CSI1_RX1_N/P11	
22		n.c.
23		GND
24		GND
25	CSI1_RX2_P/P13	
26		n.c.
27	CSI1_RX2_N/P14	
28		n.c.
29		GND
30		GND
31	CSI1_RX3_P/P16	
32		n.c.
33	CSI1_RX3_N/P17	
34		n.c.
35		GND
36		GND
37	I2C_CAM1_CK/S1	
38	CAM1_PWR#/P109	
39	I2C_CAM1_DAT/S2	
40	CAM1_RST#/P111	

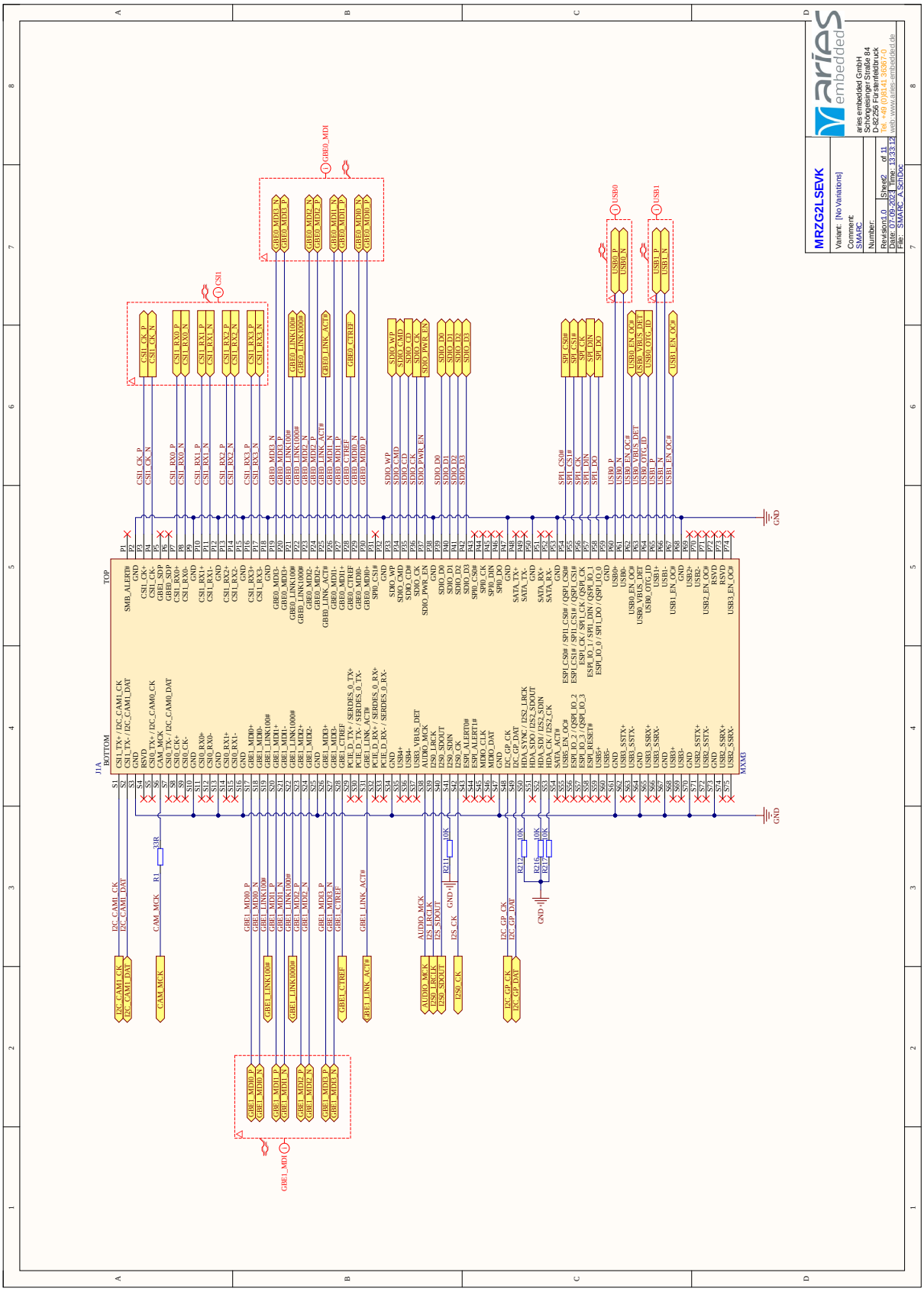
CHAPTER

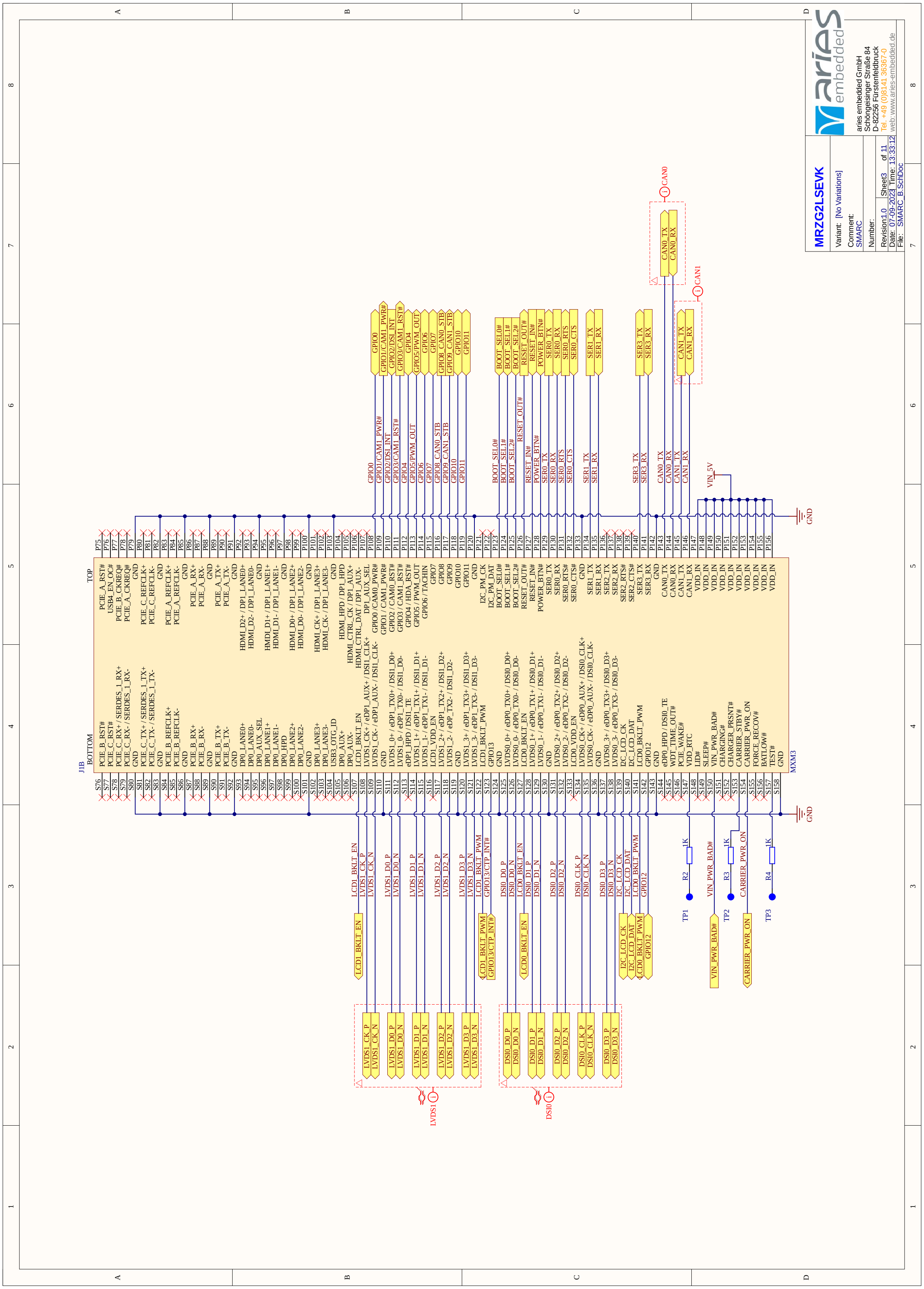
FOUR

SCHEMATICS

A more detailed and searchable document on the parts overview can be made available on request under email sales@aries-embedded.de.


MRZG2LSEVK
TFT Interface and Touch Controller
Table of Content
Sheet # Description
1 Title page. ToC, Revision History.
2 SMARC-A (MXM3)
3 SMARC-B (MXM3)
4 SYSTEM
5 USB + ETHERNET
6 CAN-BUS
7 DISPLAY_DP
8 DISPLAY_RGB
9 DISPLAY_LVDS
10 CAMERA
11 POWER
Revision History
Revision Date Changes
1.00 2023-09-07 Init. Version MRZG2LSEVK
MODUL MOUNTING HOLES
CONNECTOR MOUNTING HOLES
CAMERA MOUNTING HOLES
Base-Board HOLES
MRZG2LSEVK
aries embedded GmbH
Schorndelsiger Straße 64
D-90425 Nürnberg
Tel.: +49 (0)911 93367-0
web: www.aries-embedded.de

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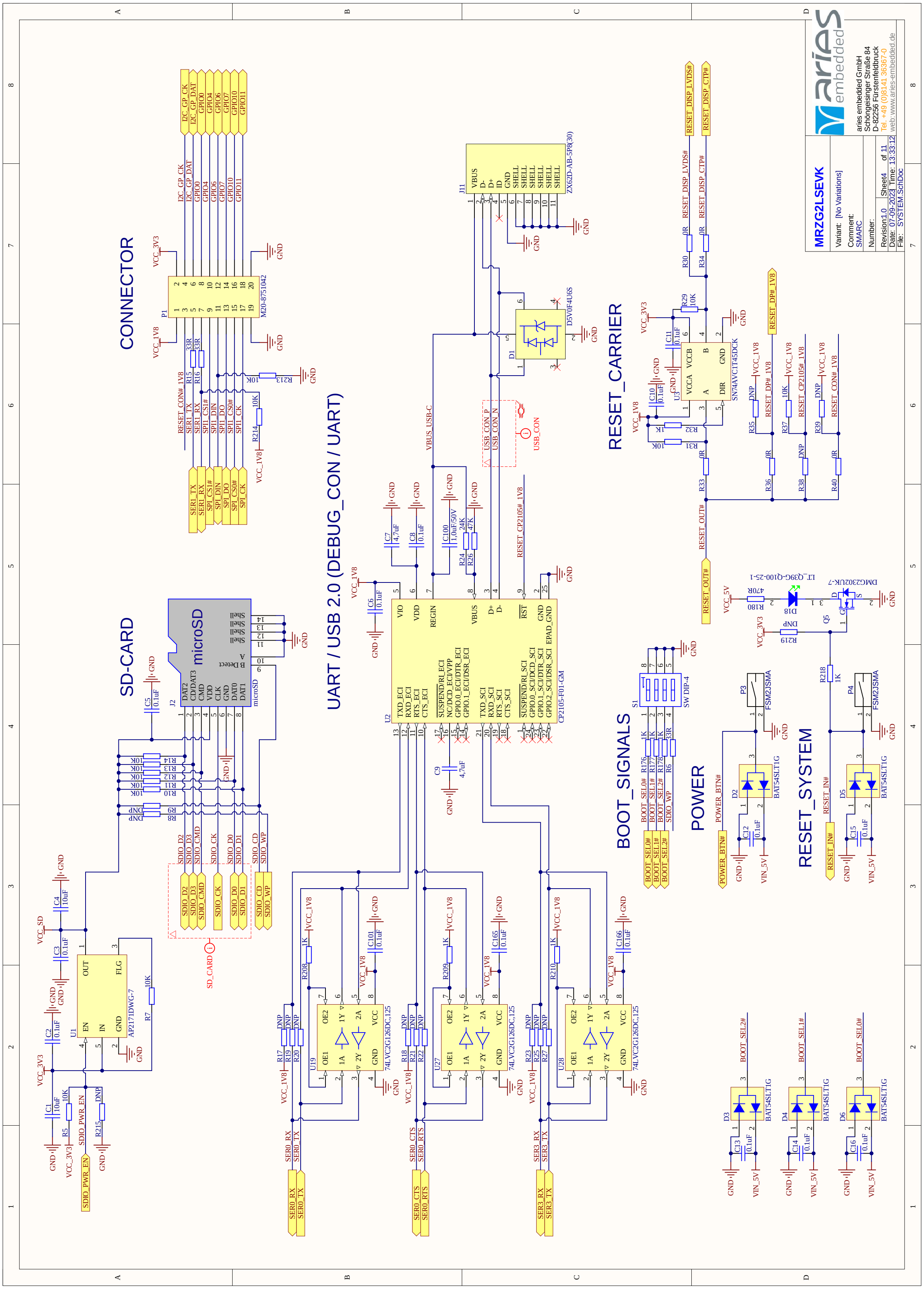
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
web: www.aries-embedded.de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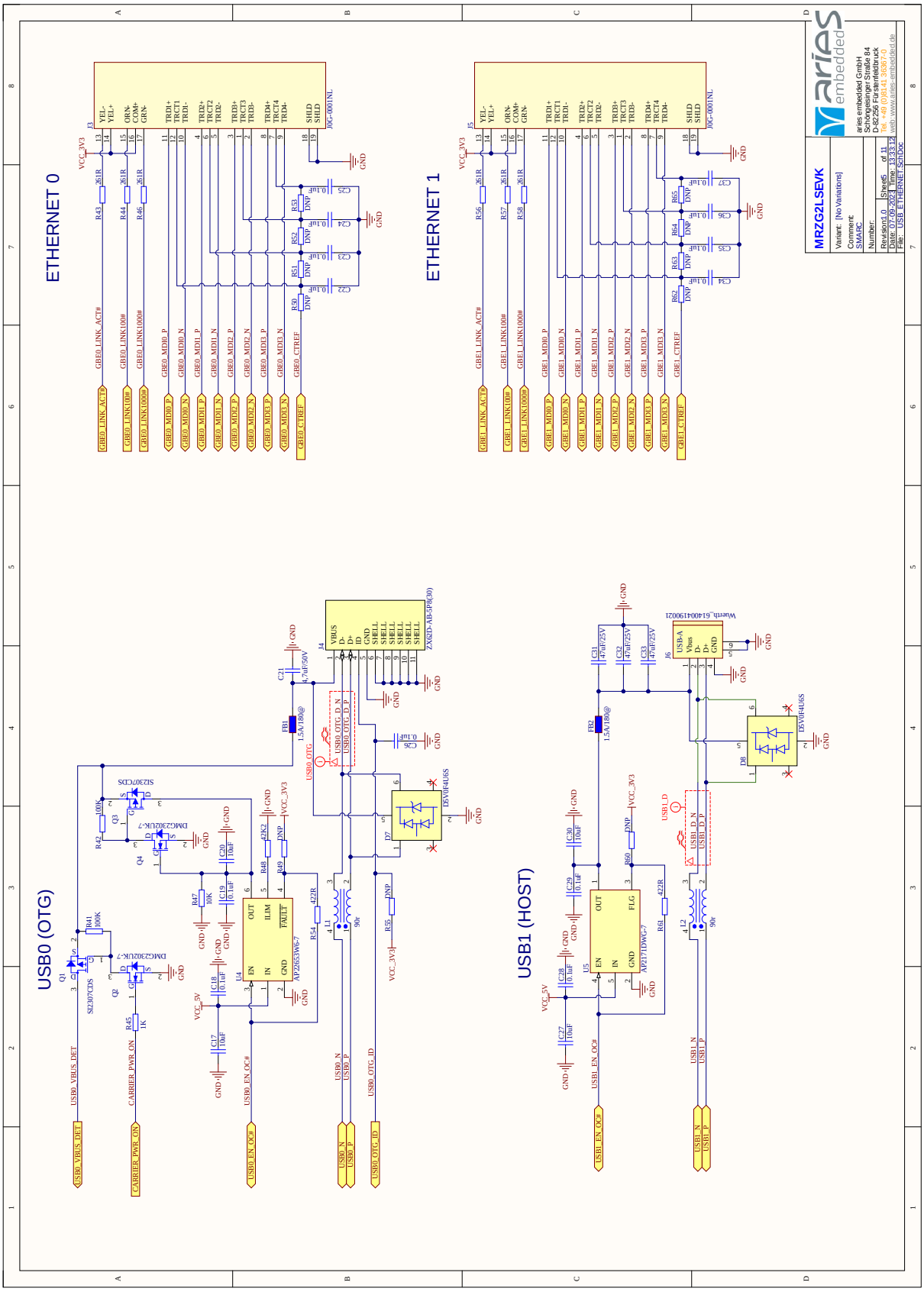
SD-CARD
UART / USB 2.0 (DEBUG_CON / UART)
RESET_CARRIER
BOOT_SIGNALS
POWER
RESET_SYSTEM
MRZG2LSEVK
aries embedded GmbH
Schongauer Straße 84
D-82256 Fürstenfeldbruck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ETHERNET 1
USB0 (OTG)
USB1 (HOST)
MRZG2LSEVK
aries embedded GmbH
Schorlingeser Straße 64
D-26736 Krummhörn/OT Upgant-Schott
Tel.: +49 (0)4923 3338710
web: www.aries-embedded.de
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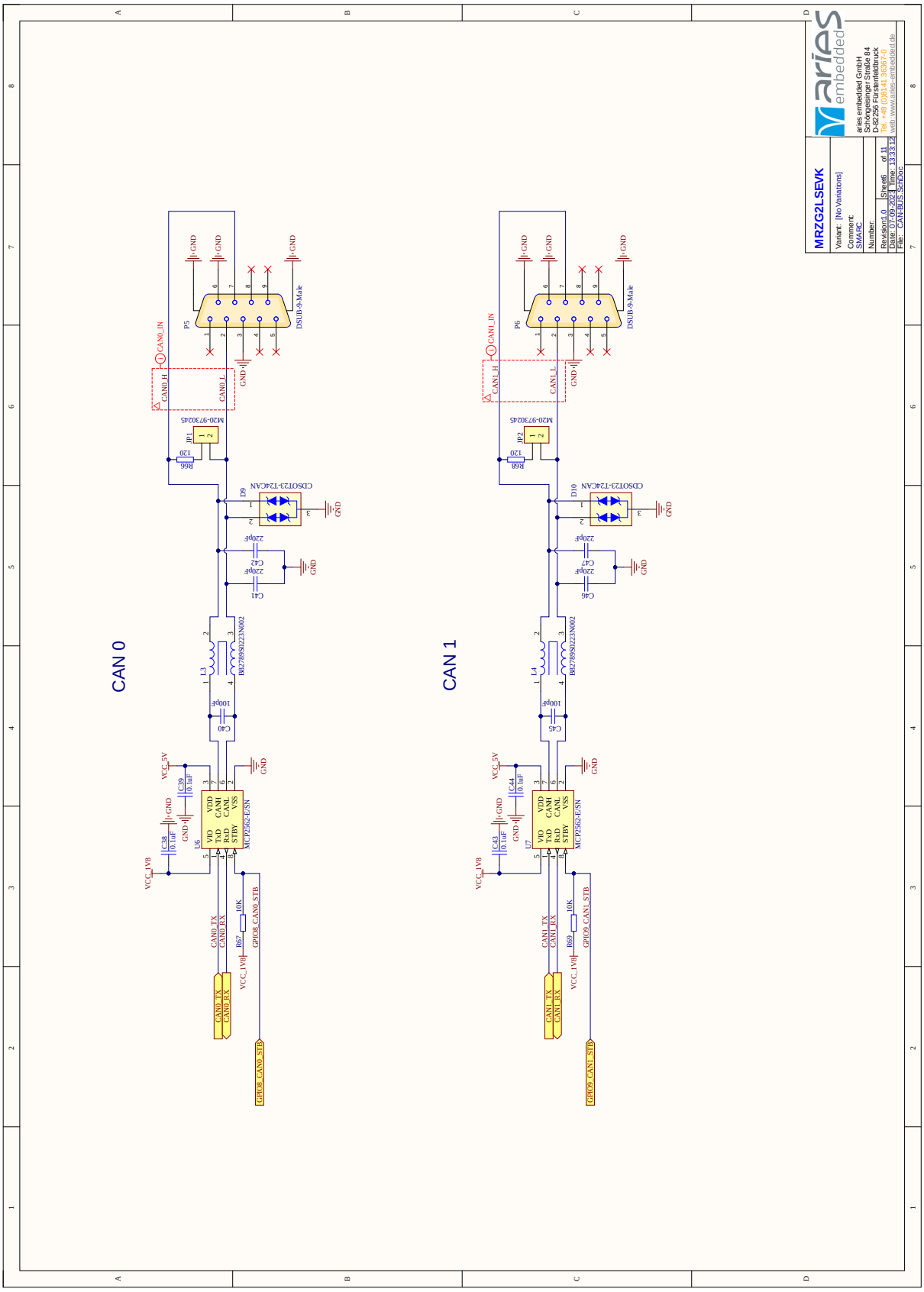
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CAN 1
MRZG2LSEVK
aries embedded GmbH
Schorndorfer Straße 64
D-70734 Fellbach/Stuttgart
Tel.:+49 (0)711 / 93 87 70
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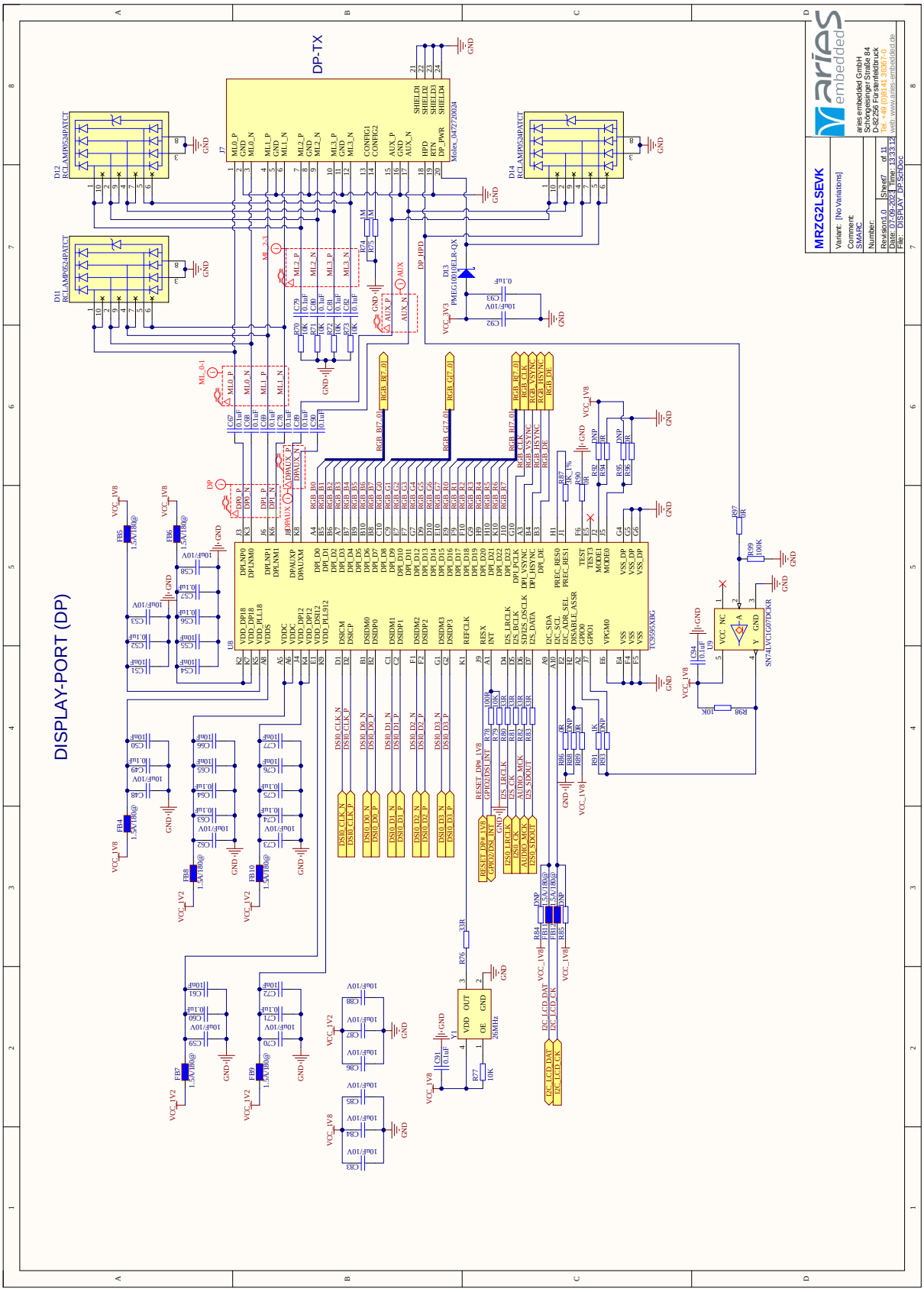
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DP-TX
MRZG2LSEVK
aries embedded GmbH
Schorndelsinger Straße 64
D-82256 Fürstenfeldbruck
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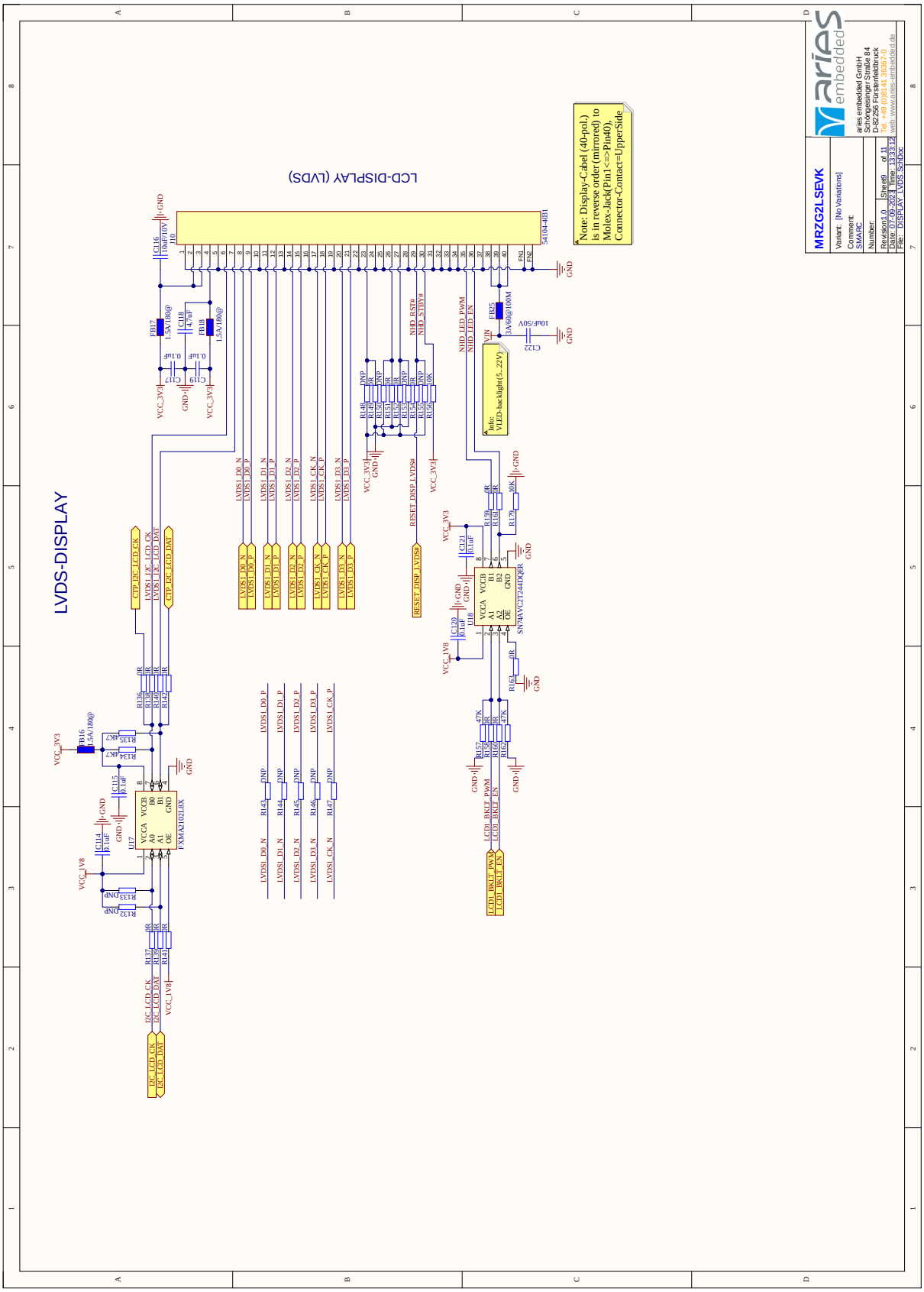
LVDS-DISPLAY
LCD-DISPLAY (LVDS)
Note: Display-Cabel (40-pol.) is in reverse order (mirrored) to Molex-Jack(Pin1<=>Pin40). Connector-Contact=UpperSide
MRZG2LSEVK
aries embedded GmbH
Schorndelsiger Straße 64
D-82256 Fürstenfeldbruck
Tel.:+49 (0)8141 / 535740
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Revision1.0
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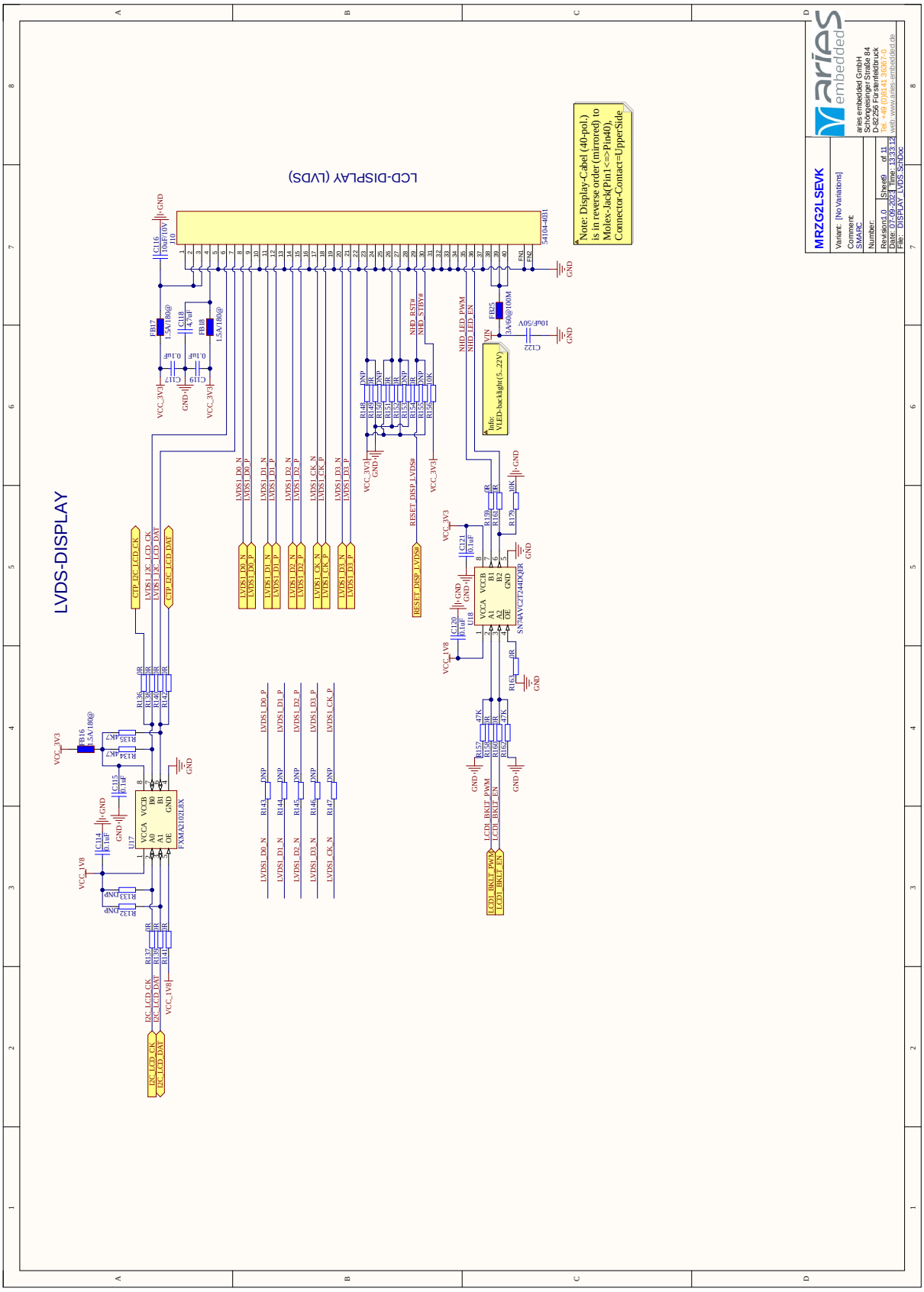
SN74AVC2T244DQ8R


LVDS-DISPLAY
LCD-DISPLAY (LVDS)
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aries embedded GmbH
Schorndelsiger Straße 64
D-82256 Fürstenfeldbruck
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web: www.aries-embedded.de
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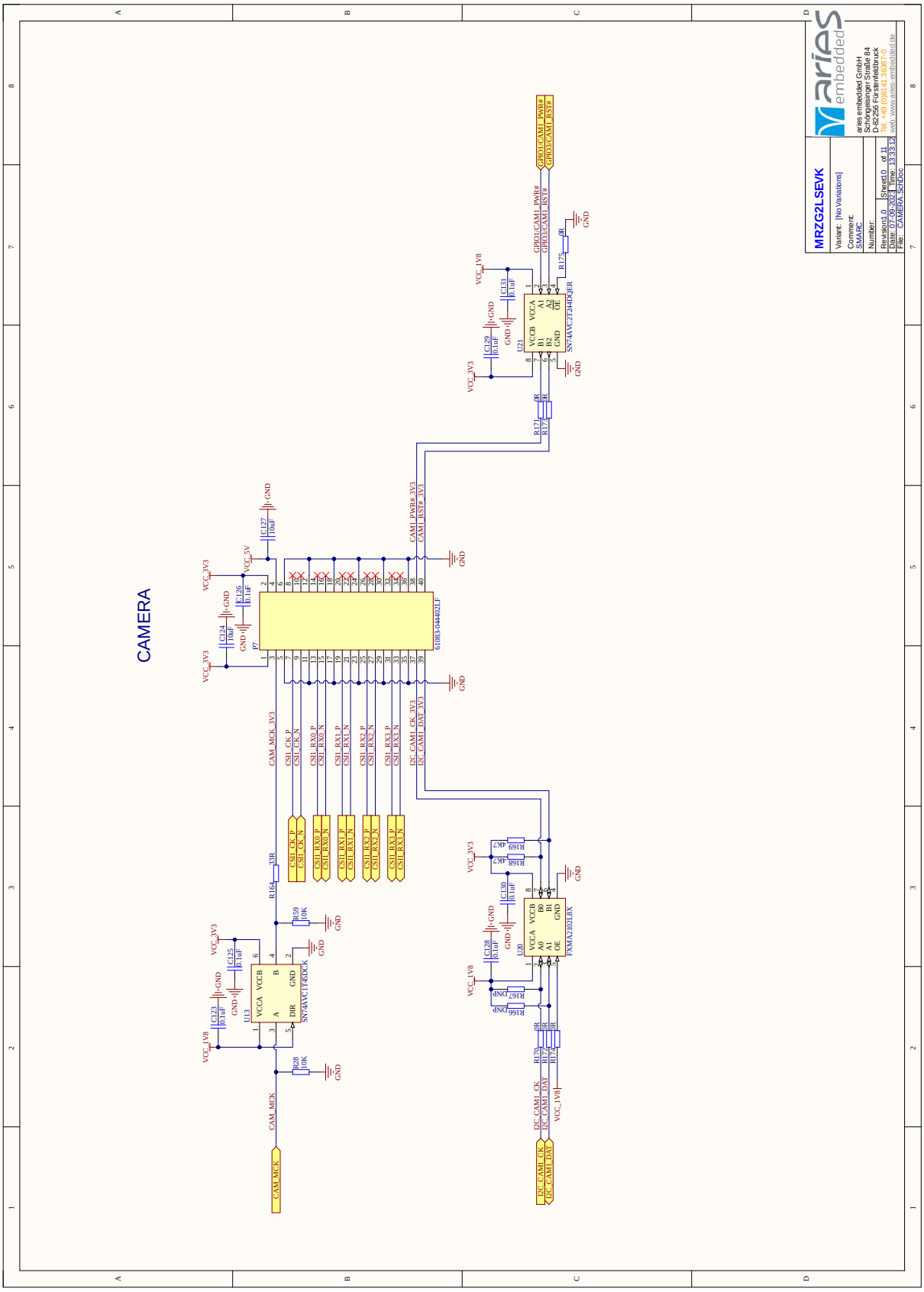
FXMA2102L8X


CAMERA
MRZG2LSEVK
aries embedded GmbH
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D-73650 Winterbach
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web: www.aries-embedded.de
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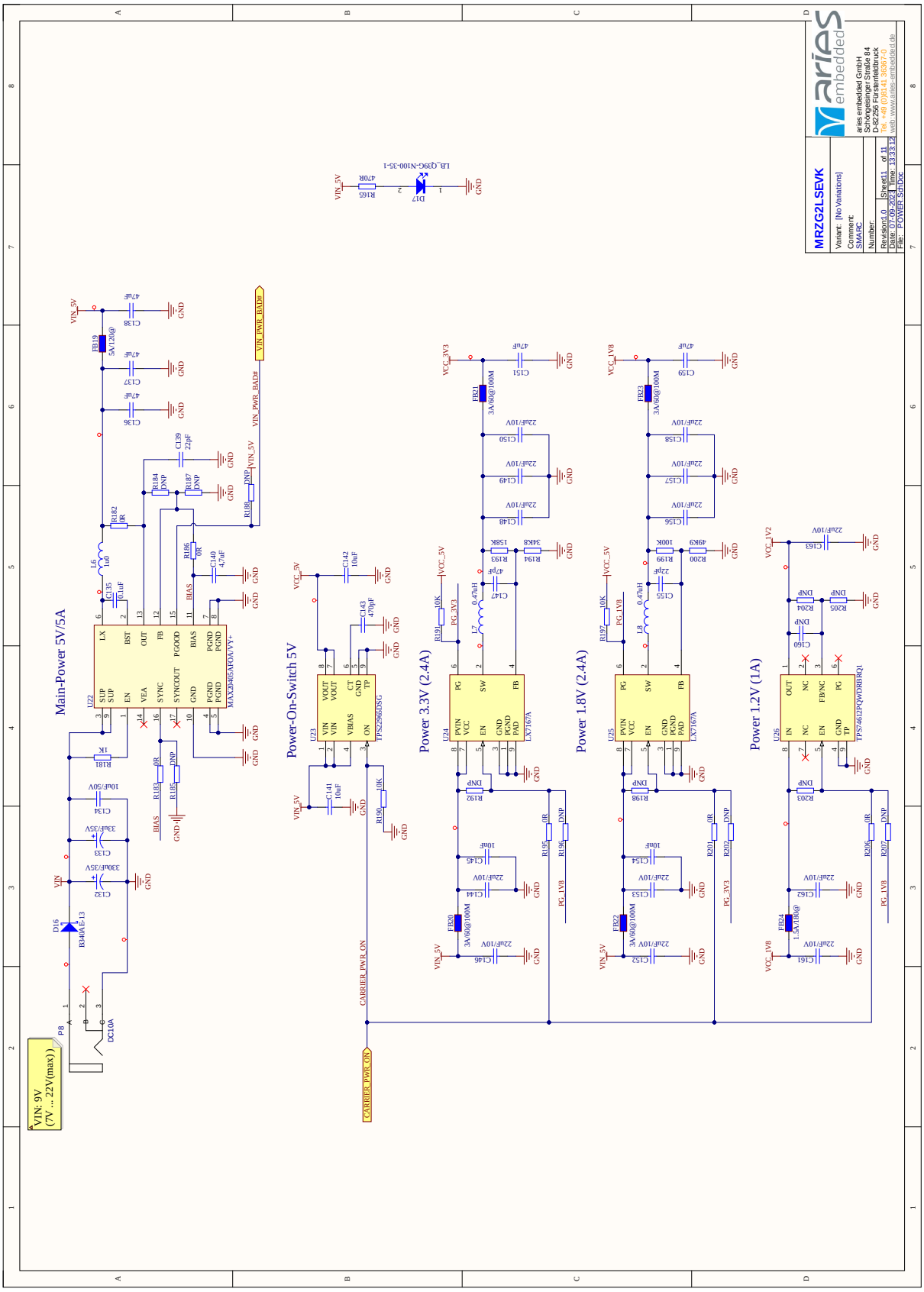
MRZG2LSEVK
Main-Power 5V/5A
Power-On-Switch 5V
Power 3.3V (2.4A)
Power 1.8V (2.4A)
Power 1.2V (1A)
VIN: 9V
(7V ... 22V(max))
CARRIER_PWR_ON
VIN_PWR_BAD#
aries embedded GmbH