
MCXLEVK Hardware Manual

Release 1.0

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ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	11.05.2021	dk	Initial creation
1.1	19.01.2022	dk	New Block Diagram New Feature Set PMod connectors are designed upside-down FPGA Pins for Pmodes

OVERVIEW

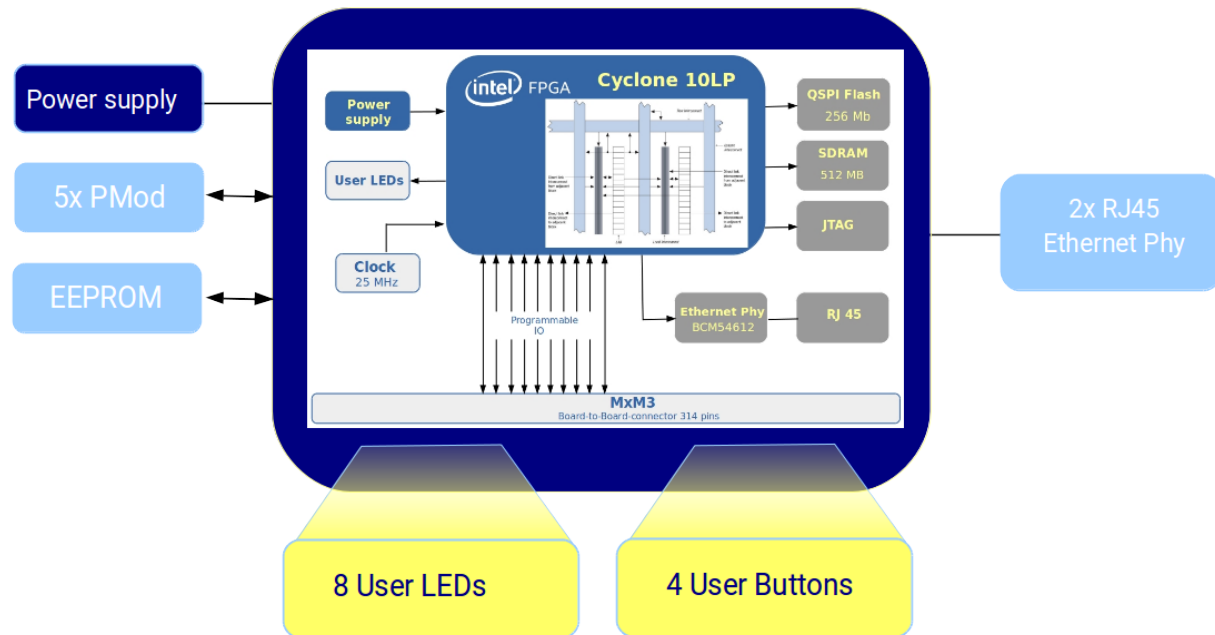
2.1 MCXLEVK

MCXLEVK represents the flexible Evaluation Platform for working with the MCXL SoM.

The system helps developers to have a smooth start with the MCXL SoMs, it can be used for designing IP, developing software as well as implementing prototypes.



2.2 Block Diagram

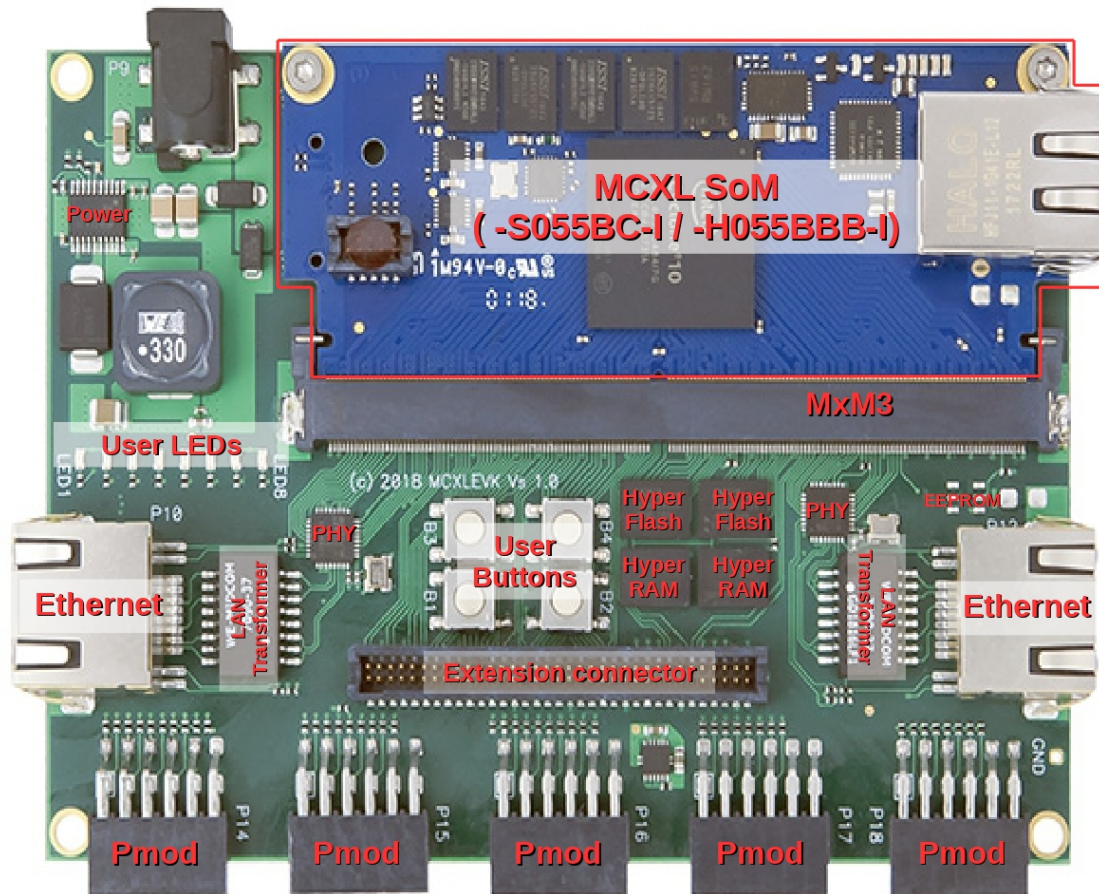


2.3 Feature Set

- MCXLEVK Cyclone 10LP
- MCXL-S055BC-I
- MCXL-H055BBB-I
- SPI EEPROM
- 8 User LEDs
- 4 User Buttons
- 5 PMod
- 2x RJ45 Ethernet Phy
- Power Supply
- 118mmx83mm

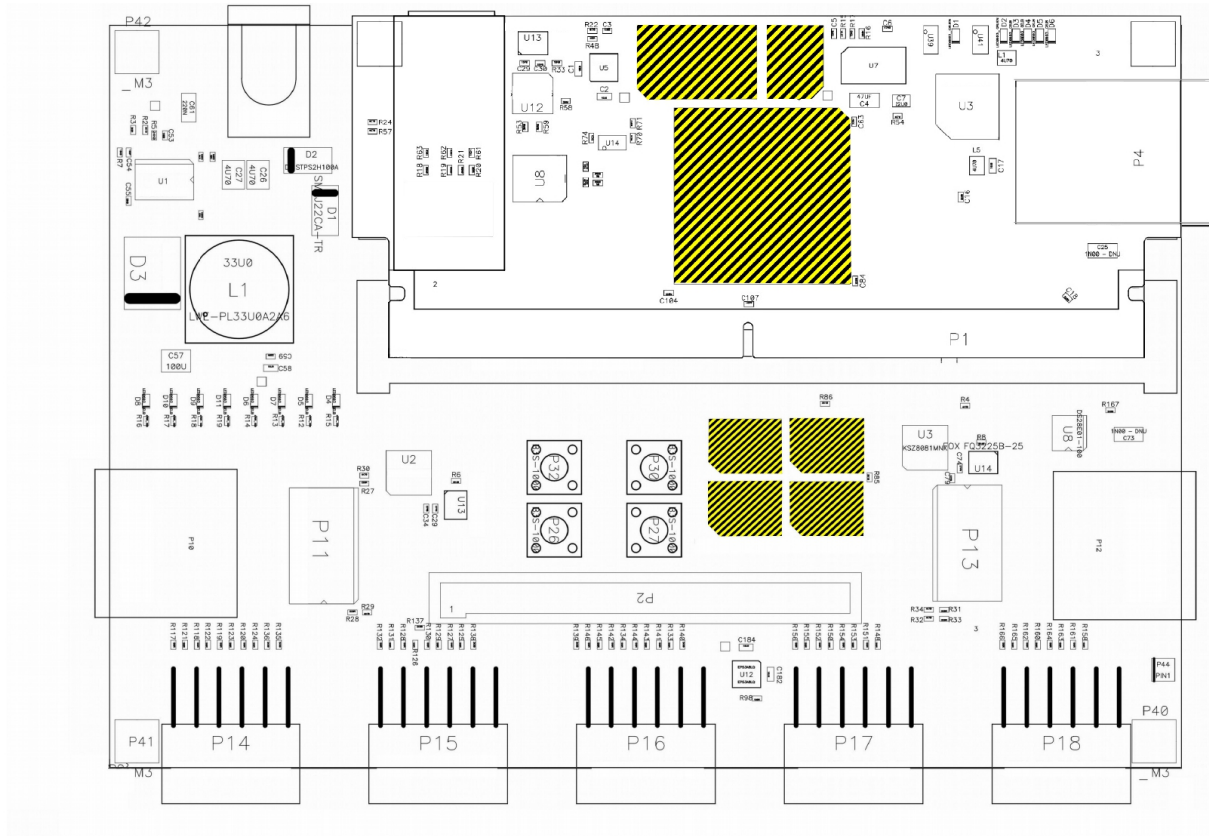
2.5 Parts Location

The available functional blocks can be found on the baseboard as follows:



2.6 Handling Recommendations

To avoid mechanical damage to the components populated on MCXLEVK it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figures below:



MCXLEVK + MCXL-S055BC-I

RESOURCES

3.1 HyperRam and HyperFlash

The MCXLEVK is equipped with two IS66WVH8M8-ALL-166B1L1 128MBit HyperRAM and two S26KS512S 512MBit HyperFlash.

The IS66WVH8M8-ALL-166B1L1 manufactured by ISSI, Integrated Silicon Solution Incare two integrated memory devices resulting in up to 256MB of 64Mbit Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 8M words by 8bits.

The S26KS512S manufactured by Cypress Semiconductor are two high-speed CMOS MirrorBit NOR flash devices resulting in up to 1024 MB of 64bit HyperFlash memory.

3.1.1 HyperFlash Signals

Function	Board Pin	FPGA Function	Pin	Pin	Function	Board Pin	FPGA Function
HyperFlash U5				HyperFlash U7			
RSTN	–	RSTN	A4	A4	RSTN	–	RSTN
HB0CS0	P1-235	B6IO18	C2	C2	HB1CS0	P1-250	B6IO31
HB0CK0	P1-240	B6IO21	B2	B2	HB1CK0	P1-249	B6IO30
HB0CK0	P1-239	B6IO20	B1	B1	HB1CK0	P1-248	B6IO29
HB0RST	P1-243	B6IO25	A2	A2	HB0RST	P1-103	B6IO17
HB0INT	P1-233	B6IO34	A5	A5	HB0INT	P1-90	B6IN0
HB0RWDS	P1-80	B6IO0	C3	C3	HB1RWDS	P1-92	B6IO8
HB0DQ0	P1-85	B6IO4	D3	D3	HB1DQ0	P1-97	B6IO12
HB0DQ1	P1-87	B6IO6	D2	D2	HB1DQ1	P1-100	B6IO14
HB0DQ2	P1-81	B6IO1	C4	C4	HB1DQ2	P1-93	B6IO9
HB0DQ3	P1-83	B6IO3	D4	D4	HB1DQ3	P1-96	B6IO11
HB0DQ4	P1-82	B6IO2	D5	D5	HB1DQ4	P1-95	B6IO10
HB0DQ5	P1-86	B6IO5	E3	E3	HB1DQ5	P1-98	B6IO13
HB0DQ6	P1-242	B6IO24	E2	E2	HB1DQ6	P1-101	B6IO15
HB0DQ7	P1-88	B6IO7	E1	E1	HB1DQ7	P1-102	B6IO16

3.1.2 HyperRAM Signals

Function	Board Pin	FPGA Function	Pin	Pin	Function	Board Pin	FPGA Function
HyperRAM U4				HyperRAM U6			
RSTN	–	RSTN	A4	A4	RSTN	–	RSTN
HB0CS1	P1-234	B6IO18	A3	A3	HB1CS1	P1-247	B6IO28
HB0CK1	P1-238	B6IO21	B2	B2	HB1CK1	P1-245	B6IO27
HB0CK1	P1-237	B6IO20	B1	B1	HB1CK1	P1-244	B6IO26
HB0RWDS	P1-80	B6IO0	C3	C3	HB1RWDS	P1-92	B6IO8
HB0DQ0	P1-85	B6IO4	D3	D3	HB1DQ0	P1-97	B6IO12
HB0DQ1	P1-87	B6IO6	D2	D2	HB1DQ1	P1-100	B6IO14
HB0DQ2	P1-81	B6IO1	C4	C4	HB1DQ2	P1-93	B6IO9
HB0DQ3	P1-83	B6IO3	D4	D4	HB1DQ3	P1-96	B6IO11
HB0DQ4	P1-82	B6IO2	D5	D5	HB1DQ4	P1-95	B6IO10
HB0DQ5	P1-86	B6IO5	E3	E3	HB1DQ5	P1-98	B6IO13
HB0DQ6	P1-242	B6IO24	E2	E2	HB1DQ6	P1-101	B6IO15
HB0DQ7	P1-88	B6IO7	E1	E1	HB1DQ7	P1-102	B6IO16

3.2 User LEDs

The eight signals, that can be used to read the Ident value of the board, are connected via a Buffer to eight LEDs. To read the ident value, enable the internal Pull-Ups and to set the ident value four 1K resistors can be equipped to set a “zero” to the respective signal. If no resistor is equipped a “one” is red.

Function	FPGA Signal	Connector	Pulldown
LED1	B4IO20	P1-A 187	R1
LED2	B4IO21	P1-A 188	R2
LED3	B4IO22	P1-A 189	R3
LED4	B4IO23	P1-A 190	R4
LED5	B4IO24	P1-A 192	R5
LED6	B4IO25	P1-A 193	R6
LED7	B4IO26	P1-A 194	R7
LED8	B4IO27	P1-A 195	R8

3.3 EEPROM

General Description The DS28E01-100 combines 1024 bits of EEPROM with challenge-and-response authentication security implemented with the ISO/IEC 10118-3 Secure Hash Algorithm (SHA-1). The 1024-bit EEPROM array is configured as four pages of 256 bits with a 64-bit scratch-pad to perform write operations. All memory pages can be write protected, and one page can be put in EEPROM-emulation mode, where bits can only be changed from a 1 to a 0 state.

Function	FPGA Signal	Connector	Pulldown
DS28IO	B8IO35	P1-B 151	R167

3.4 User Buttons

The MCXLEVK is equipped with 4 Surface-mounting Switches B3S-1000 with a Sealed Structure for High Reliability.

Function	FPGA Signal	Connector
BUTTON1	RST	P1-A 208
BUTTON2	B4IO36	P1-A 207
BUTTON3	B4IO18	P1-A 209
BUTTON4	B4IO19	P1-A 210

3.5 PMIC

Power on the MCXLEVK is controlled by a LM25576 Texas Instruments Step-Down Switching Regulator. Operating with an input voltage range of 6V to 42V, the LM25576 delivers 3A of continuous output current with an integrated 170-mΩ N-Channel MOSFET. Operating Frequency Adjustable is between 50kHz and 1MHz with Single Resistor.

3.6 Pin Out

3.6.1 PHY Ethernet

The MCXLEVK module is equipped with two single-supply 10Base-T Ethernet KSZ8081MNX physical-layer transceivers which are connected via MII to the board.

PHY U2:

Function	FPGA Signal	Connector	Function	FPGA Signal	Connector
PHY_RSTN	B3IO0	P1-A 5	PHY1_CRS	B3IO1	P1-A 6
PHY1_MDC	B3IO14	P1-A 22	PHY1_RXDO	B3IO10	P1-A 17
PHY1_MDIO	B3IO15	P1-A 23	PHY1_RXD1	B3IO11	P1-A 18
PHY1_TXC	B3IN1	P1-A 26	PHY1_RXD2	B3IO12	P1-A 20
PHY1_TXEN	B3IO7	P1-A 13	PHY1_RXD3	B3IO13	P1-A 21
PHY1_TXDO	B3IO6	P1-A 12	PHY1_INTR	B3IO8	P1-A 15
PHY1_TXD1	B3IO5	P1-A 11	PHY1_RXC	B3IN0	P1-A 25
PHY1_TXD2	B3IO4	P1-A 10	PHY1_RXDV	B3IO9	P1-A 16
PHY1_TXD3	B3IO3	P1-A 8	PHY1_LEDA1	–	–
PHY1_COL	B3IO2	P1-A 7	PHY1_LEDA2	–	–

PHY U3:

Function	FPGA Signal	Connector	Function	FPGA Signal	Connector
PHY_RSTN	B7IO0	P1-A 5	PHY2_CRS	B7IO2	P1-B 107
PHY2_MDC	B7IN0	P1-B 126	PHY2_RXDO	B7IO13	P1-B 121
PHY2_MDIO	B7IN1	P1-B 127	PHY2_RXD1	B7IO14	P1-B 122
PHY2_TXC	B7IO9	P1-B 116	PHY2_RXD2	B7IO15	P1-B 123
PHY2_TXEN	B7IO8	P1-B 115	PHY2_RXD3	B7IO38	P1-B 125
PHY2_TXDO	B7IO7	P1-B 113	PHY2_INTR	B7IO10	P1-B 117
PHY2_TXD1	B7IO6	P1-B 112	PHY2_RXC	B7IO11	P1-B 118
PHY2_TXD2	B7IO5	P1-B 111	PHY2_RXDV	B7IO12	P1-B 120
PHY2_TXD3	B7IO4	P1-B 110	PHY2_LEDA1	–	–
PHY2_COL	B7IO3	P1-B 108	PHY2_LEDA2	–	–

3.6.2 Connectors

Pmod Module Connectors

Five 2x6 angled pin headers are available on the MCXLEVK board which fit the requirements for Pmod modules.

PMod connectors are designed upside-down.

PMOD P14:

Pin	Function	FPGA	FPGA PIN	Connector
1	3.3V	—	—	—
3	GND	—	—	—
5	PMODA7	B5IO21	W20	P1-A 213
7	PMODA6	B5IO23	T18	P1-A 215
9	PMODA5	B5IO25	R19	P1-A 218
11	PMODA4	B5IO27	P20	P1-A 220

Pin	Function	FPGA	FPGA PIN	Connector
2	3.3V	—	—	—
4	GND	—	—	—
6	PMODA3	B5IO20	R17	P1-A 212
8	PMODA2	B5IO22	T17	P1-A 214
10	PMODA1	B5IO24	R18	P1-A 217
12	PMODA0	B5IO26	R20	P1-A 219

PMOD P15:

Pin	Function	FPGA	FPGA PIN	Connector
1	3.3V	—	—	—
3	GND	—	—	—
5	PMODB7	B4IO34	W14	P1-A 204
7	PMODB6	B4IO32	R16	P1-A 202
9	PMODB5	B4IO30	Y17	P1-A 199
11	PMODB4	B4IO28	V15	P1-A 197

Pin	Function	FPGA	FPGA PIN	Connector
2	3.3V	—	—	—
4	GND	—	—	—
6	PMODB3	B4IO35	W15	P1-A 205
8	PMODB2	B4IO33	T16	P1-A 203
10	PMODB1	B4IO31	W17	P1-A 200
12	PMODB0	B4IO29	U15	P1-A 198

PMOD P16:

Pin	Function	FPGA	FPGA PIN	Connector
1	3.3V	—	—	—
3	GND	—	—	—
5	PMODC7	B5IO34	M20	P1-A 229
7	PMODC6	B5IO32	N20	P1-A 227
9	PMODC5	B5IO30	N17	P1-A 224
11	PMODC4	B5IO28	P17	P1-A 222

Pin	Function	FPGA	FPGA PIN	Connector
2	3.3V	—	—	—
4	GND	—	—	—
6	PMODC3	B5IO35	M19	P1-A 230
8	PMODC2	B5IO33	N19	P1-A 228
10	PMODC1	B5IO31	N18	P1-A 225
12	PMODC0	B5IO29	N16	P1-A 223

PMOD P17:

Pin	Function	FPGA	FPGA PIN	Connector
1	3.3V	—	—	—
3	GND	—	—	—
5	PMODD7	B7IO37	F14	P1-B 280
7	PMODD6	B7IO35	F11	P1-B 278
9	PMODD5	B7IO33	E12	P1-B 275
11	PMODD4	B7IO31	E14	P1-B 273

Pin	Function	FPGA	FPGA PIN	Connector
2	3.3V	—	—	—
4	GND	—	—	—
6	PMODD3	B8IO0	G10	P1-B 282
8	PMODD2	B7IO37	G15	P1-B 279
10	PMODD1	B7IO34	E11	P1-B 277
12	PMODD0	B7IO32	E13	P1-B 274

PMOD P18:

Pin	Function	FPGA	FPGA PIN	Connector
1	3.3V	—	—	—
3	GND	—	—	—
5	PMODE7	B8IO7	F9	P1-B 290
7	PMODE6	B8IO5	C10	P1-B 288
9	PMODD5	B8IO3	E10	P1-B 285
11	PMODD4	B8IO1	F10	P1-B 283

Pin	Function	FPGA	FPGA PIN	Connector
2	3.3V	–	–	–
4	GND	–	–	–
6	PMODE3	B8IO38	B10	P1-B 128
8	PMODE2	B8IO6	G9	P1-B 289
10	PMODD1	B8IO4	G11	P1-B 287
12	PMODD0	B8IO2	D10	P1-B 284

Samtec Extension Connector

The MCXLEVK hosts a Tiger Eye TFM-135-02-S-D-LC Samtec extension board-to-board connector. Its pinout is shown in the following table.

Pin	Function	FPGA	Connector	Pin	Function	FPGA	Connector
1	P2IO0	B4IO2	P1-A 27	2	P2IO1	B4IO1	P1-A 28
3	GND	–	–	4	GND	–	–
5	P2IO2	B4IO2	P1-A 30	6	P2IO3	B4IO3	P1-A 31
7	GND	–	–	8	3.3V	–	–
9	P2IO4	B4IO4	P1-A 32	10	P2IO5	B4IO5	P1-A 33
11	P2IO6	B4IN0	P1-A 35	12	P2IO7	B4IN1	P1-A 36
13	P2IO8	B4IO6	P1-A 37	14	P2IO9	B4IO7	P1-A 38
15	P2IO10	B4IO8	P1-A 40	16	P2IO11	B4IO9	P1-A 41
17	GND	–	–	18	3.3V	–	–
19	P2IO12	B4IO10	P1-A 42	20	P2IO13	B4IO12	P1-A 43
21	P2IO14	B4IO13	P1-A 45	22	P2IO15	B4IO13	P1-A 46
23	P2IO16	B4IO14	P1-A 47	24	P2IO17	B4IO15	P1-A 48
25	P2IO18	B4IO16	P1-A 50	26	P2IO19	B4IO17	P1-A 51
27	GND	–	–	28	3.3V	–	–
29	P2IO20	B4IO18	P1-A 52	30	P2IO21	B4IO19	P1-A 53
31	P2IO22	B5IO0	P1-A 55	32	P2IO23	B5IO1	P1-A 56
33	P2IO24	B5IO2	P1-A 57	34	P2IO25	B5IO3	P1-A 58
35	P2IO26	B5IO4	P1-A 60	36	P2IO27	B5IO5	P1-A 61
37	GND	–	–	38	3.3V	–	–
39	P2IO28	B5IO6	P1-A 62	40	P2IO29	B5IO7	P1-A 63
41	P2IO30	B5IO8	P1-A 65	42	P2IO31	B5IO9	P1-A 66
43	P2IO32	B5IO10	P1-A 70	44	P2IO33	B5IO11	P1-A 71
45	P2IO34	B5IO12	P1-A 72	46	P2IO35	B5IO13	P1-A 73
47	GND	–	–	48	3.3V	–	–
49	P2IO36	B5IO36	P1-B 232	50	P2IO37	B7IO16	P1-A 254
51	P2IO38	B7IO17	P1-A 255	52	P2IO39	B7IO18	P1-A 257
53	P2IO40	B7IO19	P1-A 258	54	P2IO41	B7IO20	P1-A 259
55	P2IO42	B7IO21	P1-A 260	56	P2IO43	B7IO22	P1-A 262
57	GND	–	–	58	3.3V	–	–
59	P2IO44	B7IO23	P1-B 263	60	P2IO45	–	–
61	P2IO46	–	–	62	P2IO47	B7IO24	P1-A 264
63	P2IO48	B7IO25	P1-A 265	64	P2IO49	B7IO26	P1-A 267
65	P2IO50	B7IO27	P1-A 268	66	P2IO51	B7IO28	P1-A 269
67	GND	–	–	68	3.3V	–	–
69	P2IO52	B7IO29	P1-A 270	70	P2IO53	B7IO30	P1-A 272

JAE MM70 MxM3 Connector

The MXCL SoM connects to the MCXLEVK Baseboard using The JAE MM70 MxM3 Connector. The MM70-314B2 is designed as card edge connector in SMARC 314 format.

Below are tables with the pins of the connector and their corresponding function.

Pin	FPGA	Function		Pin	FPGA	Function
Connector P1:A						
1	3.3V	–		2	3.3V	–
3	3.3V	–		4	GND	–
5	B3IO0	PHY_RSTN		6	B3IO1	PHY1_CRS
7	B3IO2	PHY1_COL		8	B3IO3	PHY1_TXD3
9	GND	–		10	B3IO4	PHY1_TXD2
11	B3IO5	PHY1_TXD1		12	B3IO6	PHY1_TXD0
13	B3IO7	PHY1_TXEN		14	GND	–
15	B3IO8	PHY1_INTR		16	B3IO9	PHY1_RXDV
17	B3IO10	PHY1_RXD0		18	B3IO11	PHY1_RXD1
19	GND	–		20	B3IO12	PHY1_RXD2
21	B3IO13	PHY1_RXD3		22	B3IO14	PHY1_MDC
23	B3IO15	PHY1_MDIO		24	GND	–
25	B3IN0	PHY1_RXC		26	B3IN1	PHY1_TXC
27	B4IO0	P2IO0		28	B4IO1	P2IO1
29	GND	–		30	B4IO2	P2IO2
31	B4IO3	P2IO3		32	B4IO4	P2IO4
33	B4IO5	P2IO5		34	GND	–
35	B4IN0	P2IO6		36	B4IN1	P2IO7
37	B4IO6	P2IO8		38	B4IO7	P2IO9
39	GND	–		40	B4IO8	P2IO10
41	B4IO9	P2IO11		42	B4IO10	P2IO12
43	B1IO11	P2IO13		44	GND	–
45	B4IO12	P3IO14		46	B4IO13	P2IO15
47	B4IO14	P2IO16		48	B4IO15	P2IO17
49	GND	–		50	B4IO16	P2IO18
51	B4IO17	P2IO19		52	B4IO18	P2IO20
53	B4IO19	P2IO21		54	GND	–
55	B5IO0	P2IO22		56	B5IO1	P2IO23
57	B5IO2	P2IO24		58	B5IO3	P2IO25
59	GND	–		60	B5IO4	P2IO26
61	B5IO5	P2IO27		62	B5IO6	P2IO28
63	B5IO7	P2IO29		64	GND	–
65	B5IO8	P2IO30		66	B5IO9	P2IO31
67	B5IN0	–		68	B5IO1	–
69	GND	–		70	B5IO10	P2IO32
71	B5IO11	P2IO33		72	B5IO12	P2IO34
73	B5IO13	P2IO35		74	GND	–
Connector P1:B						
75	B5IO14	–		76	B5IO15	–
77	B5IO16	–		78	B5IO17	–
79	GND	–		80	B6IO0	HB0RWDS
81	B6IO1	HB0DQ2		82	B6IO2	HB0QQ4
83	B6IO3	HB0DQ3		84	GND	–

continues on next page

Table 2 – continued from previous page

Pin	FPGA	Function	Pin	FPGA	Function
85	B6IO4	HB0DQ0	86	B6IO5	HB0DQ5
87	B6IO6	HB0DQ1	88	B6IO7	HB0DQ7
89	GND	–	90	B6IN0	HB1INT
91	B6IN1	–	92	B6IO8	HB1RWDS
93	B6IO9	HB1DQ2	94	GND	–
95	B6IO10	HB1DQ4	96	B6IO11	HB1DQ3
97	B6IO12	HB1DQ0	98	B6IO13	HB1DQ5
99	GND	–	100	B6IO14	HB1DQ1
101	B6IO15	HB1DQ6	102	B6IO16	HB1DQ7
103	B6IO17	HB1RST	104	GND	–
105	B7IO0	P2IO45	106	B7IO1	P2IO46
107	B7IO2	PHY2_CRS	108	B7IO3	PHY1_COL
109	GND	–	110	B7IO4	PHY2_TXD3
111	B7IO5	PHY2_TXD2	112	B7IO6	PHY2_TXD1
113	B7IO7	PHY2_TXD0	114	GND	–
115	B7IO8	PHY2_TXEN	116	B7IO9	PHY2_TXC
117	B7IO10	PHY2_INTR	118	B7IO11	PHY2_RXC
119	GND	–	120	B7IO12	PHY2_RDV
121	B7IO13	PHY2_RXD0	122	B7IO14	PHY2_RXD1
123	B7IO15	PHY2_RXD2	124	GND	–
125	B7IO38	PHY2_RXD3	126	B7IN0	PHY2_MDC
127	B7IN1	PHY2_MDIO	128	B8IO38	PMODE3
129	GND	–	130	B8IN0	–
131	B8IN1	–	132	B8IO20	–
133	B8IO21	–	134	GND	–
135	B8IO22	–	136	B8IO23	–
137	B8IO24	–	138	B8IO25	–
139	GND	–	140	B8IO26	–
141	B8IO27	–	142	B8IO28	–
143	B8IO29	–	144	GND	–
145	B8IO30	–	146	B8IO31	–
147	B8IO32	–	148	B8IO33	–
149	GND	–	150	B8IO34	–
151	B8IO35	DS28IO	152	B8IO36	–
153	B8IO37	G7	154	GND	–
155	HW_RST	–	156	GND	–
Connector P1:A					
157	3.3V	–	158	3.3V	–
159	3.3V	–	160	3.3V	–
161	GND	–	162	–	–
163	–	–	164	–	–
165	–	–	166	3.3V	–
167	–	–	168	–	–
169	–	–	170	–	–
171	3.3V	–	172	–	–
173	–	–	174	–	–
175	–	–	176	3.3V	–
177	–	–	178	–	–
179	–	–	180	–	–

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Table 2 – continued from previous page

Pin	FPGA	Function	Pin	FPGA	Function
181	3.3V	–	182	–	–
183	–	–	184	–	–
185	–	–	186	3.3V	–
187	B4IO20	LED1	188	B4IO21	LED2
189	B4IO22	LED3	190	B4IO23	LED4
191	3.3V	–	192	B4IO24	LED5
193	B4IO25	LED6	194	B4IO26	LED7
195	B4IO27	LED8	196	3.3V	–
197	B4IO28	PMODB4	198	B4IO29	PMODB0
199	B4IO30	PMODB5	200	B4IO31	PMODB1
201	3.3V	–	202	B4IO32	PMODB6
203	B4IO33	PMODB2	204	B4IO334	PMODB7
205	B4IO35	PMODB3	206	3.3V	–
207	B4IO36	BUTTON2	208	RST	BUTTON1
209	B5IO18	BUTTON3	210	B5IO19	BUTTON4
211	GND	–	212	B5IO20	PMODA3
213	B5IO21	PMODA7	214	B5IO22	PMODA2
215	B5IO23	PMODA6	216	3.3V	–
217	B5IO24	PMODA1	218	B5IO25	PMODA5
219	B5IO26	PMODA0	220	B5IO27	PMODA4
221	3.3V	–	222	B5IO28	PMODC4
223	B5IO29	PMODC0	224	B5IO30	PMODC5
225	B5IO31	PMODC1	226	3.3V	–
227	B5IO32	PMODC6	228	B5IO33	PMODC2
229	B5IO34	PMODC7	230	B5IO35	PMODC3
231	3.3V	–	232	B5IO36	P2IO36
Connector P1:B					
233	B6IO34	HBOINT	234	B6IO18	HBOCS1
235	B6IO19	HB0CS0	236	1.8V	–
237	B6IO20	HB0CK1	238	B6IO21	HB0CK1
239	B6IO22	HBOCK0	240	B6IO23	HBOCK0
241	1.8V	–	242	B6IO24	HB0DQ6
243	B6IO25	HB0RST	244	B6IO26	HB1CK1
245	B6IO27	HB1CK1	246	1.8V	–
247	B6IO28	HB2CS1	248	B6IO29	HB1CK0
249	B6IO30	HB1CK0	250	B6IO31	HB1CS0
251	1.8V	–	252	B6IO32	–
253	B6IO33	–	254	B7IO16	P2IO37
255	B7IO17	P2IO38	256	GND	–
257	B7IO18	P2IO39	258	B7IO19	P2IO40
259	B7IO20	P2IO41	260	B7IO21	P2IO42
261	3.3V	–	262	B7IO22	P2IO43
263	B7IO23	P2IO44	264	B7IO24	P2IO47
265	B7IO25	P2IO48	266	3.3V	–
267	B7IO26	P2IO49	268	B7IO27	P2IO50
269	B7IO28	P2IO51	270	B7IO29	P2IO52
271	3.3V	–	272	B7IO30	P2IO53
273	B7IO31	PMODD4	274	B7IO32	PMODD0
275	B7IO33	PMODD5	276	3.3V	–

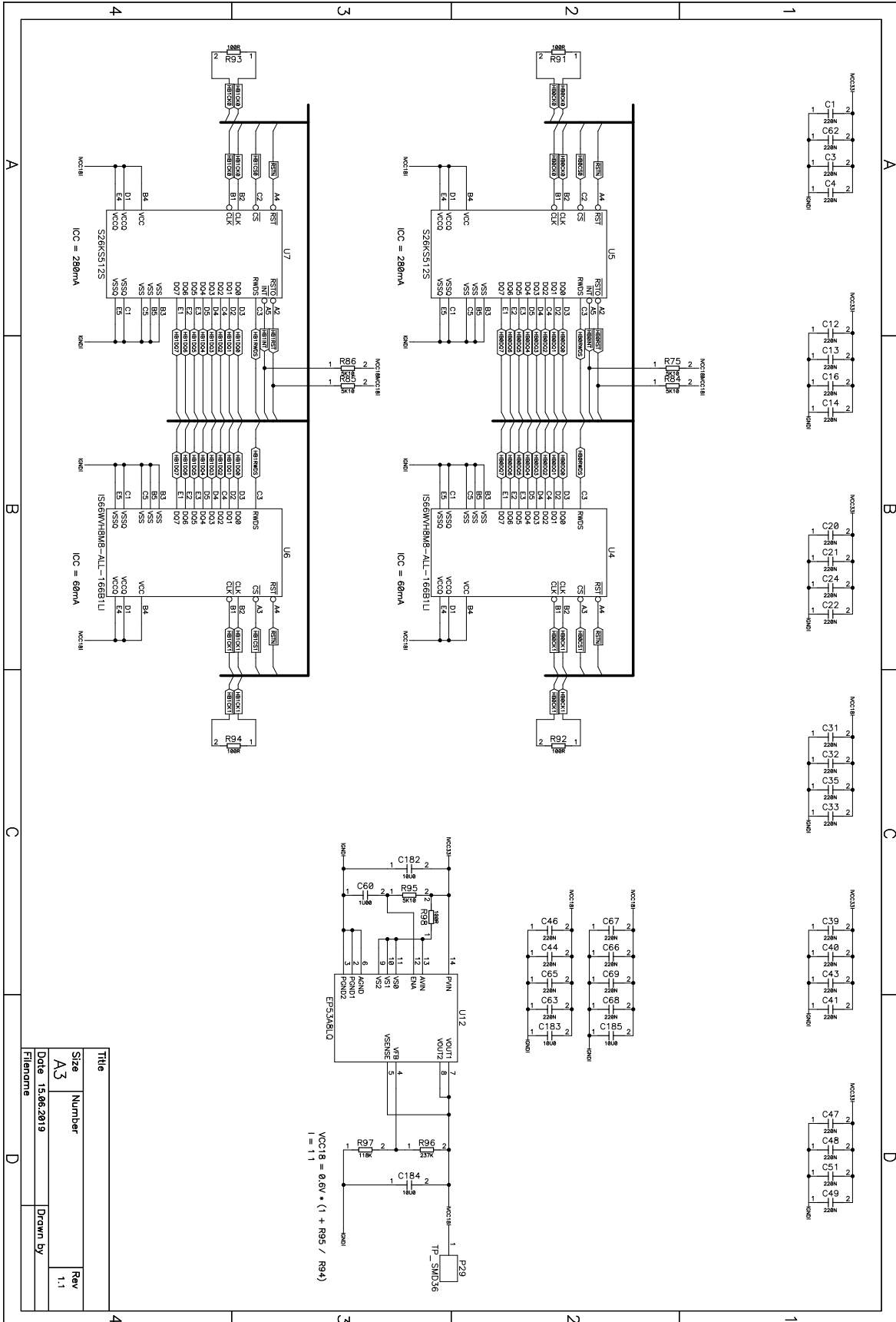
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Table 2 – continued from previous page

Pin	FPGA	Function		Pin	FPGA	Function
277	B7IO34	PMODD1		278	B7IO35	PMODD6
279	B7IO36	PMODD2		280	B7IO37	PMODD7
281	GND	–		282	B8IO0	PMODD3
283	B8IO1	PMODD4		284	B8IO2	PMODE0
285	B8IO3	PMODE5		286	3.3V	–
287	B8IO4	PMODE1		288	B8IO5	PMODE6
289	B8IO6	PMODE2		290	B8IO7	PMODE7
291	3.3V	–		292	B8IO8	–
293	B8IO9	–		294	B8IO10	–
295	B8IO11	–		296	3.3V	–
297	B8IO12	–		298	B8IO13	–
299	B8IO14	–		300	B8IO15	–
301	3.3V	–		302	B8IO16	–
303	B8IO17	–		304	B8IO18	–
305	B8IO19	–		306	3.3V	–
307	B1IO0	–		308	B1IO1	–
309	B1IO2	–		310	B1IO3	–
311	GND	–		312	B1IO4	–
313	B1IO5	–		314	GND	–

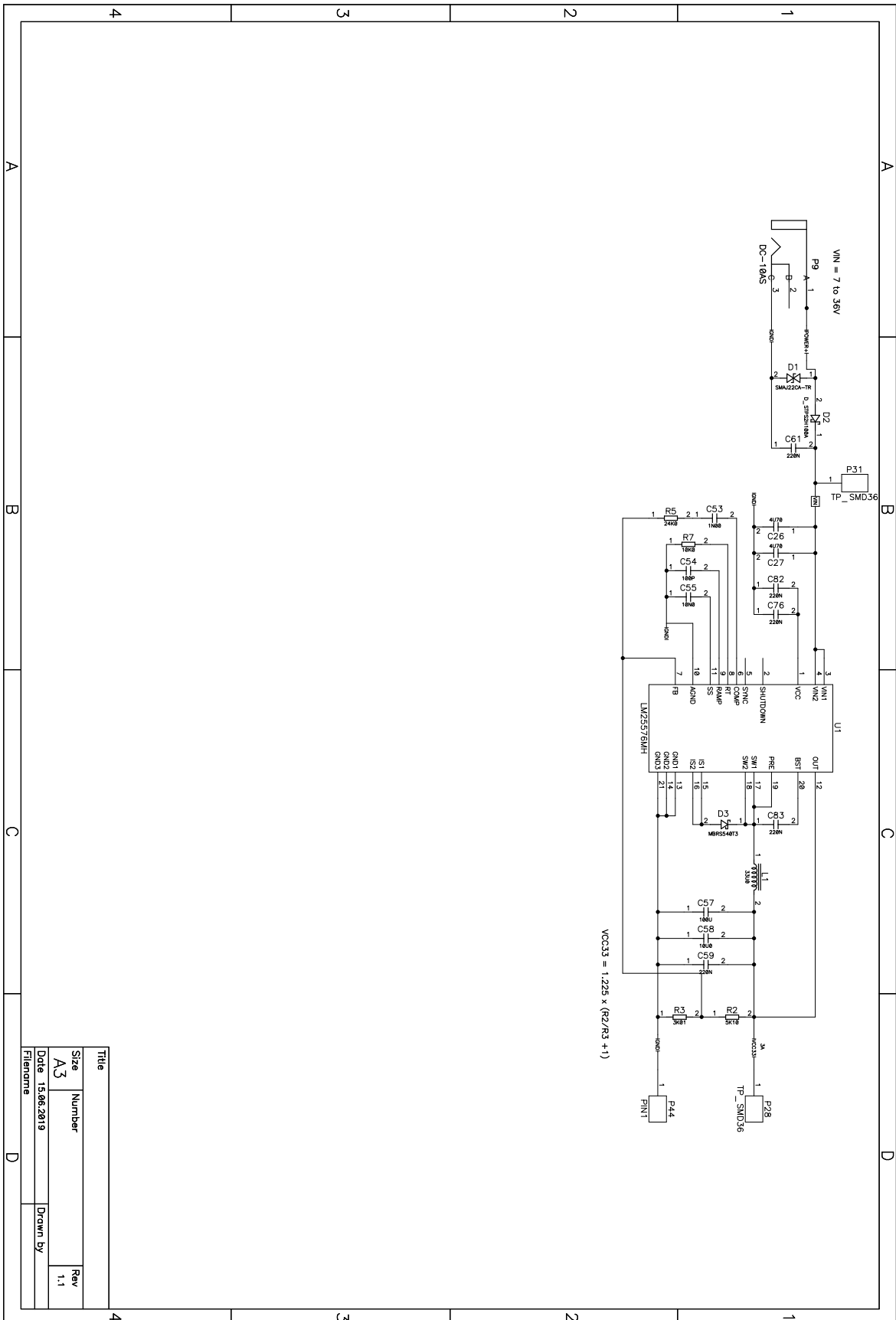
APPENDIX

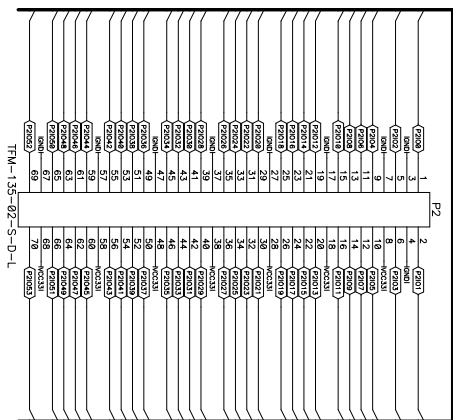
Schematics

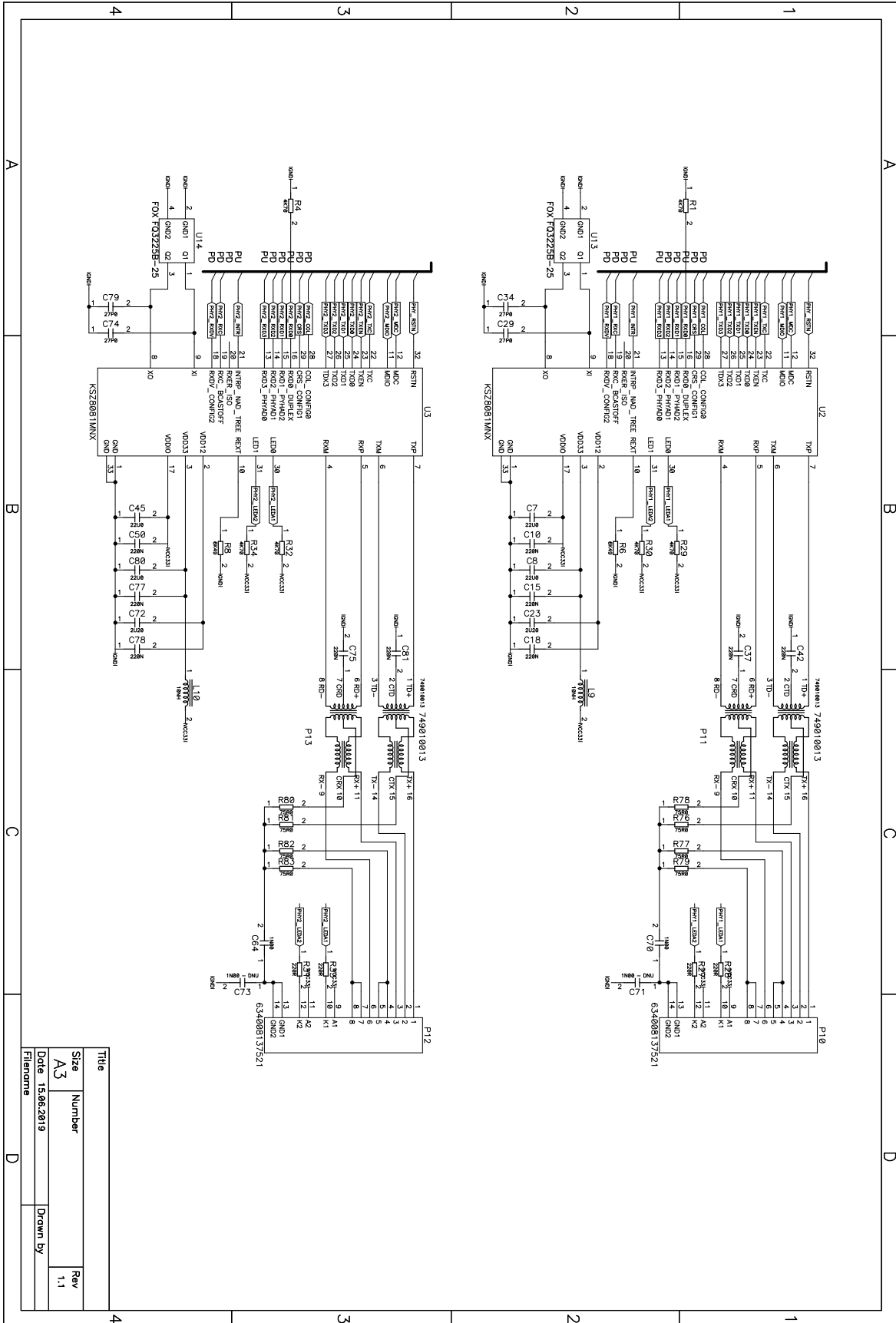


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Size	Number	Rev
A3		1.1
Date	15.06.2019	Drawn by
Filename		

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					MCX33 2	CC33 159	MCX33 160	MCX33 161				
					MCX33 3	CC33 161	MCX33 162	MCX33 163				
3	A	B	C	D	P1-B							
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					MCX33 5	CC33 165	MCX33 166	MCX33 167				
					MCX33 6	CC33 167	MCX33 168	MCX33 169				
2	A	B	C	D	P1-C							
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					MCX33 9	CC33 173	MCX33 174	MCX33 175				
1	A	B	C	D	P1-D							
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					MCX33 12	CC33 179	MCX33 180	MCX33 181				
					P1-E							
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4.1 Layout Diagram

