MCV Hardware Manual

Version: **1.5**

Created on: October 20, 2023

Created by: ARIES Embedded GmbH

CONTENTS:

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

Adress:

ARIES Embedded GmbH

Schöngeisinger Str. 84

D-82256 Fürstenfedbruck

Germany

Phone:

+49 (0) 8141/36 367-0

Fax:

+49 (0) 8141/36 367-67

1.2 Disclaimer

ARIES Embedded does not guarantee that the information in this document is up-to-date, correct, complete or of good quality. Liability claims against ARIES Embedded, referring to material or non-material related damages caused, due to usage or non-usage of the information given in this document, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of ARIES Embedded. ARIES Embedded explicitly reserves the rights to change or add to the contents of this Preliminary User's Manual or parts of it without notification.

1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	28.05.2015	aw	Initial creation
1.1	04.07.2016	aw	Transition to pdf documentation Inserted 'Care and Maintenance'
1.2	09.03.2017	aw	Updated data for connector location
1.3	06.06.2017	bnh	Corrected pinout
1.4	20.09.2022	dk	Corrected pinout
1.4.1	14.10.2022	dk	Connector Location added
1.5	20.10.2023	js	Updated clocking, gpio, images Minor corrections

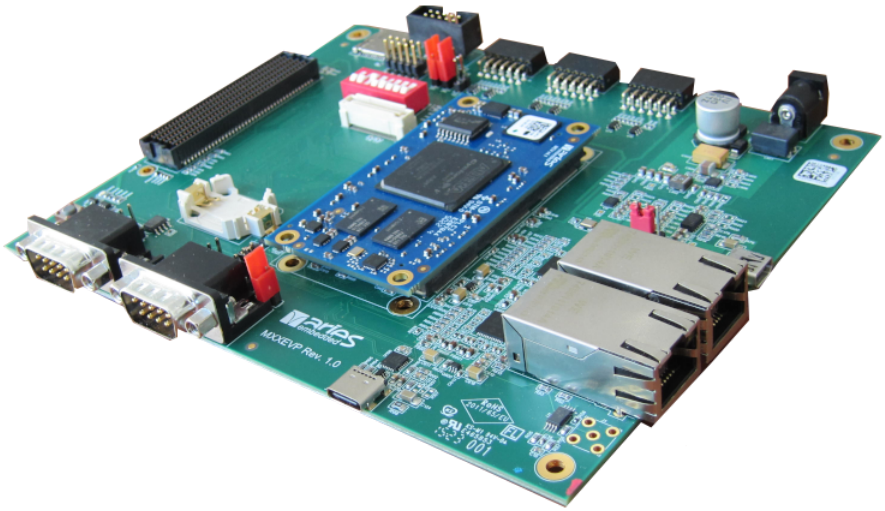
CHAPTER

TWO

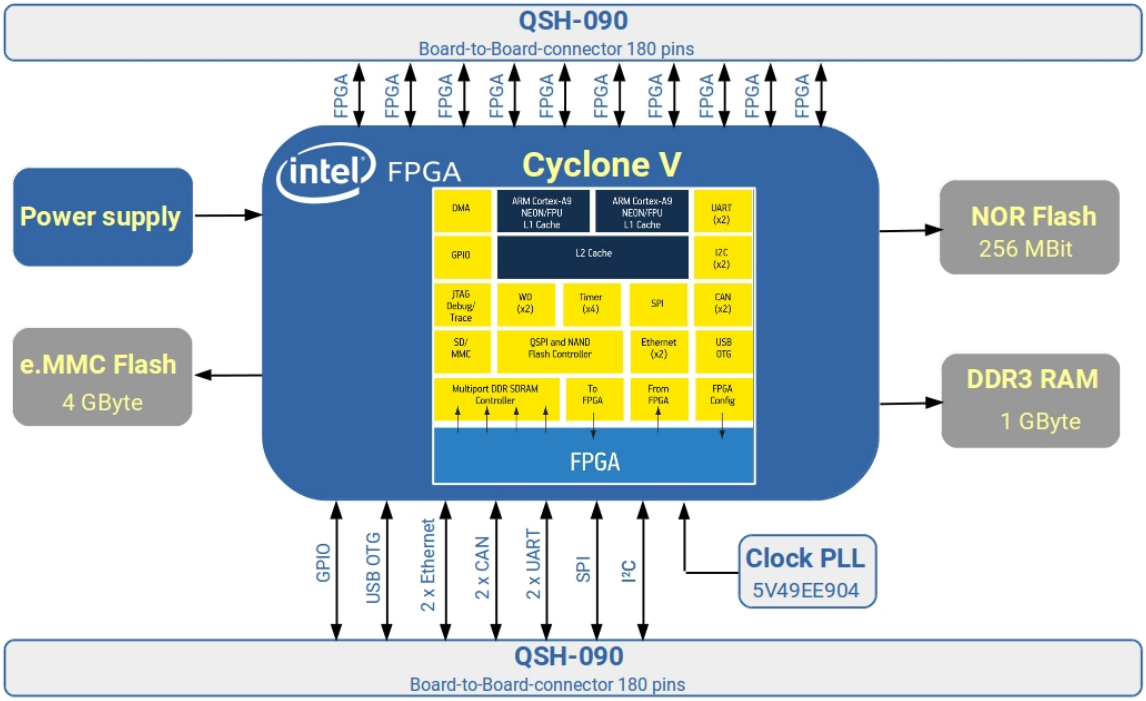
OVERVIEW

2.1 MCV

The MCV System on Module is a credit card size industrial module based on the Altera Cyclone V SoC device. MCV offers full flexibility for most projects in industrial, medical or avionics environment. To enable a seamless integration MCV features different derivatives of the MCV SoC FPGA, eMMC memory as well as DDR3 RAM. All necessary supply voltages are generated on the System on Module so that it is sufficient to provide the 3V3 power supply voltage as well as a ground signal to it.

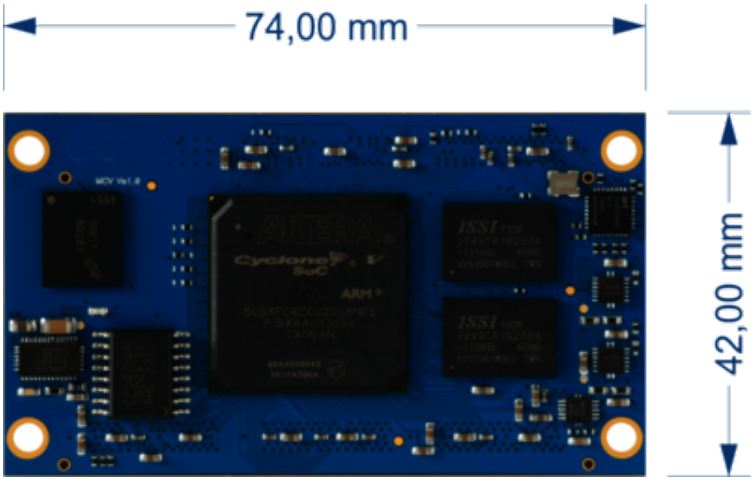


2.2 Block Diagram

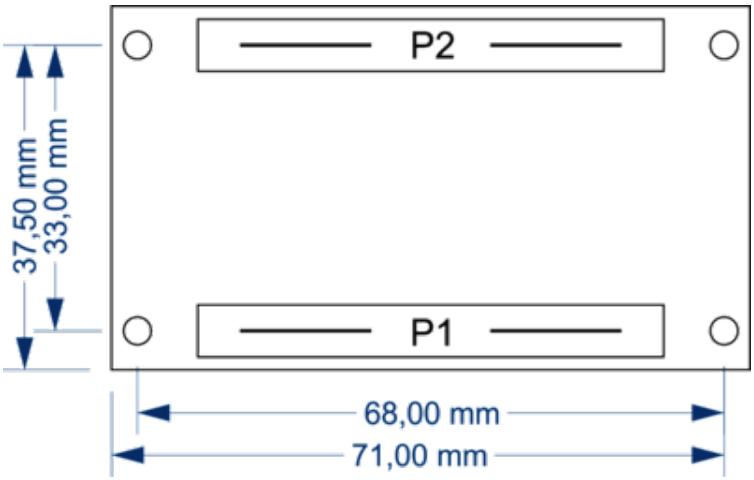


2.3 Dimensions

The total board dimensions of MCV are as follows:



The board mounting holes and connectors are located as shown in the following figure:



The mounting holes are suitable for M3 screws.

2.4 Feature Set

The MCV System on Module features:

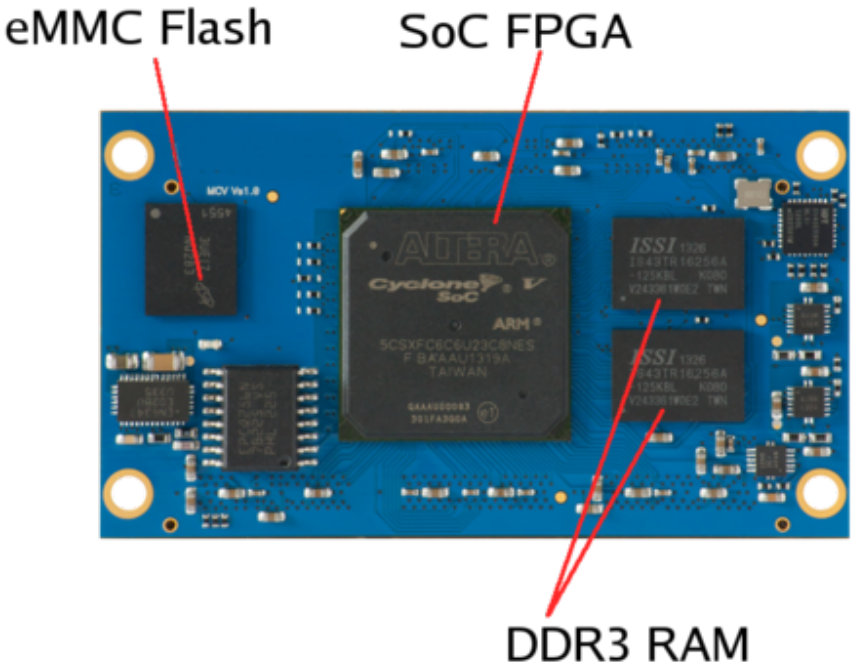
- **Altera Cyclone V SoC FPGA**
  - **without PCIe support**
    - A2: 5CSEBA2U23C8N, 25KLE, 36 DSP blocks
    - A4: 5CSEBA4U23C8N, 40KLE, 58 DSP blocks
    - A5: 5CSEBA5U23C8N, 85KLE, 87 DSP blocks
    - A6: 5CSEBA6U23C8N, 110KLE, 112 DSP blocks
  - **with PCIe support**
    - A2: 5CSXFC2C6U23C7N, 25KLE, 36 DSP blocks, 6 transceivers 2.5 Gbit/s
    - A4: 5CSXFC4C6U23C7N, 40KLE, 58 DSP blocks, 6 transceivers 2.5 Gbit/s
    - A5: 5CSXFC5C6U23C7N, 85KLE, 87 DSP blocks, 6 transceivers 2.5 Gbit/s
    - A6: 5CSXFC6C6U23C7N, 110KLE, 112 DSP blocks, 6 transceivers 2.5 Gbit/s
- Dual 800 MHz Cortex A9 Cores
- HPS-Peripherals
- 1 GByte DDR3 Memory
- 256 Mbit Configuration Device
- 4GByte eMMC memory
- 143 FPGA signals
- 66 HPS signals
- Clock distribution

2.5 Part Label

The MCV part-label is located at the eMMC NAND flash component:

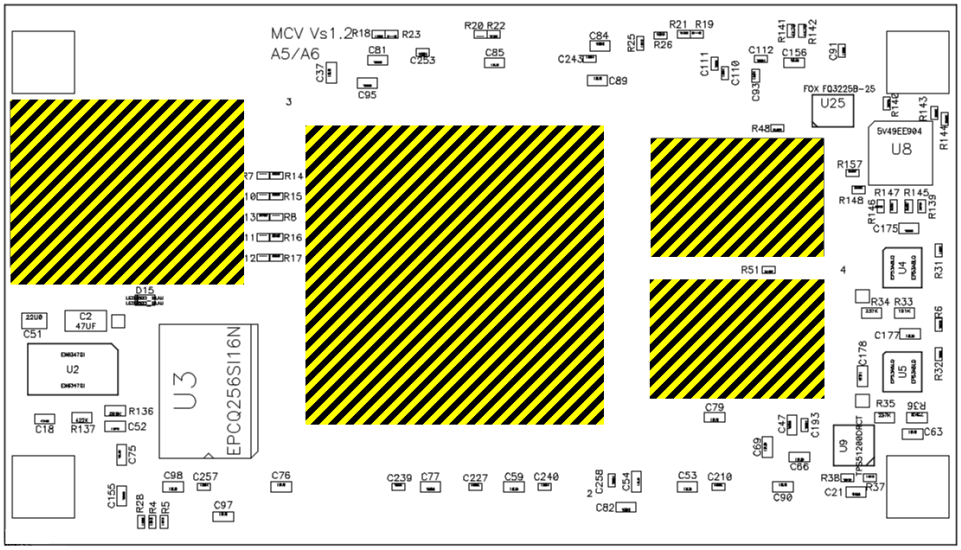
The MCV part label supplies the product information as follows:

2.6 Parts Overview



2.7 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on MCV it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

RESOURCES

3.1 Components

3.1.1 SoC-FPGA

Altera's Cyclone V SoCs provide the industry's lowest system cost and power, along with performance levels you need to differentiate your high-volume applications.

Device	All Cyclone V SoC Devices (SE, SX, ST)
CPU core	ARM Cortex™-A9 MPCore™ processor with ARM CoreSight™ debug and trace technology (single and dual-core variants) • 925 MHz CPU clock rate in -C6 speed grade • 800 MHz CPU clock rate in -C7, -I7 speed grades • 700 MHz CPU clock rate in -A7 speed grade • 600 MHz CPU clock rate in -C8 speed grade
Coprocessors	ARM Neon media processing engine with vector floating-point (VFP) v3 double-precision floating-point unit for each processor, snoop control unit (SCU), acceleration coherency port (ACP)
Layer 1 cache	32 KB L1 instruction cache, 32 KB L1 data cache
Layer 2 cache	512 KB shared L2 cache
On-chip memory	64 KB on-chip RAM, 64 KB on-chip ROM
HPS hard memory controller	Multiport SDRAM controller with support for DDR2, DDR3, DDR3L and LPDDR2 with optional error correction code (ECC) support 400 MHz/800 Mbps external memory interface User-configurable memory width of 8, 16, 16+ECC, 32, 32+EEC Up to 4 GB address range with built-in memory protection control
Quad serial peripheral interface (SPI) flash controller	Supports SPIx1, SPIx2, or SPIx4 (quad SPI) serial NOR flash devices Up to 4 chip selects
SD/SDIO/MMC controller	Supports SD, eSD, SDIO, eSDIO, MMC, eMMC, and CE-ATA with integrated DMA
NAND flash controller	Supports 8 bit ONFI 1.0 NAND flash devices Programmable-hardware ECC for single-level cell (SLC) and multilevel cell (MLC) devices
Ethernet media access controller (EMAC)	2 x 10/100/1000 EMAC with RGMII external PHY interface and integrated DMA
USB On-The-Go controller	2 x USB 2.0 OTG controllers with ULPI external PHY interface and integrated DMA
(OTG)	–
UART controller	2 x UART 16550 compatible
SPI controller	2 x SPI masters 2 x SPI slaves
I2C controller	4 x I2C
CAN controller	2 x CAN Protocol specification 2.0 (A and B)
General-purpose I/O (GPIO)	Up to 71 GPIO and 14 input-only pins, with digital de-bounce and configurable interrupt mode
Direct memory access (DMA) controller	8-channel DMA Supports flow control with 31 peripheral handshake interfaces
Timers	Private interval and watchdog timer for each processor Global timer for processor subsystem 4 X general-purpose timers 2 X watchdog timers
HPS phased-lock loops (PLLs)	3
Maximum HPS I/O	181

More information is available on the Altera Website.

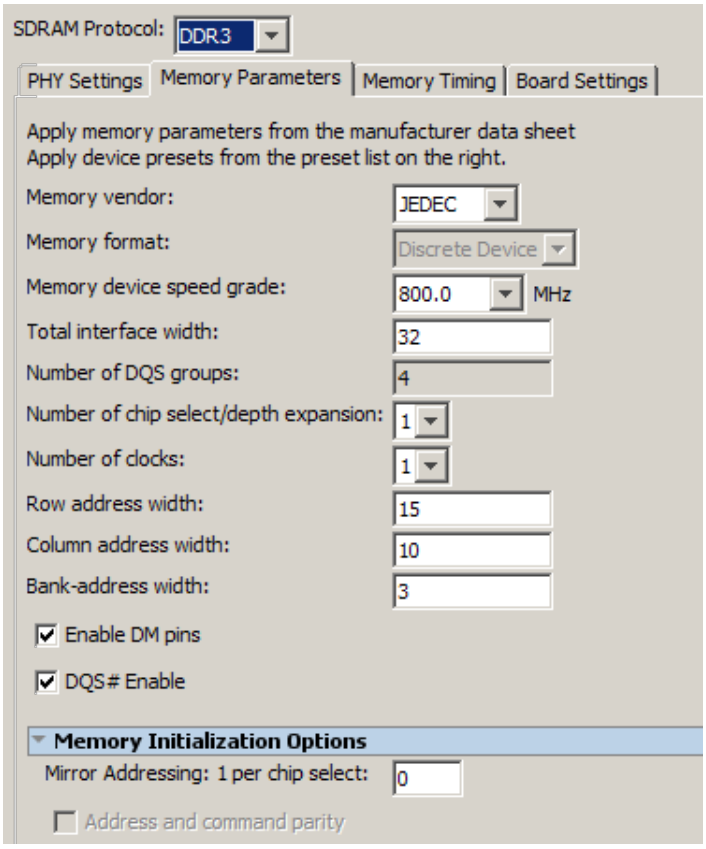
Cyclone V SoC FPGA derivatives on MCV

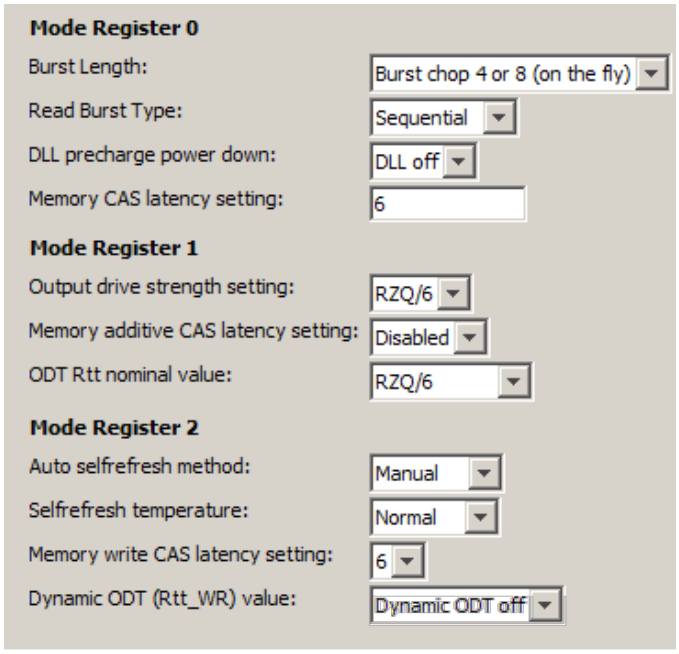
MCV supports the following Cyclone V SoC FPGA derivatives:

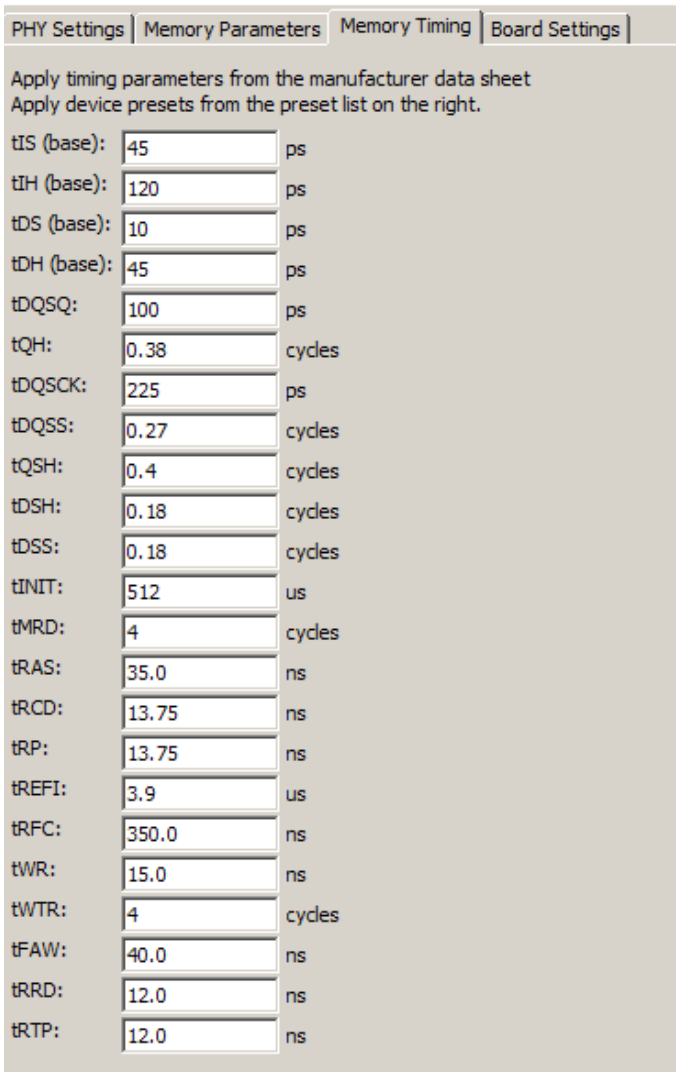
Without PCIe Support		With PCIe Support	
5CSEBA2U23C8N	25KLE, 36 DSP blocks	5CSXFC2C6U23C7N	25KLE, 36 DSP blocks, 6 transceivers 2.5Gbit/s
5CSEBA4U23C8N	40KLE, 58 DSP blocks	5CSXFC4C6U23C7N	40KLE, 58 DSP blocks, 6 transceivers 2.5Gbit/s
5CSEBA5U23C8N	85KLE, 87 DSP blocks	5CSXFC5C6U23C7N	85KLE, 87 DSP blocks, 6 transceivers 2.5Gbit/s
5CSEBA6U23C8N	110KLE, 112 DSP blocks	5CSXFC6C6U23C7N	110KLE, 112 DSP blocks, 6 transceivers 2.5Gbit/s

3.1.2 DDR3 RAM

MCV is equipped with 2 pieces K4B4G1646D-BIK0000 resulting in 1GByte of DDR3 memory and a bus width of 32 bit. The memory interface is clocked at 400 MHz using the 1.5V DDR3 standard. Figure shows the memory settings in QSys. A Preset is available for all the memory settings for the MCV module:




Mode Register 0
Burst Length:
Burst chop 4 or 8 (on the fly)
Read Burst Type:
Sequential
DLL precharge power down:
DLL off
Memory CAS latency setting:
6
Mode Register 1
Output drive strength setting:
RZQ/6
Memory additive CAS latency setting:
Disabled
ODT Rtt nominal value:
RZQ/6
Mode Register 2
Auto selfrefresh method:
Manual
Selfrefresh temperature:
Normal
Memory write CAS latency setting:
6
Dynamic ODT (Rtt_WR) value:
Dynamic ODT off


PHY Settings
Memory Parameters
Memory Timing
Board Settings
Apply timing parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
tIS (base): 45 ps
tIH (base): 120 ps
tDS (base): 10 ps
tDH (base): 45 ps
tDQSQ: 100 ps
tQH: 0.38 cycles
tDQSCK: 225 ps
tDQSS: 0.27 cycles
tQSH: 0.4 cycles
tDSH: 0.18 cycles
tDSS: 0.18 cycles
tINIT: 512 us
tMRD: 4 cycles
tRAS: 35.0 ns
tRCD: 13.75 ns
tRP: 13.75 ns
tREFI: 3.9 us
tRFC: 350.0 ns
tWR: 15.0 ns
tWTR: 4 cycles
tFAW: 40.0 ns
tRRD: 12.0 ns
tRTP: 12.0 ns

3.1.3 eMMC NAND Flash

MCV supports in its standard version 4GByte of eMMC NAND memory. The THGBMDG5D1LBAIT component by Toshiba/Kioxia is a 32GBit MLC NAND Flash in 15nm technology. More information could be requested on the Toshiba/Kioxia Website.

The following table shows the connection between eMMC and SoC FPGA:

Function	FPGA Pin
SDIO_CMD	D14
SDIO_D0	C13
SDIO_D1	B6
SDIO_D2	B11
SDIO_D3	B9
SDIO_D4	H13
SDIO_D5	A4
SDIO_D6	H12
SDIO_D7	B4
HPS_SDIO_CLK	B8

3.1.4 EPCQ Flash

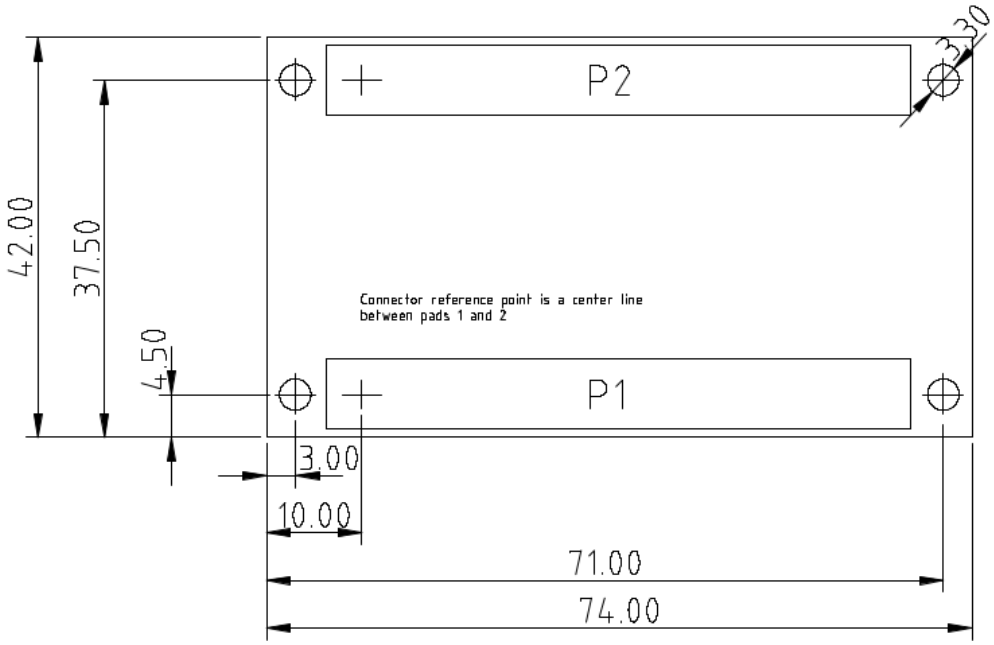
A 256Mbit QSPI Flash device is connected to the configuration interface of the FPGA. Using an Active Serial (AS) configuration scheme, the FPGA configures out of this EPCQ Flash.

The EPCQ flash is connected as follows:

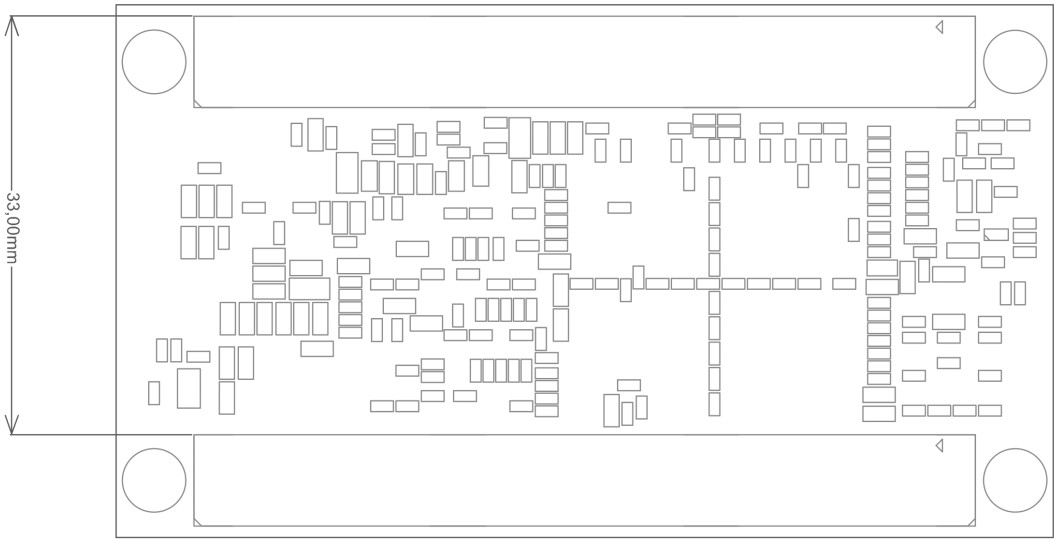
Function	FPGA Pin
CSOn	AA6
DCLK	AA8
DATA0	AD7
DATA1	AC6
DATA2	AC5
DATA3	AB6

3.1.5 Connectors

MCV supplies its signals on two Samtec QSH-090-01-F-D-A connectors.



Connector Location:



Connector Features:

- 0,50 mm (.0197") pitch
- 5,00 mm - 30,00 mm stack heights
- Plating: Au or Sn over 50micro" (1,27 microm) Ni
- **Current Rating:**
  - Contact: 2 A per pin (1 pin powered per row)
  - Ground Plane: 25 A per ground plane (1 ground plane powered)
- Operating Temp Range: -55°C to +125°C
- Voltage Rating: 125 VAC (5 mm Stack Height)
- Max Cycles: 100
- Insulator Material: Liquid Crystal Polymer
- Contact Material: Phosphor Bronze
- RoHS Compliant: Yes

More information on the connectors is available on the Samtec website.

3.2 Boot Options

MCV is configured to boot from eMMC flash memory.

Six resistors on the module provide the selection of the BSEL signals of the SoC FPGA. During reset of the SoC FPGA the BSEL pins are monitored by the SOC FPGA and can be used for different purpose after booting.

BSEL [2..0]	Boot Source	Resistors
001	FPGA	R19 R18 R22
101	emmc	R21 R18 R22

The SoC FPGA can be configured using the onboard QSPI flash in Active Serial (AS) mode or using the HPS. The default boot mode is FPP16 Standard – the HPS will configure the FPGA. The MSEL pins have to be set accordingly as follows:

MSEL[5..0]	Boot Source	Resistors
00000	FPP16 Fast	R14 R15 R8 R16 R17
00100	FPP16 Standard	R14 R15 R13 R16 R17
00001	FPP16 Security, Fast	R14 R15 R8 R16 R12
00101	FPP16 Security, Standard	R14 R15 R13 R16 R12
00010	FPP16 Compression, Security, Fast	R14 R15 R8 R11 R17
00110	FPP16 Compression, Security, Standard	R14 R15 R13 R11 R17
10010	AS Fast	R7 R15 R8 R11 R17
10011	AS Standard	R7 R15 R8 R11 R12

The MSEL settings for Cyclone V devices are given as follows:

Configuration Scheme	Compression Feature	Design Security Feature	V_{CCPGM} (V)	Power-On Reset (POR) Delay	Valid MSEL[4..0]
FPP x8	Disabled	Disabled	1.8/2.5/3.0/3.3	Fast	10100
				Standard	11000
	Disabled	Enabled	1.8/2.5/3.0/3.3	Fast	10101
				Standard	11001
	Enabled	Enabled/Disabled	1.8/2.5/3.0/3.3	Fast	10110
				Standard	11010
FPP x16	Disabled	Disabled	1.8/2.5/3.0/3.3	Fast	00000
				Standard	00100
	Disabled	Enabled	1.8/2.5/3.0/3.3	Fast	00001
				Standard	00101
	Enabled	Enabled/Disabled	1.8/2.5/3.0/3.3	Fast	00010
				Standard	00110
PS	Enabled/Disabled	Enabled/Disabled	1.8/2.5/3.0/3.3	Fast	10000
				Standard	10001
AS (x1 and x4)	Enabled/Disabled	Enabled/Disabled	3.0/3.3	Fast	10010
				Standard	10011
JTAG-based configuration	Disabled	Disabled	—	—	Use any valid MSEL pin settings above

3.3 Clocking

Version 3.0

The clock scheme of the MCV module is based on the IDT programmable clock generator 5V49EE904. The 5V49EE904 is sourced from a 25MHz crystal. The device provides a 25MHz Clock to the HPS and two 50MHz clock signals to the FPGA. Two differential Clock outputs (A,B and C,D) are available on P2 together with the power supply signals (IDTV4, IDTV5). Two additional 3.3V Clock signals are also routed to connector P2. The I^2C interface signals and the Select signals are available on the connector P2, too.

Version 4.0

The clock scheme of the MCV module is based on the 5P35023 VersaClock programmable clock generator. The 5P35023 device is a three PLL architecture design, and each PLL is individually programmable and allowing for up to five unique frequency outputs. The 5P35023 has built-in unique features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshot Reduction Technology (ORT) and Extreme Low Power DCO. An internal OTP memory allows the user to store the configuration in the device without programming after power up, then program the 5P35023 again through the I2C interface.

- New clock chip does not have EEPROM and can not store different configurations. IDT_SELx pins are not used any more, IDTV5 and CLKEXTC, CLKEXTD clocks are not available in V4.0.
- New clock chip offers the OTP memory, but it is not system programmable and needs to be programmed before the assembly. Non programmed IC is assembled on MCV 4.0.
- Prog pin (J2-169) is connected but does not have any function.
- It can be reprogrammed in system with I2C, but it needs to be reprogrammed every time after cold start. HPS clock is available on blank device, so it is possible to program chip in U-Boot or Linux
- The factory image uses the preloader to program the clock chip, then issues a warm reset. This ensures that the Ethernet clock is running when the PHYs of the MCVEVP are initializing.

A copy of the configuration-file which is programmed on MCV by default can be obtained on request.

3.3.1 Clock Driver Outputs

The clock driver outputs are provided as follows:

Version 3.0

IO-pin	Clock	Frequency	Voltage
30 / Out0	CLKextE	–	3.3V
7 / Out1	CLK50A	50MHz	VCCIO8A
8 / Out2	CLK50B	50MHz	VCCIO8A
24 / Out3	CLKextF	–	3.3V
10 / Out4	CLKextA	–	IDTV4
11 / Out4B	CLKextB	–	IDTV4
14 / Out5	CLKextC	–	IDTV5
15 / Out5B	CLKextD	–	IDTV5
23 / Out6	CLK25HPS	25MHz	3.3V

Version 4.0

IO-pin	Clock	Frequency	Voltage
DIFF2/24	CLKEXTE	–	3.3V
SE2/12	CLK50A	programmable	VCCIO8A
SE3/19	CLK50B	programmable	VCCIO8A
DIFF2B/23	CLKEXTF	–	3.3V
DIFF1/18	CLKEXTA	–	IDTV4
DIFF1B/17	CLKEXTB	–	IDTV4
REF/8	CLK25HPS	25MHz	3.3V

Important: For MCV v4.0 and later it is required to supply the clock generator with all voltages. This concerns especially IDTV4 (Pin J2-164, 2.5V or 3.3V), even if the corresponding differential clock (CLKEXTA, CLKEXTB) is not used. Otherwise the clock generator will not start at all.

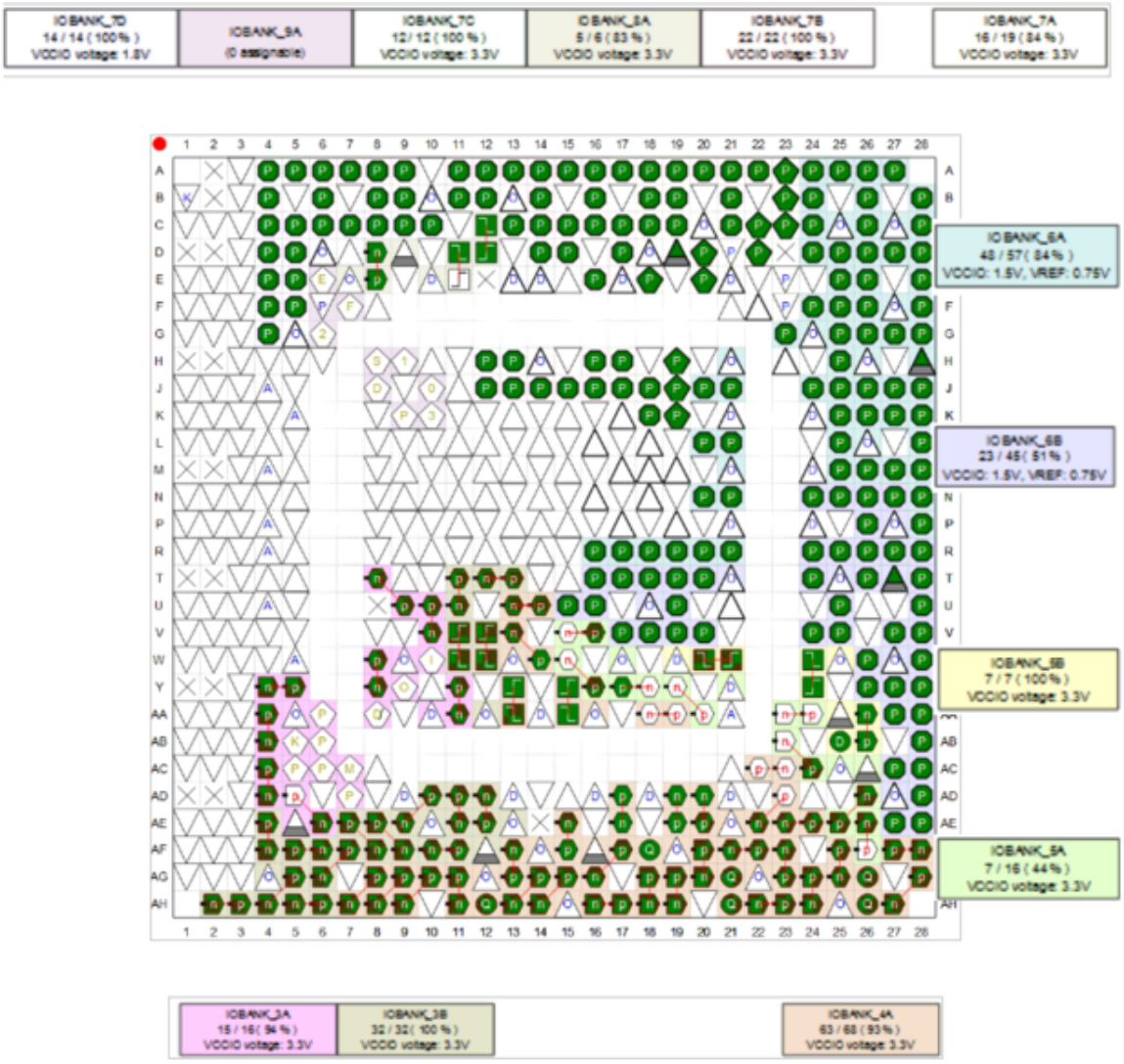
3.3.2 FPGA Clock Sources

The Clocks are supplied to the SoC FPGA as specified below:

Function	FPGA Pin	FPGA Signal
–	C12	CLK50A
–	D12	CLK50B
25MHz	E20	HPS-Clock1
25MHz	D20	HPS-Clock2

3.4 I/O Banks

The following image shows an overview of the FPGA I/O banks:



3.4.1 I/O Bank Voltages

The following table shows the voltages of the IO-Banks. Make sure that the corresponding VCCPD Pins are connected respective the information in Table. Several IO-Banks are connected to supply rails directly, other IO-Banks are powered externally via the connectors to allow the full flexibility of IO-Standards. For more information of the I/O Standards refer to Table 5-9 in the Cyclone V Datasheet.

IO-Bank	Voltage	VCCPD	VREF
3A	3.3V	3.3V	
3B	VCCIO3B	VC-CPD3B4A	
4A	VCCIO4A	VC-CPD3B4A	
5A	VCCIO5A	VCCPD5A	
5B	VCCPD8A	VCCPD8A	
6A	1.5V	2.5V	0.75V
6B	1.5V	2.5V	0.75V
7A	3.3V	3.3V	
7B	VCCIO7B	VCCPD7B	
7C	3.3V	3.3V	
7D	VCCIO7D	VCCPD7D	
8A	VCCIO8A	VCCPD8A	

The VCCPD pins have to be powered respective to the Voltage of the IO-Bank:

Bank Voltage	VCCPD
3.3V	3.3V
3.0V	3.0V
2.5V	2.5V
1.8V	2.5V
1.5V	2.5V
1.2V	2.5V

3.5 JTAG

The JTAG connection of HPS and FPGA are connected in a chain. The JTAG Signals are located in IO-Bank 3A and 7A, both connected to 3.3V. The JTAG pins are available on the following pins con connector P1:

Function	Pin	Pin	Function
VCC33	1	2	GND
VCC33	3	4	TDO
VCC33	5	6	TCK
VCC33	7	8	TDI
VCC33	9	10	TMS

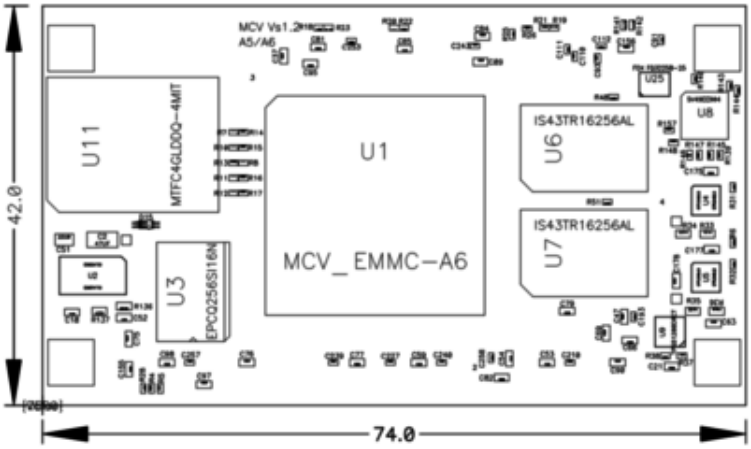
3.6 Pin Out

On MCV the Pin multiplexing can be set to the requirements of the application.

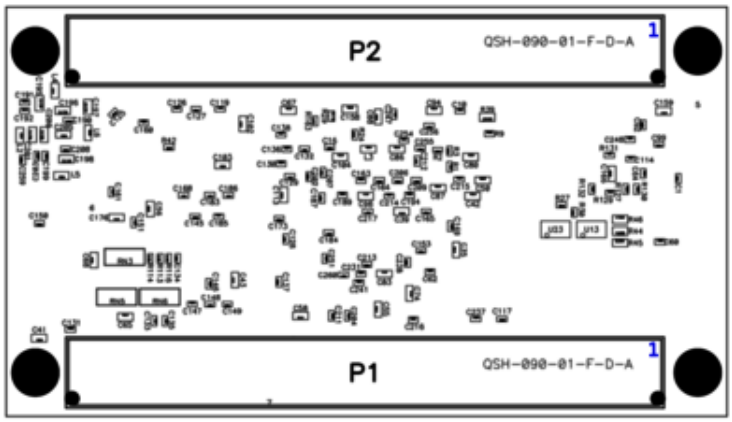
The eMMC flash is mandatory as it is connected on the System on Module. All other signals are routed to the connector P2. The power supply of IOBANK 7B and 7D has to be sourced from the baseboard, according to the selected IO-Standards.

Important: On MCV v4.0 and later the clock chip is required to be programmed via I2C (IDT_SDAT on J2-165, IDT_SCLK on J2-167). These pins are no longer available as GPIO.

MCV top view:



MCV bottom view:



3.6.1 Connector P1

Function	FPGA	Pin	Pin	FPGA	Function
VCC33	–	1	2	–	GND
VCC33	–	3	4	–	TDO
VCC33	–	5	6	–	TCK
VCC33	–	7	8	–	TDI
VCC33	–	9	10	–	TMS
VCC33	–	11	12	–	VCCPD8A
VCCIO8A	–	13	14	xx	IOB5B5
IOB8A3	D8	15	16	xx	IOB5B4
IOB8A2	E8	17	18	xx	IOB5B3
IOB8A1	D11	19	20	xx	IOB5B2
IOB8A0	E11	21	22	xx	IOB5B1
VCCIO8A	–	23	24	xx	IOB5B0
VCC33	25	26	–	–	VCCPD8A
IOB3A15	T8	27	28	Y11	IOB3A7
IOB3A14	U9	29	30	AA11	IOB3A6
IOB3A13	V10	31	32	AD5	IOB3A5
IOB3A12	U10	33	34	AE6	IOB3A4
IOB3A11	Y8	35	36	AD4	IOB3A3
IOB3A10	W8	37	38	AC4	IOB3A2
IOB3A9	Y4	39	40	AA4	IOB3A1
IOB3A8	Y5	41	42	AB4	IOB3A0
VCCIO3B	–	43	44	–	VCCIO3B
IOB3B31	AH2	45	46	AF9	IOB3B15
IOB3B30	AH3	47	48	AE8	IOB3B14
IOB3B29	AH4	49	50	AF8	IOB3B13
IOB3B28	AG5	51	52	AE7	IOB3B12
IOB3B27	AH5	53	54	AF4	IOB3B11
IOB3B26	AH6	55	56	AE4	IOB3B10
IOB3B25	AG6	57	58	AF6	IOB3B9
IOB3B24	AF7	59	60	AF5	IOB3B8
VCCIO3B	–	61	62	–	VCCPD3B4A
IOB3B23	AE9	63	64	W11	IOB3B7
IOB3B22	AD10	65	66	V11	IOB3B6
IOB3B21	AF10	67	68	U11	IOB3B5
IOB3B20	AF11	69	70	T11	IOB3B4
IOB3B19	AD11	71	72	W12	IOB3B3
IOB3B18	AE11	73	74	V12	IOB3B2
IOB3B17	AD12	75	76	T13	IOB3B1
IOB3B16	AE12	77	78	T12	IOB3B0
VCCIO3B	–	79	80	–	VCCPD3B4A
IOB4A67	AH11	81	82	AH9	IOB4A33
IOB4A66	AG11	83	84	AG10	IOB4A32
VCCIO4A	–	85	86	–	VCCIO4A
IOB4A65	AH13	87	88	AH8	IOB4A31
IOB4A64	AG14	89	90	AG9	IOB4A30
IOB4A63	AH14	91	92	AH7	IOB4A29
IOB4A62	AG15	93	94	AG8	IOB4A28

continues on next page

Table 1 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
IOB4A61	AG16	95	96	AE15	IOB4A27
IOB4A60	AF17	97	98	AF15	IOB4A26
IOB4A59	AH16	99	100	AE17	IOB4A25
IOB4A58	AH17	101	102	AD17	IOB4A24
VCCIO4A	–	103	104	–	VCCPD3B4A
IOB4A57	AH18	105	106	V13	IOB4A23
IOB4A56	AG18	107	108	W14	IOB4A22
IOB4A55	AH19	109	110	AA13	IOB4A21
IOB4A54	AG19	111	112	Y13	IOB4A20
IOB4A53	AH21	113	114	AF13	IOB4A19
IOB4A52	AG21	115	116	AG13	IOB4A18
IOB4A51	AH22	117	118	AH12	IOB4A17
IOB4A50	AH23	119	120	AF18	IOB4A16
VCCIO4A	–	121	122	–	VCCPD3B4A
IOB4A49	AH24	123	124	AG23	IOB4A15
IOB4A48	AG24	125	126	AF23	IOB4A14
IOB4A47	AG25	127	128	AF22	IOB4A13
IOB4A46	AF25	129	130	AF21	IOB4A12
IOB4A45	AH26	131	132	AF20	IOB4A11
IOB4A44	AG26	133	134	AG20	IOB4A10
IOB4A43	AH27	135	136	AE19	IOB4A9
IOB4A42	AG28	137	138	AD19	IOB4A8
VCCIO4A	–	139	140	–	VCCIO4A
IOB4A41	AF28	141	142	AE23	IOB4A7
IOB4A40	AF27	143	144	AE24	IOB4A6
IOB4A39	AE22	145	146	AD20	IOB4A5
IOB4A38	AD23	147	148	AE20	IOB4A4
IOB4A37	AC23	149	150	U13	IOB4A3
IOB4A36	AC22	151	152	U14	IOB4A2
IOB4A35	AA18	153	154	AA15	IOB4A1
IOB4A34	AA19	155	156	Y15	IOB4A0
VCCIO5A	–	157	158	V5	VCCPD5A
IOB5A15	AE26	159	160	Y19	IOB5A7
IOB5A14	AF26	161	162	AA20	IOB5A6
IOB5A13	AB23	163	164	Y18	IOB5A5
IOB5A12	AC24	165	166	Y17	IOB5A4
IOB5A11	AA23	167	168	V15	IOB5A3
IOB5A10	AA24	169	170	V16	IOB5A2
IOB5A9	W15	171	172	AD26	IOB5A1
IOB5A8	Y16	173	174	AE25	IOB5A0
VCCIO5A	–	175	176	–	VCCPD5A
VCC33	–	177	178	–	VCC33
VCC33	–	179	180	–	VCC33

The FPGA pins marked 'xx' are specific to the used derivative according to the following table:

Version 3.0

Pin	A2/A4	A5/A6
IOB5B5	H6	W20
IOB5B4	H5	W21
IOB5B3	K8	AA26
IOB5B2	L8	AB26
IOB5B1	L9	W24
IOB5B0	L10	Y24
Nrst	H4	AB25

Version 4.0

FPGA Pin	Function A2/A4	Function A5/A6
Y24	GND	IOB5B0
W24	GND	IOB5B1
AB26	GND	IOB5B2
AA26	GND	IOB5B3
W21	GND	IOB5B4
W20	GND	IOB5B5
AB25	GND	IOB5B6
L10	IOB5B0	GND
L9	IOB5B1	GND
L8	IOB5B2	GND
K8	IOB5B3	GND
H5	IOB5B4	GND
H6	IOB5B5	GND
H4	IOB5B6	GND

3.6.2 Connector P2

The following signals are routed to connector P2:

Group	Signals	VCCIO	VCCPD
–	6 Transceiver	–	–
–	2 Ref Clocks	–	–
IOB7A	19 signals IO-Bank 7A	VCC33	VCC33
IOB7B	22 signals IO-Bank 7B	VCCIO7B	VCCPD7B
IOB7C	2 signals IO Bank 7C	VCC33	VCC333
IOB7D	14 signals IO-Bank 7D	VCCIO7D	VCCPD7D
–	14 signals IO-Bank 5A,6A	VCC15	VCC25
IDT	6 Clocks, I^2C, SEL	–	–

The following Signals are available on connector P2:

Version 3.0

Function	FPGA	Pin	Pin	FPGA	Function
GND	–	1	2	–	GND
REFCLK0Lp	V5	3	4	P8	REFCLK1Lp
REFCLK0Ln	V4	5	6	N8	REFCLK1Ln
GND	–	7	8	–	GND
GXB_RX_L0p	AF2	9	10	P2	GXB_RX_L3p
GXB_RX_L0n	AF1	11	12	P1	GXB_RX_L3n
GND	–	13	14	–	GND
GXB_TX_L0p	AD2	15	16	M2	GXB_TX_L3p
GXB_TX_L0n	AD1	17	18	M1	GXB_TX_L3n
GND	–	19	20	–	GND
GXB_RX_L1p	AB2	21	22	K2	GXB_RX_L4p
GXB_RX_L1n	AB1	23	24	K1	GXB_RX_L4n
GND	–	25	26	–	GND
GXB_TX_L1p	Y2	27	28	H2	GXB_TX_L4p
GXB_TX_L1n	Y1	29	30	H1	GXB_TX_L4n
GND	–	31	32	–	GND
GXB_RX_L2p	V2	33	34	F2	GXB_RX_L5p
GXB_RX_L2n	V1	35	36	F1	GXB_RX_L5n
GND	–	37	38	–	GND
GXB_TX_L2p	T2	39	40	D2	GXB_TX_L5p
GXB_TX_L2n	T1	41	42	D1	GXB_TX_L5n
GND	–	43	44	–	GND
–	–	45	46	–	–
–	–	47	48	–	–
GND	–	49	50	–	GND
–	–	51	52	–	–
–	–	53	54	–	–
GND	–	55	56	–	GND
–	–	57	58	–	–
–	–	59	60	–	–
VCC33	–	61	62	–	VCC33
reserved	–	63	64	–	reserved
reserved	–	65	66	–	reserved
reserved	–	67	68	–	reserved
reserved	–	69	70	A5	HPS_GPIO37
HPS_GPIO44	B12	71	72	–	reserved
reserved	–	73	74	–	reserved
VCC33	–	75	76	–	VCC33
VCCIO7B	–	77	78	–	VCCPD7B
HPS_GPIO33	A6	79	80	A9	HPS_GPIO27
HPS_GPIO31	A7	81	82	J12	HPS_GPIO24
HPS_GPIO29	A8	83	84	A11	HPS_GPIO25
HPS_GPIO22	J13	85	86	A12	HPS_GPIO23
HPS_GPIO16	J14	87	88	J16	HPS_GPIO32
HPS_GPIO14	J15	89	90	A13	HPS_GPIO21
HPS_GPIO28	D15	91	92	C14	HPS_GPIO34
HPS_GPIO26	C15	93	94	A14	HPS_GPIO19

continues on next page

Table 2 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
HPS_GPIO30	H16	95	96	B14	HPS_GPIO35
HPS_GPIO20	E16	97	98	A15	HPS_GPIO17
HPS_GPIO18	D17	99	100	A16	HPS_GPIO15
VCCIO7B	–	101	102	–	VCCPC7B
VCCIO7D	–	103	104	–	VCCPD7D
HPS_GPIO4	C4	105	106	C10	HPS_GPIO1
HPS_GPIO2	F5	107	108	C9	HPS_GPIO3
HPS_GPIO13	D5	109	110	C8	HPS_GPIO5
HPS_GPIO12	E5	111	112	C7	HPS_GPIO7
HPS_GPIO0	E4	113	114	C6	HPS_GPIO9
HPS_GPIO6	D4	115	116	C5	HPS_GPIO11
HPS_GPIO8	F4	117	118	G4	HPS_GPIO10
VCCIO7D	–	119	120	–	VCCPD7D
HPS_GPIO64	B16	121	122	B18	HPS_GPIO59
HPS_GPIO66	C16	123	124	A18	HPS_GPIO57
HPS_GPIO58	C17	125	126	A19	HPS_GPIO55
HPS_GPIO63	C19	127	128	B19	HPS_GPIO65
HPS_GPIO62	H17	129	130	A20	HPS_GPIO53
HPS_GPIO52	K18	131	132	B21	HPS_GPIO50
HPS_GPIO60	J17	133	134	A21	HPS_GPIO51
HPS_GPIO54	J18	135	136	C21	HPS_GPIO48
HPS_GPIO61	A17	137	138	A22	HPS_GPIO49
HPS_GPIO56	C18	139	140	–	VCC33
VCC33	–	141	142	–	VCC33
HPS_GPI10	U15	143	144	T26	HPS_DQ_32
HPS_GPI11	U16	145	146	P26	HPS_GPI5
HPS_GPI7	T16	147	148	R28	HPS_GPI4
HPS_DQS_4	V18	149	150	T17	HPS_GPI6
HPS_DQ_34	AC28	151	152	AC27	HPS_GPI12
HPS_GPI8	Y28	153	154	U25	HPS_DQ_33
HPS_GPI9	Y26	155	156	V24	HPS_GPI13
VCC33	–	157	158	–	VCC33
HPS_RSTn	A23	159	160	–	CLKextA
VCCBAT D7	–	161	162	–	CLKextB
VCC33	–	163	164	–	IDTV4
IDT_SDAT	–	165	166	–	CLKextC
IDT_SCLK	–	167	168	–	CLKextD
IDT_SEL0	–	169	170	–	IDTV5
IDT_SEL1	–	171	172	–	CLKextF
IDT_SEL2	–	173	174	–	CLKextE
VCC33	–	175	176	–	VCC33
VCC33	–	177	178	–	VCC33
VCC33	–	179	180	–	VCC33

Version 4.0

Function	FPGA	Pin	Pin	FPGA	Function
GND	–	1	2	–	GND
REFCLK0Lp	V5	3	4	P8	REFCLK1Lp

continues on next page

Table 3 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
REFCLK0Ln	V4	5	6	N8	REFCLK1Ln
GND	–	7	8	–	GND
GXB_RX_L0p	AF2	9	10	P2	GXB_RX_L3p
GXB_RX_L0n	AF1	11	12	P1	GXB_RX_L3n
GND	–	13	14	–	GND
GXB_TX_L0p	AD2	15	16	M2	GXB_TX_L3p
GXB_TX_L0n	AD1	17	18	M1	GXB_TX_L3n
GND	–	19	20	–	GND
GXB_RX_L1p	AB2	21	22	K2	GXB_RX_L4p
GXB_RX_L1n	AB1	23	24	K1	GXB_RX_L4n
GND	–	25	26	–	GND
GXB_TX_L1p	Y2	27	28	H2	GXB_TX_L4p
GXB_TX_L1n	Y1	29	30	H1	GXB_TX_L4n
GND	–	31	32	–	GND
GXB_RX_L2p	V2	33	34	F2	GXB_RX_L5p
GXB_RX_L2n	V1	35	36	F1	GXB_RX_L5n
GND	–	37	38	–	GND
GXB_TX_L2p	T2	39	40	D2	GXB_TX_L5p
GXB_TX_L2n	T1	41	42	D1	GXB_TX_L5n
GND	–	43	44	–	GND
–	–	45	46	–	–
–	–	47	48	–	–
GND	–	49	50	–	GND
–	–	51	52	–	–
–	–	53	54	–	–
GND	–	55	56	–	GND
–	–	57	58	–	–
–	–	59	60	–	–
VCC33	–	61	62	–	VCC33
reserved	–	63	64	–	reserved
reserved	–	65	66	–	reserved
reserved	–	67	68	–	reserved
reserved	–	69	70	A5	HPS_GPIO37
HPS_GPIO44	B12	71	72	–	reserved
reserved	–	73	74	–	reserved
VCC33	–	75	76	–	VCC33
VCCIO7B	–	77	78	–	VCCPD7B
HPS_GPIO33	A6	79	80	A9	HPS_GPIO27
HPS_GPIO31	A7	81	82	J12	HPS_GPIO24
HPS_GPIO29	A8	83	84	A11	HPS_GPIO25
HPS_GPIO22	J13	85	86	A12	HPS_GPIO23
HPS_GPIO16	J14	87	88	J16	HPS_GPIO32
HPS_GPIO14	J15	89	90	A13	HPS_GPIO21
HPS_GPIO28	D15	91	92	C14	HPS_GPIO34
HPS_GPIO26	C15	93	94	A14	HPS_GPIO19
HPS_GPIO30	H16	95	96	B14	HPS_GPIO35
HPS_GPIO20	E16	97	98	A15	HPS_GPIO17
HPS_GPIO18	D17	99	100	A16	HPS_GPIO15
VCCIO7B	–	101	102	–	VCCPC7B

continues on next page

Table 3 – continued from previous page

Function	FPGA	Pin	Pin	FPGA	Function
VCCIO7D	–	103	104	–	VCCPD7D
HPS_GPIO4	C4	105	106	C10	HPS_GPIO1
HPS_GPIO2	F5	107	108	C9	HPS_GPIO3
HPS_GPIO13	D5	109	110	C8	HPS_GPIO5
HPS_GPIO12	E5	111	112	C7	HPS_GPIO7
HPS_GPIO0	E4	113	114	C6	HPS_GPIO9
HPS_GPIO6	D4	115	116	C5	HPS_GPIO11
HPS_GPIO8	F4	117	118	G4	HPS_GPIO10
VCCIO7D	–	119	120	–	VCCPD7D
HPS_GPIO64	B16	121	122	B18	HPS_GPIO59
HPS_GPIO66	C16	123	124	A18	HPS_GPIO57
HPS_GPIO58	C17	125	126	A19	HPS_GPIO55
HPS_GPIO63	C19	127	128	B19	HPS_GPIO65
HPS_GPIO62	H17	129	130	A20	HPS_GPIO53
HPS_GPIO52	K18	131	132	B21	HPS_GPIO50
HPS_GPIO60	J17	133	134	A21	HPS_GPIO51
HPS_GPIO54	J18	135	136	C21	HPS_GPIO48
HPS_GPIO61	A17	137	138	A22	HPS_GPIO49
HPS_GPIO56	C18	139	140	–	VCC33
VCC33	–	141	142	–	VCC33
HPS_GPI10	U15	143	144	T26	HPS_DQ_32
HPS_GPI11	U16	145	146	P26	HPS_GPI5
HPS_GPI7	T16	147	148	R28	HPS_GPI4
HPS_DQS_4	V18	149	150	T17	HPS_GPI6
HPS_DQ_34	AC28	151	152	AC27	HPS_GPI12
HPS_GPI8	Y28	153	154	U25	HPS_DQ_33
HPS_GPI9	Y26	155	156	V24	HPS_GPI13
VCC33	–	157	158	–	VCC33
HPS_RSTn	A23	159	160	–	CLKextA
VCCBAT D7	–	161	162	–	CLKextB
VCC33	–	163	164	–	IDTV4
IDT_SDAT	–	165	166	–	–
IDT_SCLK	–	167	168	–	–
PROG	–	169	170	–	–
–	–	171	172	–	CLKextF
–	–	173	174	–	CLKextE
VCC33	–	175	176	–	VCC33
VCC33	–	177	178	–	VCC33
VCC33	–	179	180	–	VCC33

3.7 Power Supply

Version 3.0

MCV is supplied by a 3,3V single supply.

Version 4.0

MCV is supplied by a MPM3840 4A single supply.

3.8 Reset

The HPS-NPOR signal and the RSTn FPGA signal are connected to the power good signal of the power stage. The Warm reset signal is available on connector P2.

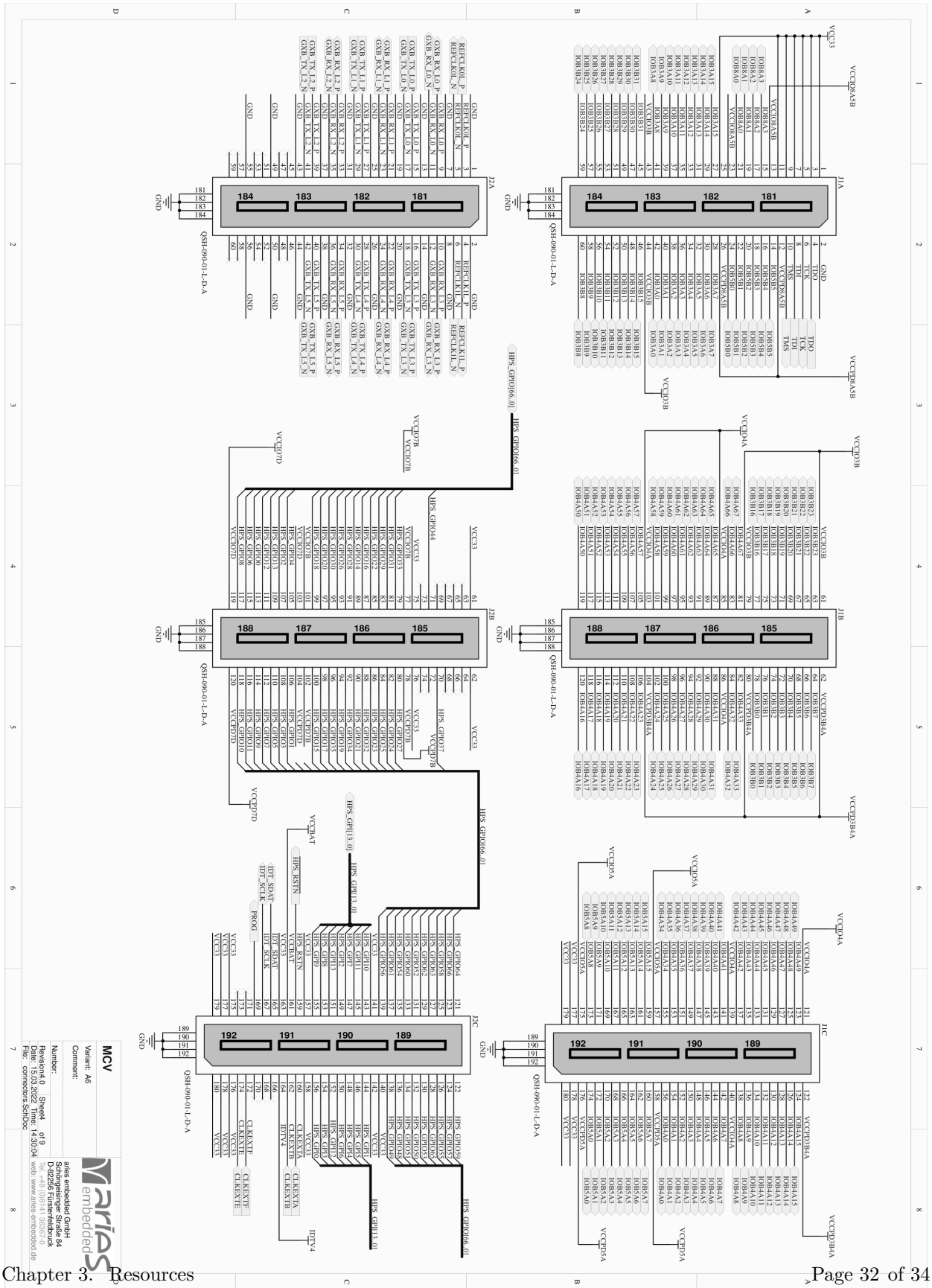
3.9 VBat

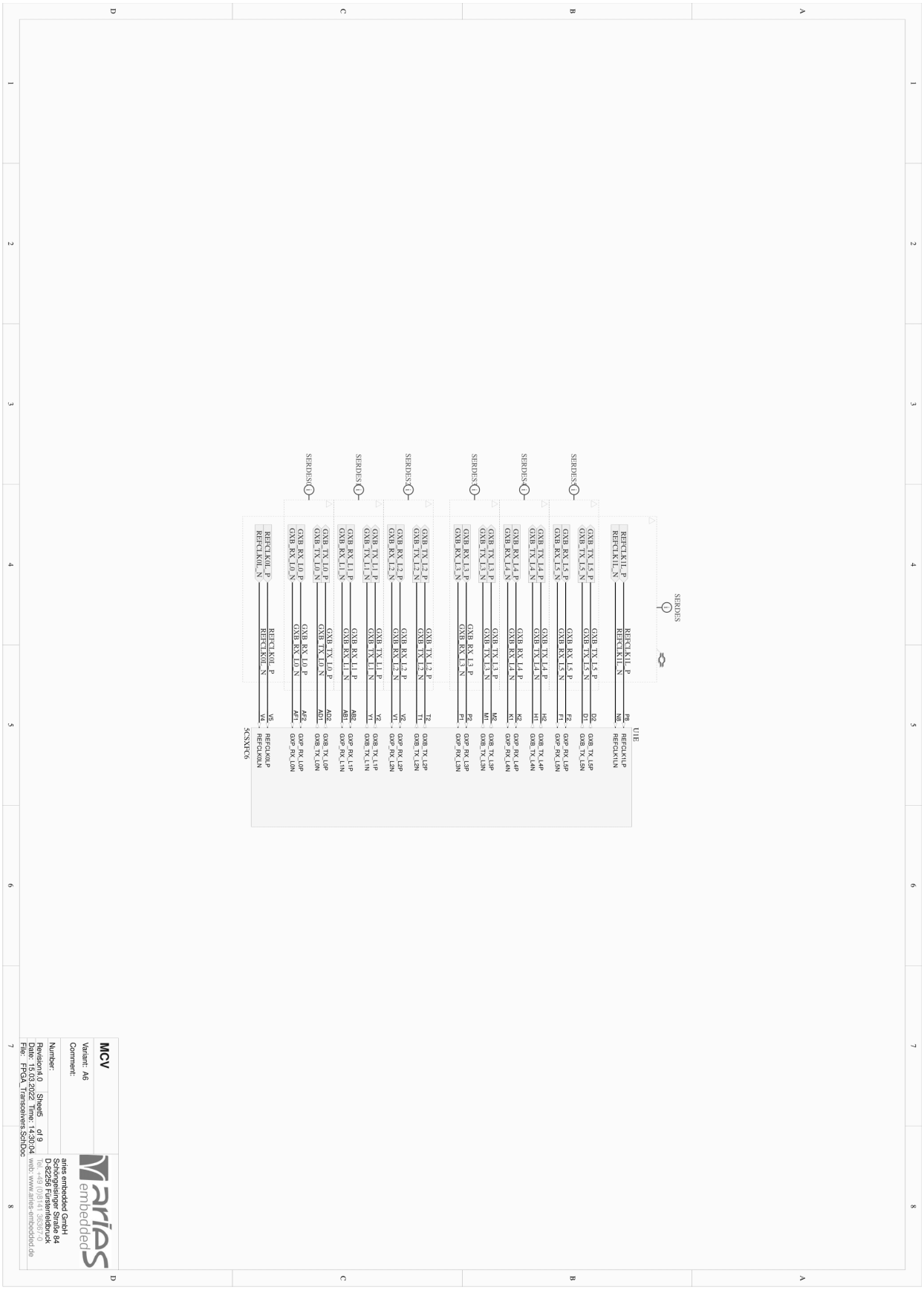
The VBAT signal is available on connector P2. The VBAT signal has to be connected to power to ensure proper functionality of the MCV SoM.

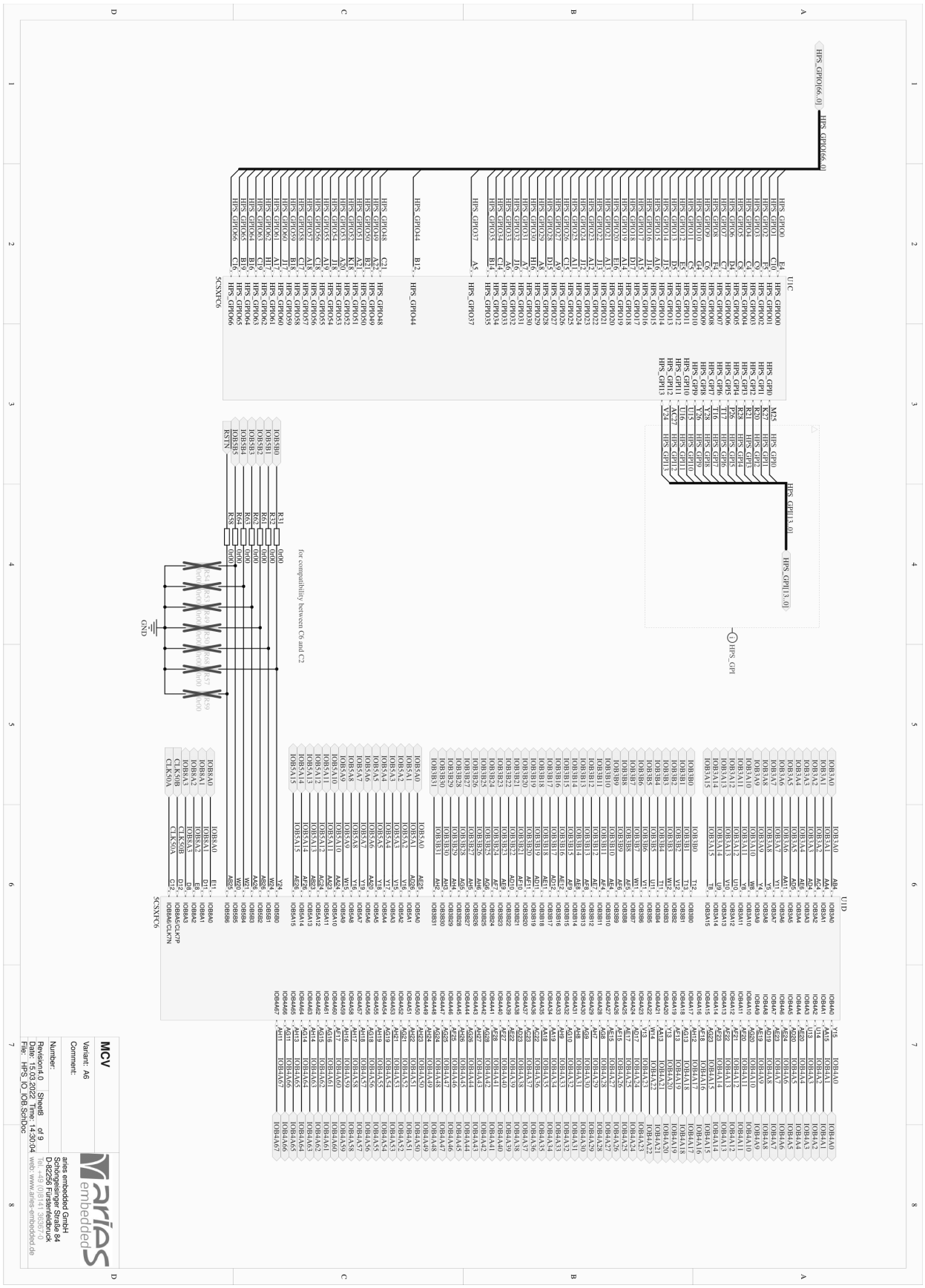
3.10 Reference Implementation

A reference FPGA project can be ontained on request.

3.11 Schematics




MCV
Variant: A6
Comment:
aries embedded GmbH
Schongaueringer Straße 84
D-82256 Fürstenfeldbruck
Tel.: +49 (0)8141 36357-0
web: www.aries-embedded.de
Number:
Revision:4.0
Sheet5 of 9
Date: 15.03.2022 Time: 14:38:04
File: FPGA_Transceivers.SchDoc
SERDES
U1E
5CSXFC6
REFCLK1I_P
REFCLK1I_N
REFCLK1IA_P
REFCLK1IA_N
SERDES1
SERDES2
SERDES3
SERDES4
SERDES5
GXB_TX_L5_P
GXB_TX_L5_N
GXB_RX_L5_P
GXB_RX_L5_N
GXB_TX_L4_P
GXB_TX_L4_N
GXB_RX_L4_P
GXB_RX_L4_N
GXB_TX_L3_P
GXB_TX_L3_N
GXB_RX_L3_P
GXB_RX_L3_N
GXB_TX_L2_P
GXB_TX_L2_N
GXB_RX_L2_P
GXB_RX_L2_N
GXB_TX_L1_P
GXB_TX_L1_N
GXB_RX_L1_P
GXB_RX_L1_N
GXB_TX_L0_P
GXB_TX_L0_N
GXB_RX_L0_P
GXB_RX_L0_N
REFCLK6I_P
REFCLK6I_N
REFCLK6GLP
REFCLK6GLN
GXP_RX_L5P
GXP_RX_L5N
GXP_RX_L4P
GXP_RX_L4N
GXP_RX_L3P
GXP_RX_L3N
GXP_RX_L2P
GXP_RX_L2N
GXP_RX_L1P
GXP_RX_L1N
GXP_RX_L0P
GXP_RX_L0N
GXB_TX_L5P
GXB_TX_L5N
GXB_TX_L4P
GXB_TX_L4N
GXB_TX_L3P
GXB_TX_L3N
GXB_TX_L2P
GXB_TX_L2N
GXB_TX_L1P
GXB_TX_L1N
GXB_TX_L0P
GXB_TX_L0N


HPS_GPIO[66..0]
HPS_GPIO66
HPS_GPIO13..0
HPS_GPIO13..0
HPS_GPI
U1C
SCSXTC6
HPS_GPIO44
HPS_GPIO37
HPS_GPIO48
HPS_GPIO49
HPS_GPIO50
HPS_GPIO51
HPS_GPIO52
HPS_GPIO53
HPS_GPIO54
HPS_GPIO55
HPS_GPIO56
HPS_GPIO57
HPS_GPIO58
HPS_GPIO59
HPS_GPIO60
HPS_GPIO61
HPS_GPIO62
HPS_GPIO63
HPS_GPIO64
HPS_GPIO65
HPS_GPIO66
IOBSB0
IOBSB1
IOBSB2
IOBSB3
IOBSB4
IOBSB5
RSTN
R31
R61
R62
R63
R64
R58
0r00
GND
for compatibility between C6 and C2
U1D
SCSXTC6
IOBA0
IOBA1
IOBA2
IOBA3
IOBA4
IOBA5
IOBA6
IOBA7
IOBA8
IOBA9
IOBA10
IOBA11
IOBA12
IOBA13
IOBA14
IOBA15
IOBA16
IOBA17
IOBA18
IOBA19
IOBA20
IOBA21
IOBA22
IOBA23
IOBA24
IOBA25
IOBA26
IOBA27
IOBA28
IOBA29
IOBA30
IOBA31
IOBA32
IOBA33
IOBA34
IOBA35
IOBA36
IOBA37
IOBA38
IOBA39
IOBA40
IOBA41
IOBA42
IOBA43
IOBA44
IOBA45
IOBA46
IOBA47
IOBA48
IOBA49
IOBA50
IOBA51
IOBA52
IOBA53
IOBA54
IOBA55
IOBA56
IOBA57
IOBA58
IOBA59
IOBA60
IOBA61
IOBA62
IOBA63
IOBA64
IOBA65
IOBA66
IOBA67
IOBSA0
IOBSA1
IOBSA2
IOBSA3
IOBSA4
IOBSA5
IOBSA6
IOBSA7
IOBSA8
IOBSA9
IOBSA10
IOBSA11
IOBSA12
IOBSA13
IOBSA14
IOBSA15
CLKS0A
CLKS0B
IOBSA0-CLK7P
IOBSA0-CLK7N
IOBSB0
IOBSB1
IOBSB2
IOBSB3
IOBSB4
IOBSB5
IOBSB6
IOBSB7
IOBSB8
IOBSB9
IOBSB10
IOBSB11
IOBSB12
IOBSB13
IOBSB14
IOBSB15
IOBSB16
IOBSB17
IOBSB18
IOBSB19
IOBSB20
IOBSB21
IOBSB22
IOBSB23
IOBSB24
IOBSB25
IOBSB26
IOBSB27
IOBSB28
IOBSB29
IOBSB30
IOBSB31
IOBSB32
IOBSB33
IOBSB34
IOBSB35
IOBSB36
IOBSB37
IOBSB38
IOBSB39
IOBSB40
IOBSB41
IOBSB42
IOBSB43
IOBSB44
IOBSB45
IOBSB46
IOBSB47
IOBSB48
IOBSB49
IOBSB50
IOBSB51
IOBSB52
IOBSB53
IOBSB54
IOBSB55
IOBSB56
IOBSB57
IOBSB58
IOBSB59
IOBSB60
IOBSB61
IOBSB62
IOBSB63
IOBSB64
IOBSB65
IOBSB66
MCV
Variant: A6
Comment:
aries embedded GmbH
Schongauinger Straße 84
D-82256 Fürstenfeldbruck
Tel.: +49 (0)8141 36367-0
web: www.aries-embedded.de
Number:
Revision:4.0
Date: 15.03.2022 Time: 14:30:04
File: HPS_IO_IOB.SchDoc
Sheet6 of 9