MCVEVP Hardware Manual

Release 1

ARIES Embedded GmbH

July 03, 2017

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

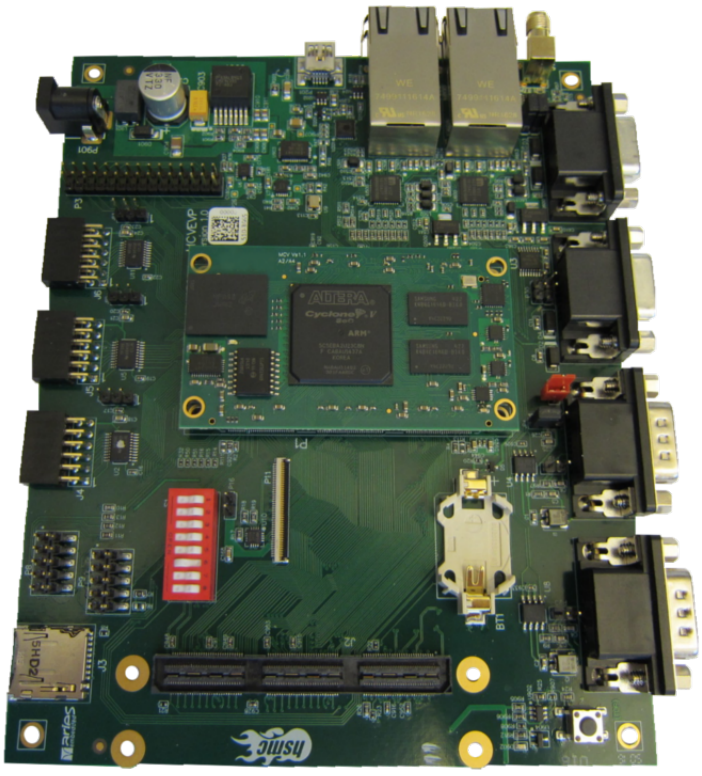
Revision	Date	Revised	Comment
1.0	20.03.2017	aw	Initial creation
1.1	29.03.2017	bnh	Pinout description completed

CHAPTER

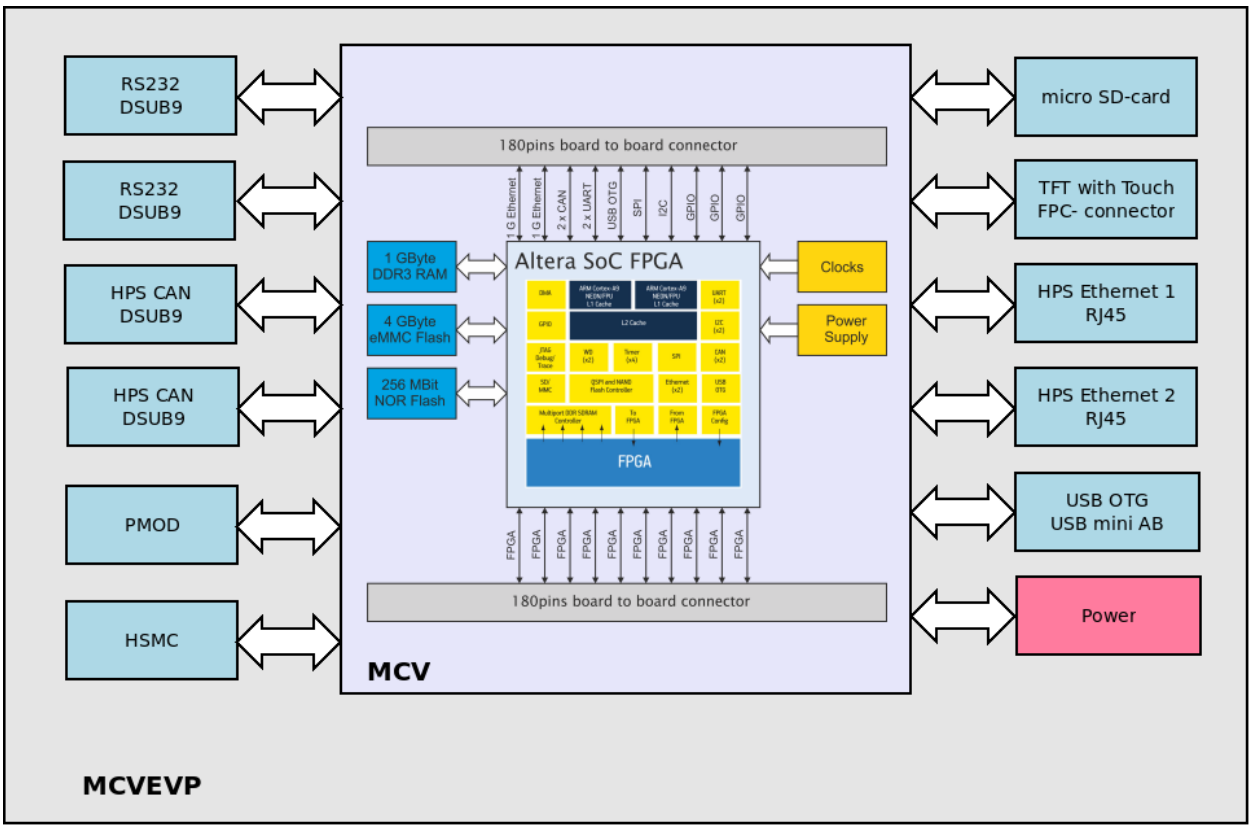
TWO

OVERVIEW

MCVEVP represents the flexible Evaluation Platform for working with the MCV SoM. It can be used for developing software as well as implementing prototyps.



2.1 Block Diagram

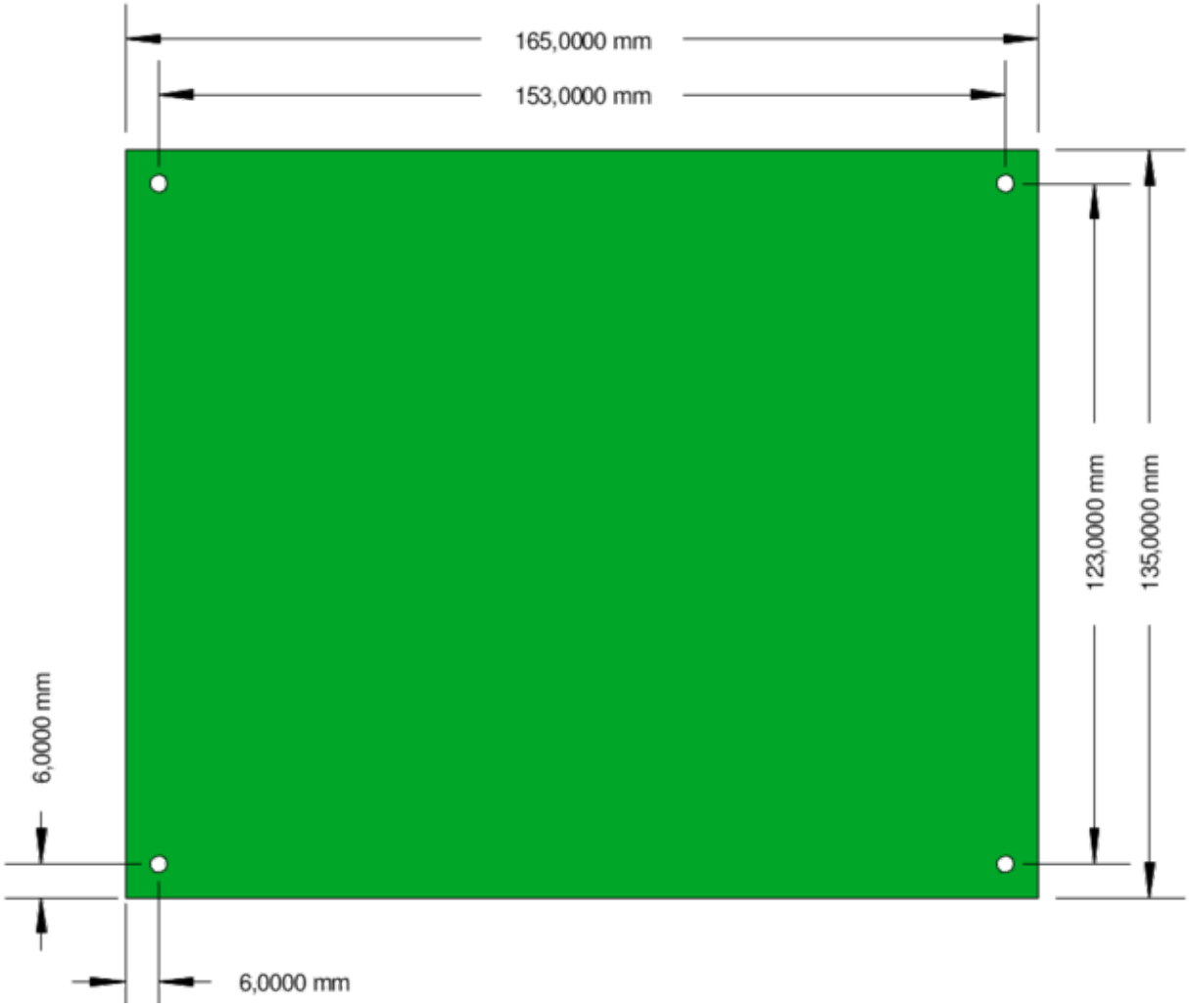


2.2 Feature Set

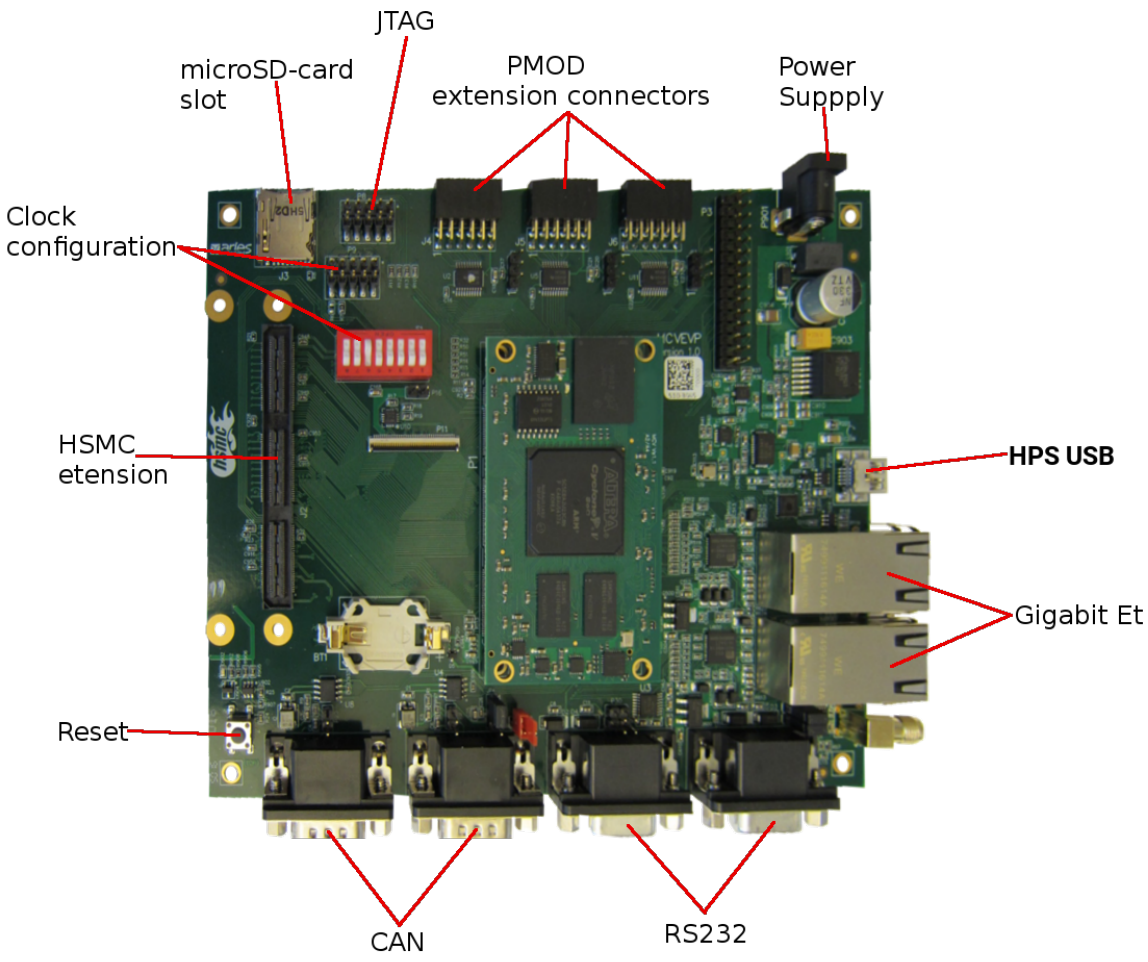
For supporting development projects and fast prototyping in the best possible way MCVEVK supplies

- 2x HPS Gigabit Ethernet on a RJ45 connector
- HPS USB on a mini-USB connector
- 2x UART on a DUSB-9 connector each
- 2x CAN on a DUSB-9 connector each
- TFT with Touch
- HSMC extension connector
- 3x PMOD extension connectors
- microSD-card slot
- boot mode selection for FPGA-/eMMC-boot-mode
- JTAG pin header
- flexible supply voltage 7V to 36V DC

2.3 Dimensions

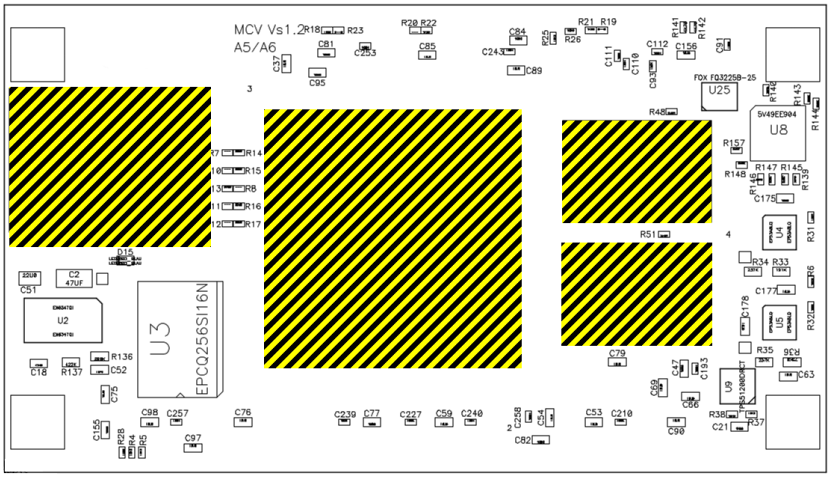


2.4 Parts Location



2.5 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on MCV it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:


MCV Vs1.2
A5/A6
U3
EPCQ256SI16N
U25
U8
5V49EE904
U2
U9

CHAPTER

THREE

RESOURCES

3.1 Ethernet

MCVEVP offers the EMAC0 and EMAC1 Ethernet Ports in RGMII mode of the Cyclone V SoC-FPGA. These ports can be accessed via the RJ45 connectors P500 and P600 supported by Microchip KSZ903 Ethernet physical-layer transceivers.

3.2 UART

The two UARTs of the SoC-FPGA HPS are available on a RS232 signal level.

The interface jumpers can be set vertical or horizontal so that the interface complies with straight- or cross-type RS232 cables. The following table shows the signal for horizontal jumper setting, in case of vertical jumper settings RX and TX signals are swapped accordingly.

3.2.1 UART1 – HPS (P21)

Pin	Function	Connector	FPGA Pin
2	RX	P2-138	A22 – HPS_GPIO49
3	TX	P2-132	B21 – HPS_GPIO50
5	GND		

3.2.2 UART2 – HPS (P22)

Pin	Function	Connector	FPGA Pin
2	RX	P1-77	AE12
3	TX	P1-75	AD12
5	GND		

3.3 USB-OTG

MCVEVP supports an USB-OTG port. The Microchip USB3320 USB-OTG Phy drives the physical connection, it is connected to the HPS of the SoC-FPGA by using the ULPI interface running at 1.8V. The respective connector on MCVEVP could be found at position P201.

3.4 CAN

Two CAN ports are available on MCVEVP. The signals on the DSUB connector can optionally be terminated by 120 Ohms. This is done by setting the jumpers at position P19 and P20.

Function	Connector-Pin	FPGA Pin
CAN0-TX	P2-129	H17 – HPS_GPIO62
CAN0-RX	P2-137	A17 – HPS_GPIO61
CAN1-TX	P2-135	J18 – HPS_GPIO54
CAN1-RX	P2-130	A20 – HPS_GPIO53

3.4.1 CAN1 (P23)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.4.2 CAN2 (P24)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.5 Boot Select

Connector P32 offers the selection of the boot-media as follows:

closed	FPGA boot
open	eMMC boot

3.6 IDT Clock-Buffer

Pin header P9 on the MCVEVK provides the I2C programming interface for the IDT Clock buffer on the MCV SoM:

3.6.1 Connector P9

Function	Pin	Pin	Function
GND	1	2	n.c.
GND	3	4	n.c.
GND	5	6	n.c.
SDAT	7	8	n.c.
SCLK	9	10	VCC18

Voltage selection at pin 10 is possible via Resistor R6 and R7. The default voltage is 1.8V.

3.6.2 DIP Switch S1

DIP Switch S1 can be used to configure the clock chip on MCV and change the JTAG scan chain. The clock chip can be programmed with an external I2C device or directly by the MCV while using the I2C0 interface. While configuring the clock chip directly with the MCV, care should be taken to use a valid configuration, since a wrong clock can render the board inoperable until it the clock chip is reconfigured with an **external** I2C device.

Switch one to three can be used to select one of six configurations stored in the IDT5V49EE904 clock generator. Switch 'on' represents a logic one and 'off' a logic zero.

Switch	Signal	Default
1	IDT_SEL0	off
2	IDT_SEL1	off
3	IDT_SEL2	off

Switch four and five connect the clock generator's I2C bus to the MCV's I2C0 bus and therefore enable it to program the clock generator directly with the MCV. These switches should always be set together.

Switch	Signal	Default
4	I2C0_SDA to IDT_SDAT	off
5	I2C0_SCL to IDT_SCL	off

Switch six to eight include/exclude the HSMC connector into the JTAG scan chain. There are only two valid combinations. The first and default one is shown in the following table and directly connects the JTAG header P8 with the MCV board.

Switch	Signal	configuration 1 (default)
6	MCV_TDO	on
7	MCV_TDO	off
8	HSMC_TDO	off

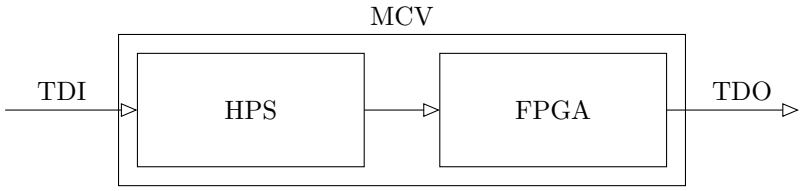


Fig. 3.1: JTAG scan chain in default configuration

The second valid combination is listed in the next table and includes the HSMC connector into the JTAG scan chain.

Switch	Signal	configuration 2
6	MCV_TDO	off
7	MCV_TDO	on
8	HSMC_TDO	on

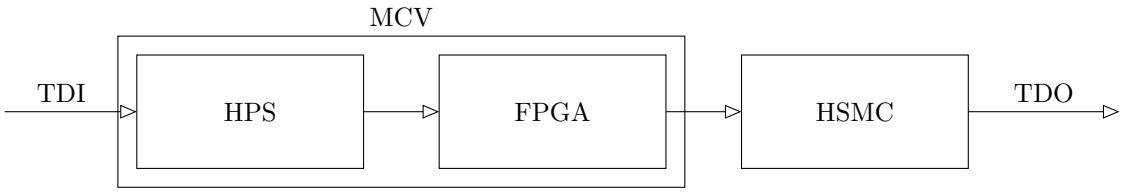


Fig. 3.2: JTAG scan chain with HSMC in serial

3.7 JTAG

P8 provides the JTAG signals of the SoC FPGA to the outer world. The JTAG connector complies with the standard Altera pinout, the USB-Blaster or the new USB-Blaster II can be directly connected. The following signals are available:

3.7.1 Connector P8

Function	Pin	Pin	Function
TCK	1	2	GND
TDO	3	4	VCC33
TMS	5	6	NC
NC	7	8	NC
TDI	9	10	GND

3.8 Pmod module connectors

Three 2x6 angled pin headers are available on the MCV EVP board which fit the requirements for Pmod modules. To support a wider range of possible modules, each connector has its own level shifter. A corresponding jumper allows the selection between 3.3V or 5V module voltage.

3.8.1 Connector J4:

Function	FPGA	Pin	Pin	FPGA	Function
IOB4A16	AF18	1	7	AH12	IOB4A17
IOB4A44	AG26	2	8	AH26	IOB4A45
IOB4A52	AG21	3	9	AH21	IOB4A53
IOB3B0	T12	4	10	T13	IOB3B1
GND		5	11		GND
VCC		6	12		VCC

3.8.2 Connector J5:

Function	FPGA	Pin	Pin	FPGA	Function
IOB3B2	V12	1	7	C19	HPS_GPIO63
IOB8A0	E11	2	8	B16	HPS_GPIO64
IOB8A1	D11	3	9	B19	HPS_GPIO65
IOB8A2	E8	4	10	C16	HPS_GPIO66
GND		5	11		GND
VCC		6	12		VCC

3.8.3 Connector J6:

Function	FPGA	Pin	Pin	FPGA	Function
HPS_GPIO26	C15	1	7	C17	HPS_GPIO58/SCL3
HPS_GPIO27	A9	2	8	B18	HPS_GPIO59/SDA3
HPS_GPIO21	A13	3	9	J17	HPS_GPIO60
HPS_GPIO20	E16	4	10	A14	HPS_GPIO19
GND		5	11		GND
VCC		6	12		VCC

3.9 HSMC connector

MCVEVP houses a High Speed Mezzanine Card (HSMC) connector. Its pinout is shown in the following table.

3.9.1 Connector J2:

Function	FPGA pin	Pin	Pin	FPGA pin	Function
NC		1	2		NC
NC		3	4		NC
GND		5	6		GND
NC		7	8		NC
NC		9	10		NC
GND		11	12		GND
GXB_TX_L5_P	D2	13	14	F2	GXB_RX_L5_P
GXB_TX_L5_N	D1	15	16	F1	GXB_RX_L5_N
GND		17	18		GND
GXB_TX_L4_P	H2	19	20	K2	GXB_RX_L4_P
GXB_TX_L4_N	H1	21	22	K1	GXB_RX_L4_N
GND		23	24		GND
GXB_TX_L3_P	M2	25	26	P2	GXB_RX_L3_P
GXB_TX_L3_N	M1	27	28	P1	GXB_RX_L3_N
GND		29	30		GND
GXB_TX_L2_P	T2	31	32	V2	GXB_RX_L2_P
GXB_TX_L2_N	T2	33	34	V1	GXB_RX_L2_N
GND		35	36		GND
GXB_TX_L1_P	Y2	37	38	AB2	GXB_RX_L1_P
GXB_TX_L1_N	Y1	39	40	AB1	GXB_RX_L1_N
GND		41	42		GND
GXB_TX_L0_P	AD2	43	44	AF2	GXB_RX_L0_P
GXB_TX_L0_N	AD1	45	46	AF1	GXB_RX_L0_N
GND		47	48		GND
HPS_GPIO51/SDA1/HSMC_SDA	A21	49	50	K18	HPS_GPIO52/SCL1/HSMC_SCL
TCK		51	52		TMS
GND		53	54		GND
HSMC_TDO		55	56		HSMC_TDI
CLK25_HSMC		57	58		NC
GND		59	60		GND
IOB4A11	AF20	61	62	Y15	IOB4A0/CLK3p

Continued on next page

Table 3.1 – continued from previous page

Function	FPGA pin	Pin	Pin	FPGA pin	Function
IOB4A10	AG20	63	64	AA15	IOB4A1/CLK3n
VCC33		65	66		VIN
IOB4A28	AG8	67	68	U14	IOB4A2
IOB4A29	AH7	69	70	U13	IOB4A3
VCC33		71	72		VIN
IOB4A30	AG9	73	74	AE20	IOB4A4
IOB4A31	AH8	75	76	AD20	IOB4A5
VCC33		77	78		VIN
IOB4A32	AG10	79	80	AE24	IOB4A6
IOB4A33	AH9	81	82	AE23	IOB4A7
VCC33		83	84		VIN
IOB4A40	AF27	85	86	AE19	IOB4A9
IOB4A41	AF28	87	88	AD19	IOB4A8
VCC33		89	90		VIN
IOB4A42	AG28	91	92	AF22	IOB4A13
IOB4A43	AH27	93	94	AF21	IOB4A12
VCC33		95	96		VIN
IOB4A48	AG24	97	98	AG23	IOB4A15
IOB4A49	AH24	99	100	AF23	IOB4A14
VCC33		101	102		VIN
IOB4A50	AH23	103	104	AG13	IOB4A18
IOB4A51	AH22	105	106	AF13	IOB4A19
VCC33		107	108		VIN
IOB4A54	AG19	109	110	Y13	IOB4A20/CLK2p
IOB4A55	AH19	111	112	AA13	IOB4A21/CLK2n
VCC33		113	114		VIN
CLKEXT_P		115	116		REFCLK0L_P
CLKEXT_N		117	118		REFCLK0L_N
VCC33		119	120		VIN
IOB4A56	AG18	121	122	W14	IOB4A22
IOB4A57	AH18	123	124	V13	IOB4A23
VCC33		125	126		VIN
IOB4A58	AH17	127	128	AE15	IOB4A24
IOB4A59	AH16	129	130	AE17	IOB4A25
VCC33		131	132		VIN
IOB4A62	AG15	133	134	AF15	IOB4A26
IOB4A63	AH14	135	136	AE15	IOB4A27
VCC33		137	138		VIN
IOB4A64	AG14	139	140	AA19	IOB4A34
IOB4A65	AH13	141	142	AA18	IOB4A35
VCC33		143	144		VIN
IOB4A66	AG11	145	146	AC22	IOB4A36
IOB4A67	AH11	147	148	AC23	IOB4A37
VCC33		149	150		VIN
IOB3B24	AF7	151	152	AD23	IOB4A38
IOB3B25	AG6	153	154	AE22	IOB4A39
VCC33		155	156		VIN
IOB3B19	AD11	157	158	AF25	IOB4A46
IOB3B18	AE11	159	160	AG25	IOB4A47

Continued on next page

Table 3.1 – continued from previous page

Function	FPGA pin	Pin	Pin	FPGA pin	Function
VCC33		161	162		VIN
IOB3B20	AF11	163	164	AF17	IOB4A60
IOB3B21	AF10	165	166	AG16	IOB4A61
VCC33		167	168		VIN
IOB3B22	AD10	169	170	Y23	IOB5B0/CLK4p
IOB3B23	AE9	171	172	W24	IOB5B1/CLK4n
VCC33		173	174		VIN
IOB5B2/CLKOUTp	AB26	175	176	W21	IOB5B4/CLK5p
IOB5B3/CLKOUTn	AA26	177	178	W20	IOB5B5/CLK5n
VCC33		179	180	**M25**	**HPS_GPI0** * / module presence detection
GND		181	182		GND
GND		183	184		GND
GND		185	186		GND
GND		187	188		GND
GND		189	190		GND
GND		191	192		GND

Important: Pins marked with * are currently mapped to different FPGA pins. Please refer to section *Pinout inconsistencies between FPGA and connector* for further information!

3.10 miniPCIe and PCIe

Unlike the MCVEVK, the MCVEVP does not house a miniPCIe slot. Nevertheless we offer adapters for miniPCIe and PCIe x8 cards, which can be inserted into the HSMC connectors.

3.11 Pin Header

Pinheader P3 provides access to 27 IO Pins of MCV.

3.11.1 Connector P3

Function	FPGA pin	Pin	Pin	FPGA pin	Function
VCC33		1	2	B14	HPS_GPIO35
HPS_GPIO14	J15	3	4	A5	HPS_GPIO37
HPS_GPIO33	A6	5	6	B12	HPS_GPIO44
HPS_GPIO34	C14	7	8	C21	HPS_GPIO48
HPS_GPI1 *	**K27**	9	10	D8	IOB8A3
HPS_GPI2 *	**R20**	11	12	Y5	IOB3A8
HPS_GPI5	P26	13	14	AH6	IOB3B26
HPS_GPI6	T17	15	16	AH5	IOB3B27
HPS_GPI7	T16	17	18	AG5	IOB3B28
HPS_GPI8	Y28	19	20	AH4	IOB3B29
HPS_GPI9	Y26	21	22	AH3	IOB3B30
HPS_GPI10	U15	23	24	AH2	IOB3B31
HPS_GPI11	U16	25	26	AA20	IOB5A6
HPS_GPI12	AC27	27	28	Y19	IOB5A7
GND		29	30		GND

Important: Pins marked with * are currently mapped to different FPGA pins. Please refer to section *Pinout inconsistencies between FPGA and connector* for further information!

3.12 Pin Multiplexing

When used on the MCVEVP baseboard, MCV supports the follwing pin multiplexing:

3.12.1 EMAC0

	SoM pin	Function	FPGA pin
INT	P2 154	**HPS_GPI3** *	R21
RX_CLK	P2 118	HPS_GPIO10	G4
RX_CTL	P2 117	HPS_GPIO8	F4
RXD0	P2 110	HPS_GPIO5	C8
RXD1	P2 116	HPS_GPIO11	C5
RXD2	P2 111	HPS_GPIO12	E5
RXD3	P2 109	HPS_GPIO13	D5
TX_CLK	P2 113	HPS_GPIO0	E4
TX_CTL	P2 114	HPS_GPIO9	C6
TXD0	P2 106	HPS_GPIO1	C10
TXD1	P2 107	HPS_GPIO2	F5
TXD2	P2 108	HPS_GPIO3	C9
TXD3	P2 105	HPS_GPIO4	C4
MDC	P2 112	HPS_GPIO7	C7
MDIO	P2 115	HPS_GPIO6	D4

Important: Pins marked with * are currently mapped to different FPGA pins. Please refer to section *Pinout inconsistencies between FPGA and connector* for further information!

3.12.2 EMAC1

	SoM pin	Function	FPGA pin
INT	P2 148	HPS_GPI4	R28
RX_CLK	P1 167	IOB5A11	AA23
RX_CTL	P1 165	IOB5A12	AC24
RXD0	P1 169	IOB5A10	AA24
RXD1	P1 170	IOB5A2	V16
RXD2	P1 168	IOB5A3	V15
RXD3	P1 173	IOB5A8	Y16
TX_CLK	P1 159	IOB5A15	AE26
TX_CTL	P1 172	IOB5A1	AD26
TXD0	P1 169	IOB5A10	AA24
TXD1	P1 163	IOB5A13	AB23
TXD2	P1 171	IOB5A9	W15
TXD3	P1 166	IOB5A4	Y17
MDC	P1 161	IOB5A14	AF26
MDIO	P1 164	IOB5A5	Y18

3.12.3 USB1

	SoM pin	Function	FPGA pin
D0	P2 100	HPS_GPIO 15	A16
D1	P2 87	HPS_GPIO 16	J14
D2	P2 98	HPS_GPIO 17	A15
D3	P2 99	HPS_GPIO 18	D17
D4	P2 85	HPS_GPIO 22	J13
D5	P2 86	HPS_GPIO 23	A12
D6	P2 82	HPS_GPIO 24	J12
D7	P2 84	HPS_GPIO 25	A11
CLK	P2 83	HPS_GPIO 29	A8
NXT	P2 88	HPS_GPIO 32	J16
DIR	P2 81	HPS_GPIO 31	A7
STP	P2 95	HPS_GPIO 30	H16

3.12.4 CAN0

CAN 0	SoM pin	Function	FPGA pin
RX	P2 137	HPS_GPIO 61	A17
TX	P2 129	HPS_GPIO 62	H17

3.12.5 CAN1

CAN 1	SoM pin	Function	FPGA pin
RX	P2 130	HPS_GPIO 53	A20
TX	P2 135	HPS_GPIO 54	J18

3.12.6 UART0

UART0	SoM pin	Function	FPGA pin
RX	P2 138	HPS_GPIO 49	A22
TX	P2 132	HPS_GPIO 50	B21

3.12.7 UART1

UART1	SoM pin	Function	FPGA pin
RX	P1 77	IOB3B16	AE12
TX	P1 75	IOB3B17	AD12

3.12.8 I2C0

I2C0	SoM pin	Function	FPGA pin
SDA	P2 126	HPS_GPIO 55	A19
SCL	P2 139	HPS_GPIO 56	C18
TOUCH_INT	P2 124	HPS_GPIO 57	A18

3.12.9 LCD

	SoM pin	Function	FPGA pin
LCD_DE	P1 72	IOB3B3	W12
LCD_DIM	P1 70	IOB3B4	T11
LCD_B5	P1 68	IOB3B5	U11
LCD_B4	P1 66	IOB3B6	V11
LCD_B3	P1 64	IOB3B7	W11
LCD_B2	P1 60	IOB3B8	AF5
LCD_B1	P1 58	IOB3B9	AF6
LCD_B0	P1 56	IOB3B10	AE4
LCD_G5	P1 54	IOB3B11	AF4
LCD_G4	P1 52	IOB3B12	AE7
LCD_G3	P1 50	IOB3B13	AF8
LCD_G2	P1 48	IOB3B14	AE8
LCD_G1	P1 46	IOB3B15	AF9
LCD_G0	P1 42	IOB3A0	AB4
LCD_R5	P1 40	IOB3A1	AA4
LCD_R4	P1 38	IOB3A2	AC4
LCD_R3	P1 36	IOB3A3	AD4
LCD_R2	P1 34	IOB3A4	AE6
LCD_R1	P1 32	IOB3A5	AD5
LCD_R0	P1 30	IOB3A6	AA11
LCD_CLK	P1 28	IOB3A7	Y11

3.13 Reset Button

Button P4 is connected to the HPS_RSTn signal of MCV.

3.14 LCD Interface

Many applications in the world of applications based on ARN architecture require display support. MCVEVP offers a TFT display interface, the MCV reference implementation offers a display controller IP. The TFT interface is implemented on the followinig signals:

Pin	Function	FPGA pin
1		
2		
3		
4	Backlight	
5	Backlight	
6	Backlight	
7	VCC33	
8		
9	LCD_DE	W12
10	Touch XP1	
11	Touch YP1	
12	LCD_DIM	T11
13	LCD_B5	U11
14	LCD_B4	V11
15	LCD_B3	W11
16	GND	
17	LCD_B2	AF5
18	LCD_B1	AF6
19	LCD_B0	AE4
20	GND	
21	LCD_G5	AF4
22	LCD_G4	AE7
23	LCD_G3	AF8
24	GND	
25	LCD_G2	AE8
26	LCD_G1	AF9
27	LCD_G0	AB4
28	GND	
29	LCD_R5	AA4
30	LCD_R4	AC4
31	LCD_R3	AD4
32	GND	
33	LCD_R2	AE6
34	LCD_R1	AD5
35	LCD_R0	AA11
36	Touch XMI	
37	Touch YMI	
38	LCD_CLK	Y11
39	GND	
40		

The backlight pins can be connected to 5V with Jumper P16.

3.15 Touch Controller

The touch controller (STMPE811) uses an I2C interface to connect to the FPGA. The interface is available on the following location:

	SoM pin	FPGA Pin	Function
SDAT	P2 126	A19	I2C0_SDA
SCLK	P2 139	C18	I2C0_SCL
INTn	P2 124	A18	HPS_GPIO57

3.16 MicroSD card

MCVEVP offers a slot to hold a microSD card.

	SoM pin	Function	FPGA pin
SD_DATA2	P1 27	IOB3A15	T8
SD_DATA3	P1 29	IOB3A14	U9
SD_CMD	P1 31	IOB3A13	V10
SD_CLK	P1 33	IOB3A12	U10
SD_DATA0	P1 35	IOB3A11	Y8
SD_DATA1	P1 37	IOB3A10	W8
SD_DETECT	P1 39	IOB3A9	Y4

CHAPTER

FOUR

POWER SUPPLY

4.1 Input voltage

The input voltage for the MCVEVP board can vary between 8.5V and 36V and is supplied via connector P901.

4.2 Bank voltages

The Bank voltages on MCVEVP are shown in the following table.

Bank	Voltage
3A	3.3V
3B	2.5 or 3.3V (selectable with JP4)
4A	
5A	3.3V (can be changed to 2.5V with R113 and R114)
7A	3.3V
7B	1.8V
7C	3.3V
7C	3.3V
8A	3.3V (can be changed to 2.5V with R111 and R112)

Note: At MCVEVP the predrive voltages are set to the same level as the IO voltages. When designing a custom Baseboard for MCV, or changing the voltage by resoldering the resistors (Bank 5A and 8A), refer to table 5-10 in Altera's *Cyclone V Device Handbook Volume 1* for predrive voltage selection.

4.3 Lithium cell holder BT1

The Altera Cyclone V SoC FPGA used on the MCV provides secure key storage in volatile memory. To keep the stored information after power down, a CR2032 lithium cell can be installed. If no cell is installed 2.5V is provided to the VCCBAT signal to keep the POR circuitry operational.

CHAPTER

FIVE

ERRATA

5.1 Pinout inconsistencies between FPGA and connector

It has been recently discovered, that there exist inconsistencies between the FPGA module and the MCV connector. Several Pins of the FPGA are routed and declared wrongly and therefore addressing these pins leads to an unexpected output at the connector.

The mentioned error affects five pins at connector P2. The following table illustrates the inconsistencies.

Pin at connector P2	FPGA pin	Current (wrong) FPGA pin	Declared function	Current function
156	M25	V24	HPS_GPI0	HPS_GPI13
144	K27	T26	HPS_GPI1	HPS_DQ_32
149	R20	V18	HPS_GPI2	HPS_DQS_4
154	R21	U25	HPS_GPI3	HPS_DQ_33
151	V24	AC28	HPS_GPI13	HPS_DQ_34

CHAPTER

SIX

APPENDIX

6.1 Schematics

MCV Evaluation Platform (EVP)

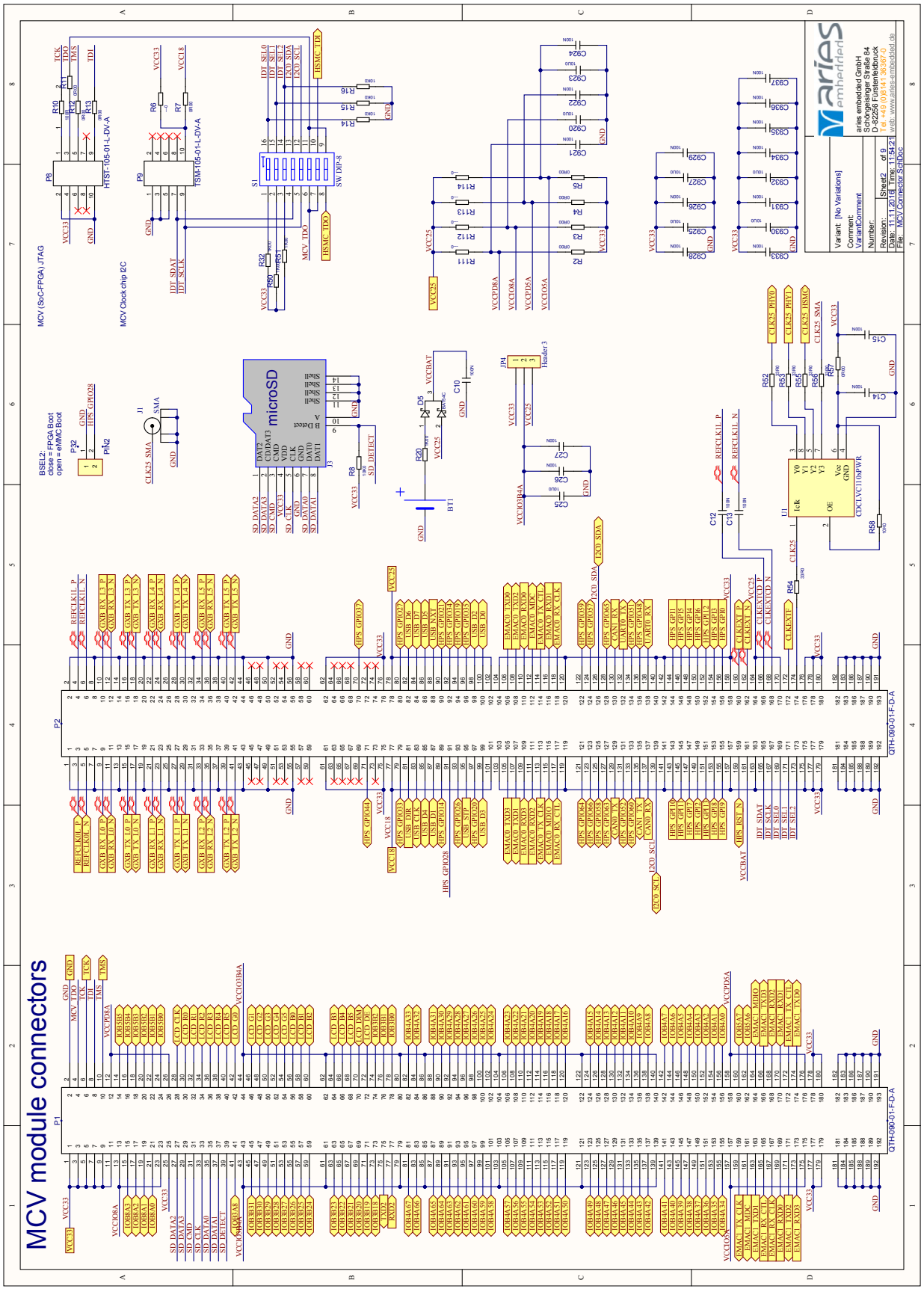
Table of Content

Revision History

Revision	Date	Changes
1.0	2016-09-20	Initial release, based on MCVEVK V3.1

Variant: [No Variations]
Comment: VariantComment
Number:
Revision:
Sheet1 of 9
Date: 11.11.2016 Time: 11:54:21
File: First_Sheet.SCHDOC

aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de


MCV module connectors
MCV (SoC-FPGA) JTAG
MCV Clock chip I2C
microSD
Header 3
aries embedded GmbH
Schützenstraße 86
D-42256 Füsten/elbruck
Tel.+49 (0)8141 36367-0
web: www.aries-embedded.de
MCV Connector Schdoc
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VariantComment:
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Revision:
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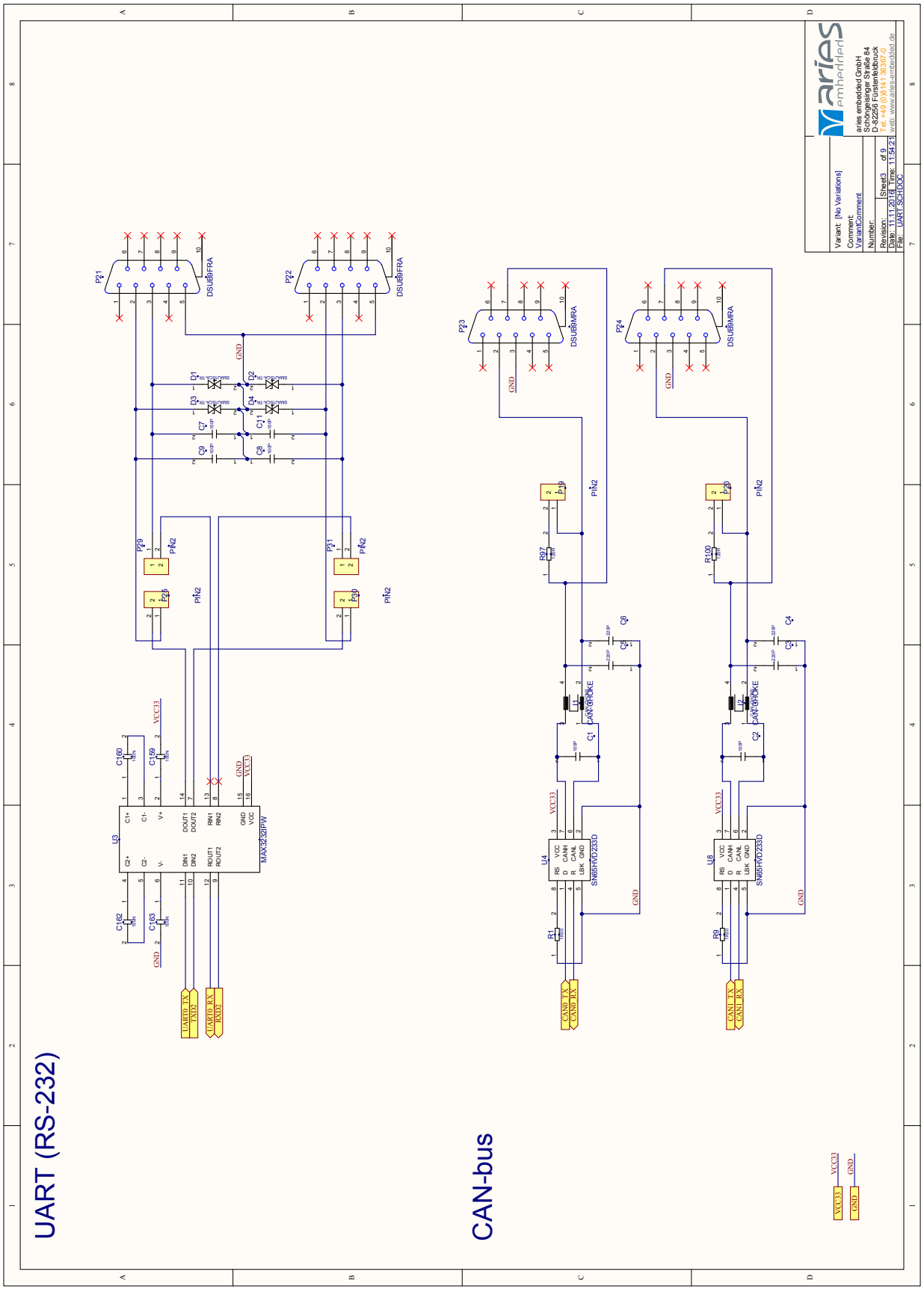
QTH-090-01-F-D-A


UART (RS-232)
CAN-bus
aries embedded GmbH
Schützenstraße 86
D-42256 Füsten/elbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de
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Comment:
VariantComment
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Revision:
Sheet3 of 9
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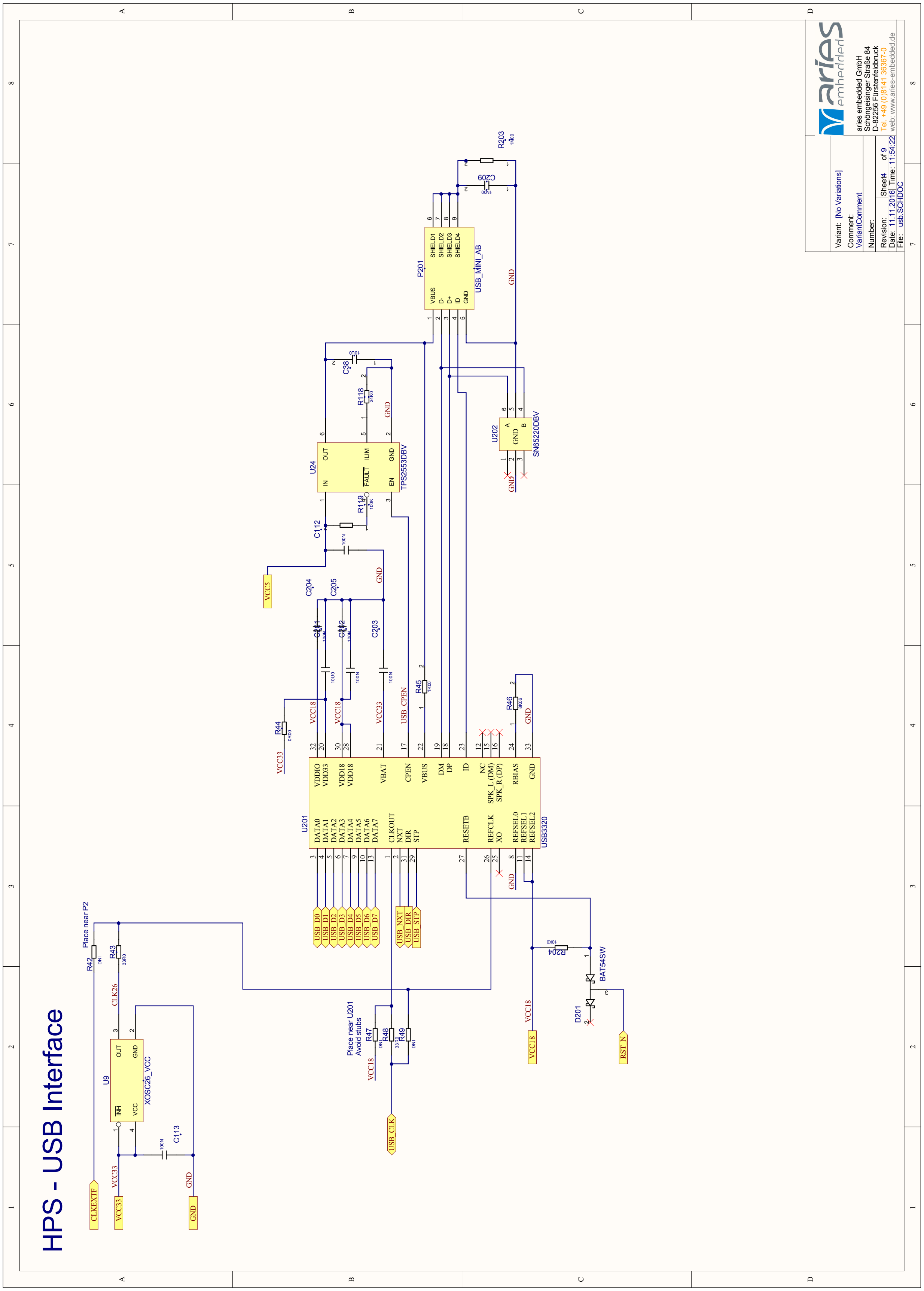
DSUB9FRA
DSUB9MRA
MAX3232IPW
SN65HVD235D
CAN-CHOKE
UART0_TX
UART0_RX
CAN1_TX
CAN1_RX
VCC33
GND


HPS - USB Interface
U201
USB3320
U24
TPS2553DBV
P201
USB_MINI_AB
U202
SN65220DBV
U9
XOSC26_VCC
D201
BAT54SW
Place near P2
Place near U201
Avoid stubs
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
web: www.aries-embedded.de
Variant: [No Variations]
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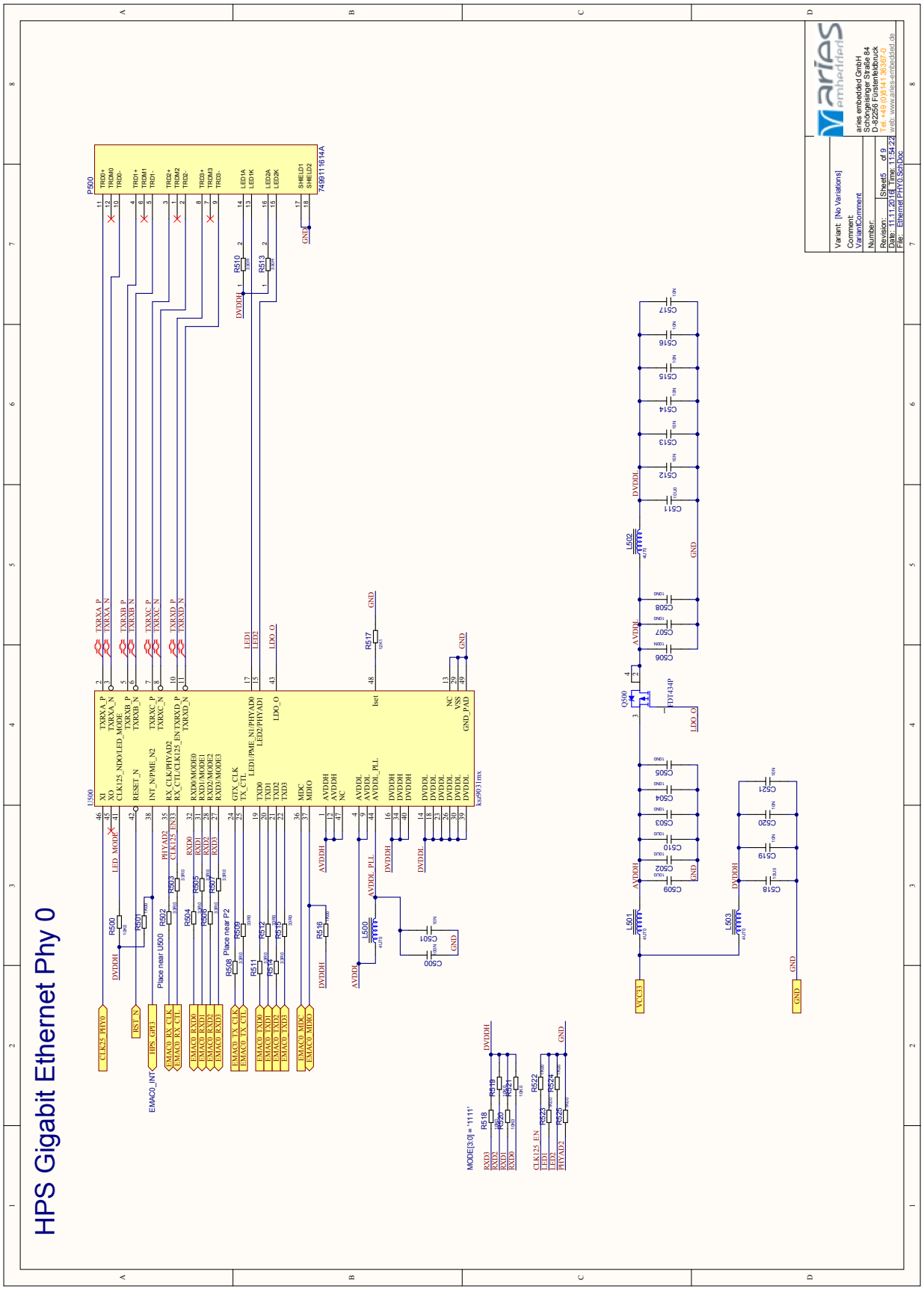
HPS Gigabit Ethernet Phy 0
aries embedded GmbH
Schützenstraße 86
D-42256 Füsten/elbruck
Tel. +49 (0)8141 36367-0
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VariantComment:
Number:
Revision:
Sheet5 of 9
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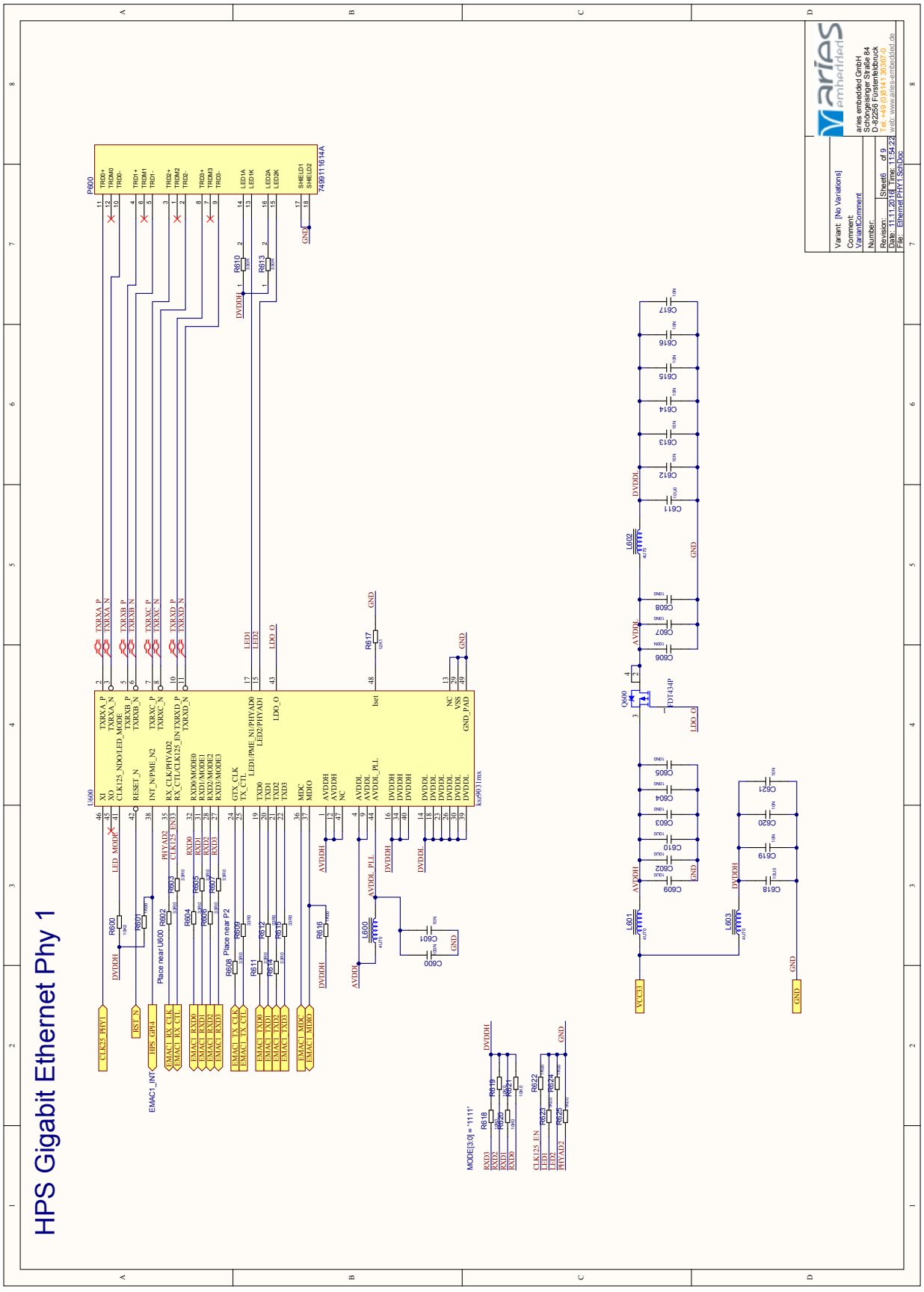
P500
U500
Q500
L500
L501
L502
L503
Place near U500
Place near P2
MODE[3:0] = '1111'
EMAC0_INT
VCC33
GND
DVDDH
AVDDH
DVDDL
AVDDL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aries embedded GmbH
Schützenstraße 86
D-32256 Füstenfeldbruck
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VariantComment
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Revision:
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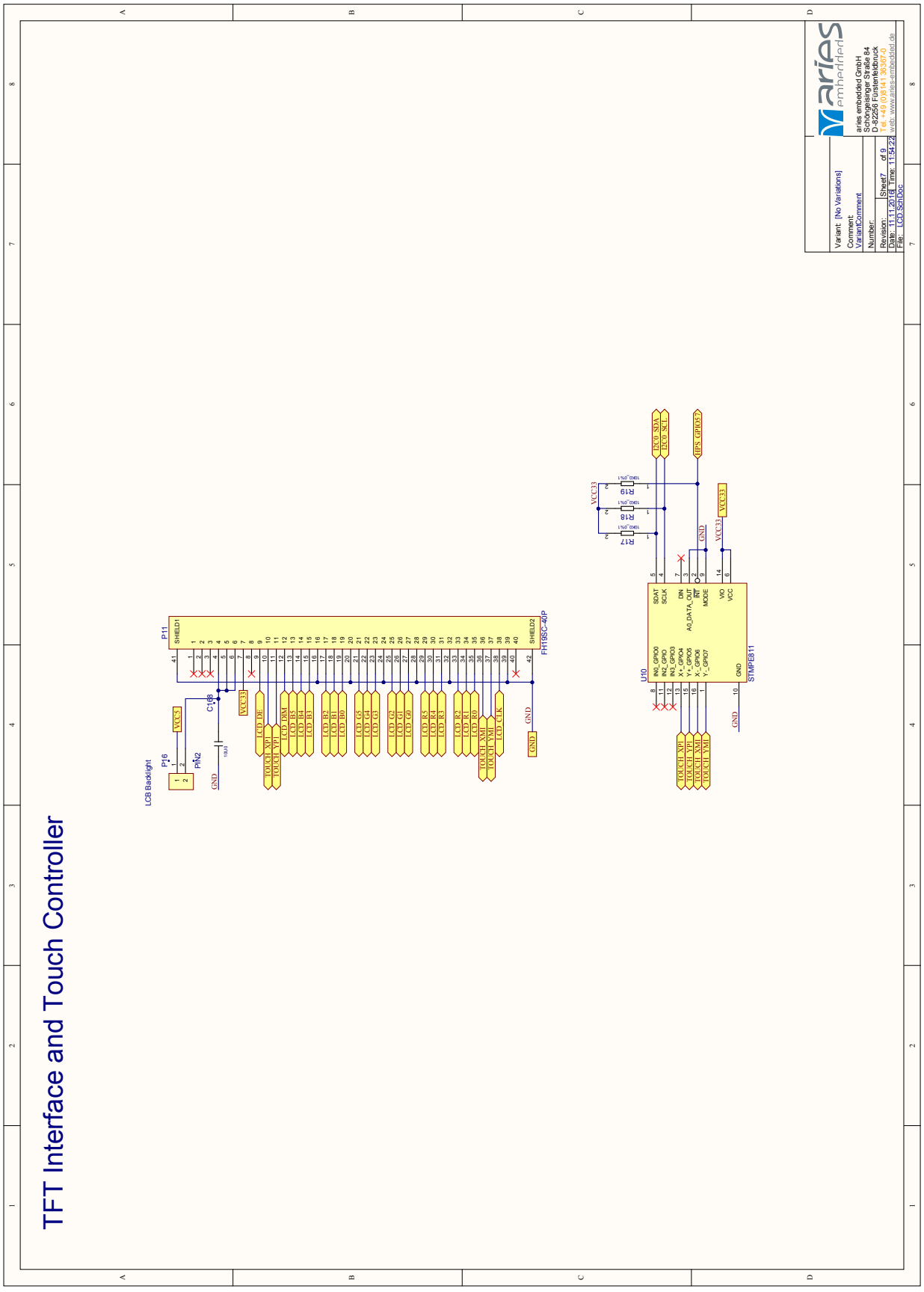
P600
U600
L600
L601
L602
L603
Q600
R600
R601
R602
R603
R604
R605
R606
R607
R608
R609
R610
R611
R612
R613
R614
R615
R616
R617
R618
R619
R620
R621
R622
R623
R624
R625
C600
C601
C602
C603
C604
C605
C606
C607
C608
C609
C610
C611
C612
C613
C614
C615
C616
C617
C618
C619
C620
C621
TXRXA_P
TXRXA_N
TXRXB_P
TXRXB_N
TXRXC_P
TXRXC_N
TXRXD_P
TXRXD_N
LED1
LED2
LDO_O
GND
DVDDH
AVDDH
AVDDL
DVDDL
VCC33
EMAC1_INT
MODE[3:0] = '1111'


TFT Interface and Touch Controller
aries embedded GmbH
Schützenweiher Straße 84
D-82256 Fürstenfeldbruck
Tel. +49 (0)8141 36367-0
web: www.aries-embedded.de
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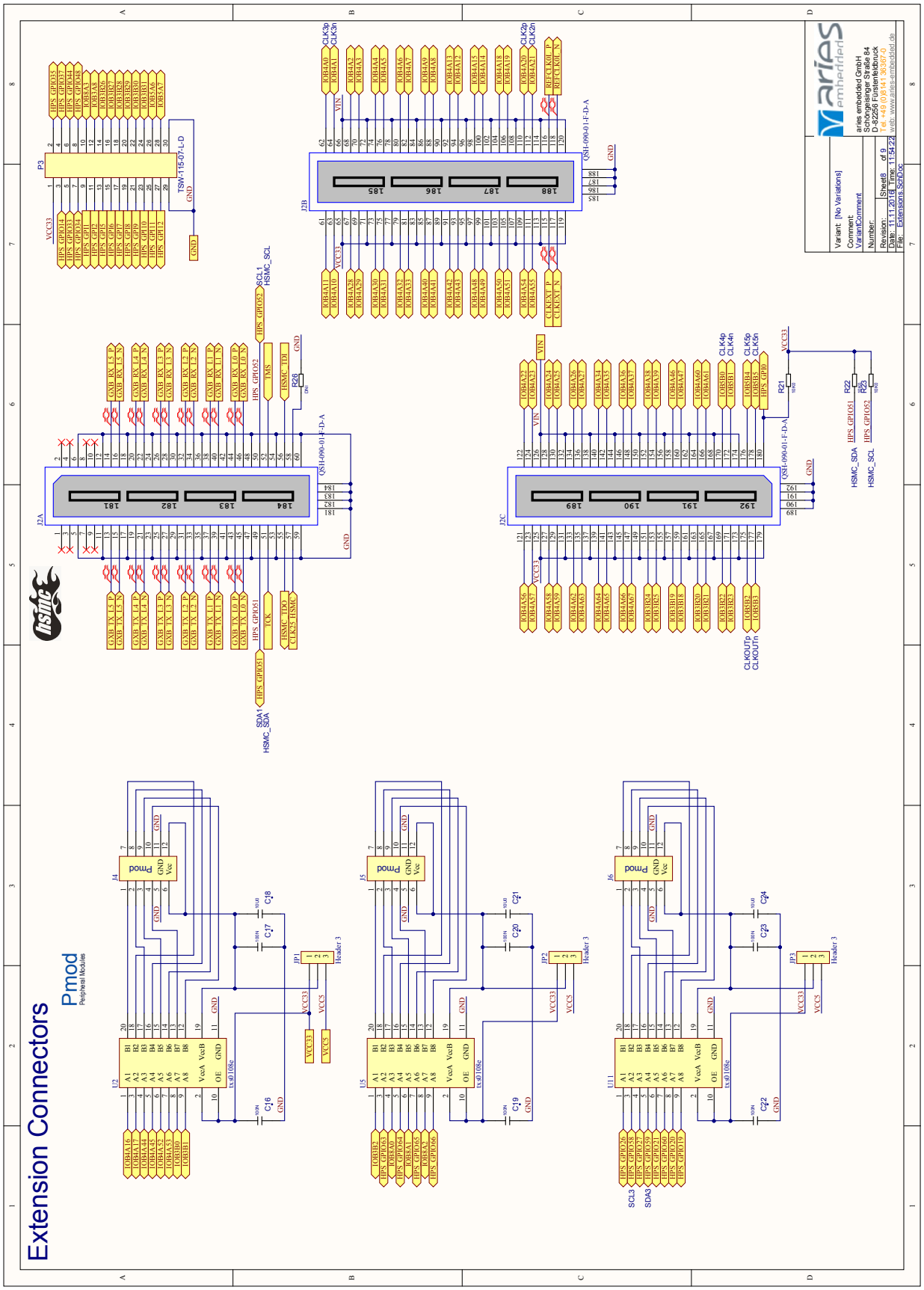
LCB Backlight
P16
P11
FH19SC-40P
C108
U10
STMPE811
R17
R18
R19
LCD_DE
LCD_DEN
LCD_B7
LCD_B6
LCD_B5
LCD_B4
LCD_B3
LCD_B2
LCD_B1
LCD_B0
LCD_G7
LCD_G6
LCD_G5
LCD_G4
LCD_G3
LCD_G2
LCD_G1
LCD_G0
LCD_R7
LCD_R6
LCD_R5
LCD_R4
LCD_R3
LCD_R2
LCD_R1
LCD_R0
LCD_CLK
TOUCH_XP
TOUCH_YP
TOUCH_XM
TOUCH_YM
I2C0_SDA
I2C0_SCL
IPS_GPIO57
VCC5
VCC33
GND


Extension Connectors
Pmod
Peripheral Modules
aries embedded GmbH
Schützenstraße 84
D-42256 Füsten/Ildbruck
Tel. +49 (0) 8141 36367-0
web: www.aries-embedded.de
Variant: [No Variations]
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VariantComment
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Revision:
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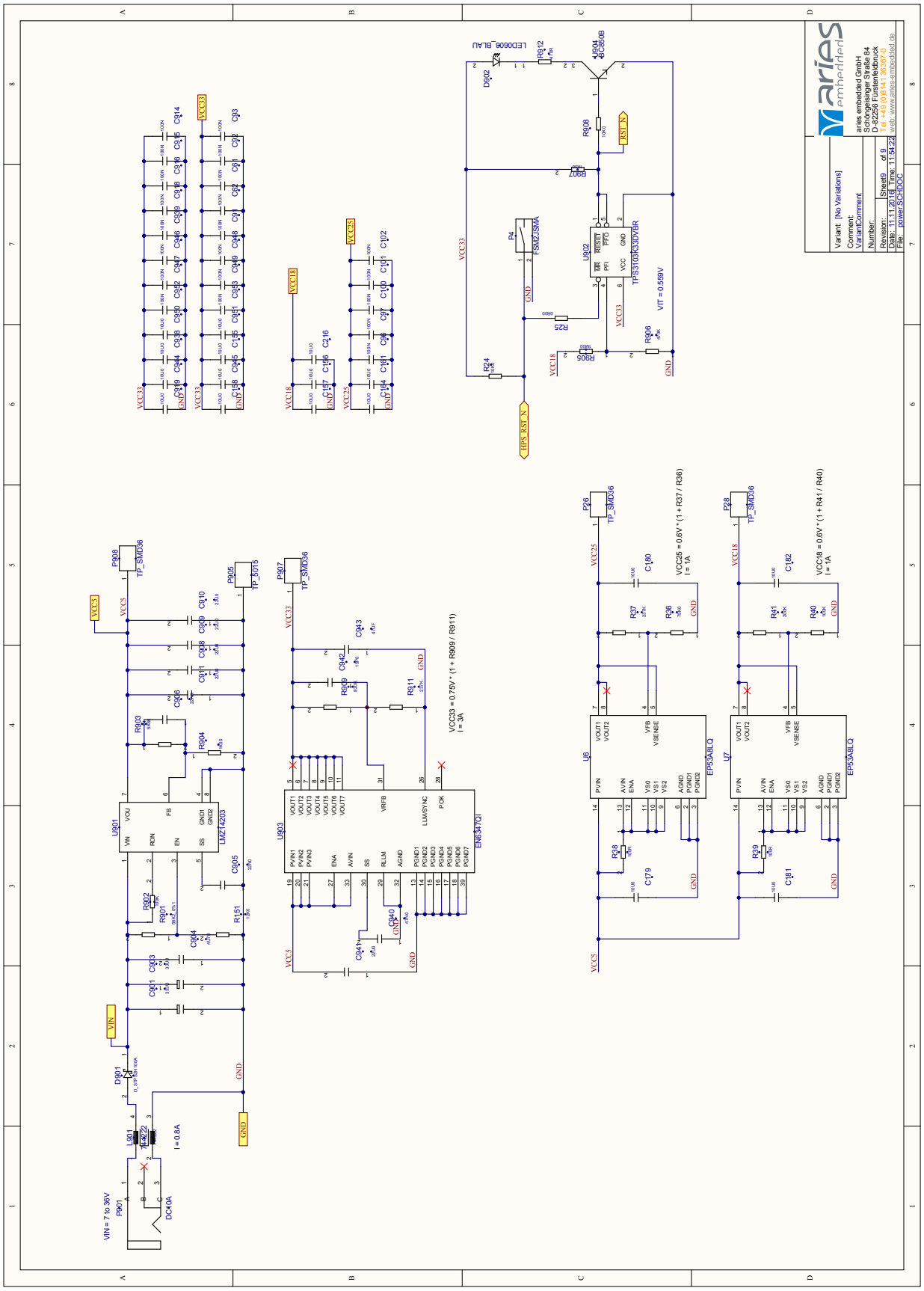
J2A
J2B
J2C
QSH-090-01-F-D-A
QSH-090-01-I-F-D-A
J4
J5
J6
JP1
JP2
Header 3
U2
U5
U11
74x8108e
Pmod
VCC33
VCC5
GND
HSMC_SDA
HSMC_SCL
HPS_GPIO51
HPS_GPIO52
TMS
TDI
TDO
TCK
CLKOUTp
CLKOUTn



6.2 Layout Diagram