MCVEVK Hardware Manual

Release 1

ARIES Embedded GmbH

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

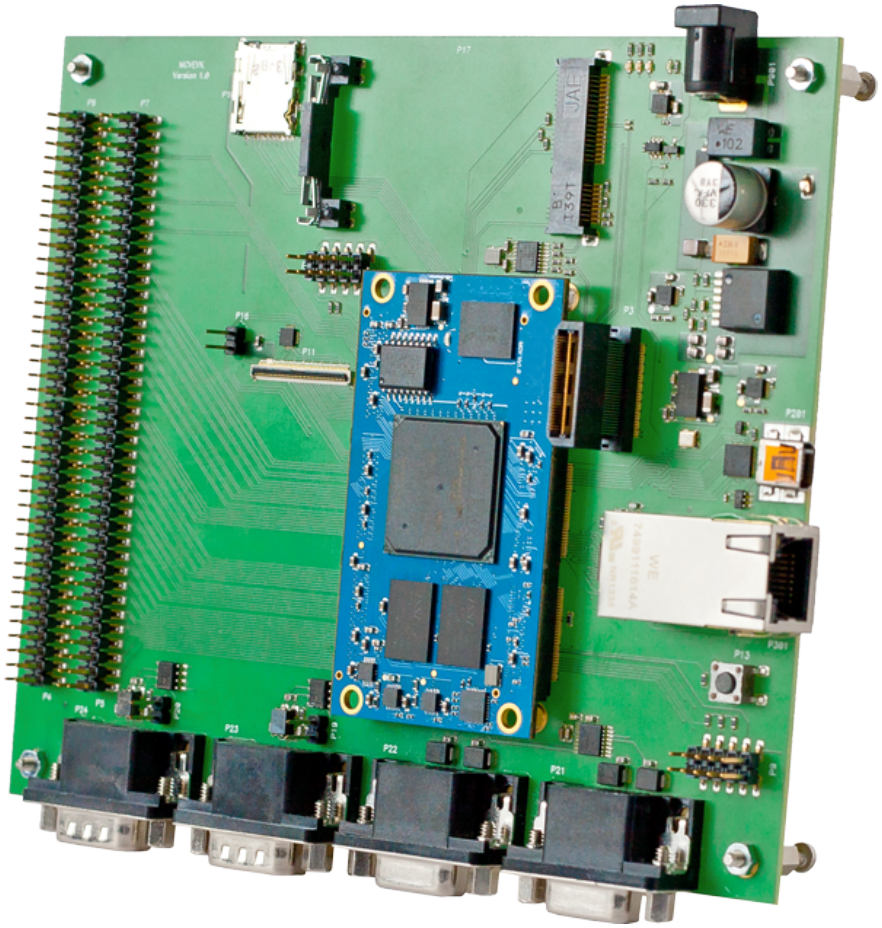
Revision	Date	Revised	Comment
1.0	28.05.2015	aw	Initial creation
1.1	04.07.2016	aw	Transition to pdf documentation Inserted ‘Care and Maintenance’

CHAPTER

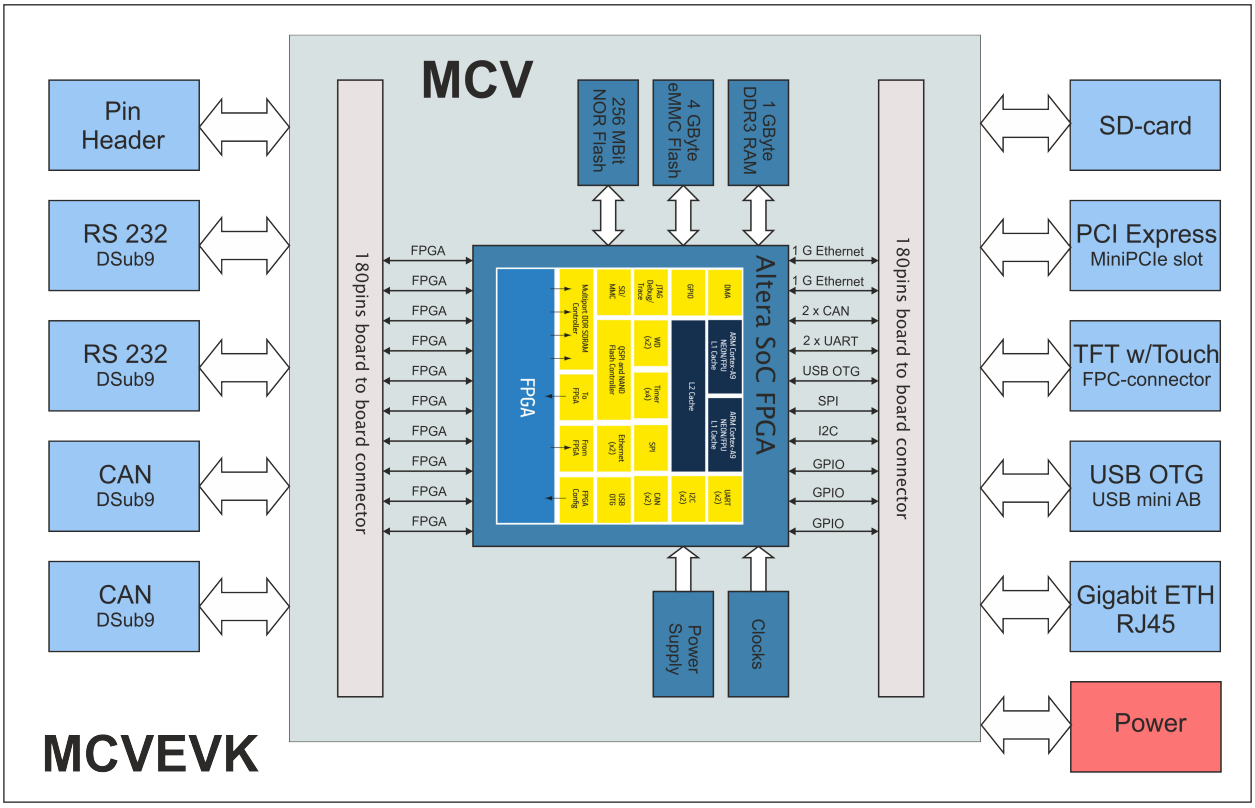
TWO

OVERVIEW

MCVEVK offers a good functionality for evaluation the MCV SoM. As many customers target to use MCV in an industrial environment the MCVEVK interfaces are layed out accordingly.



2.1 Block Diagram

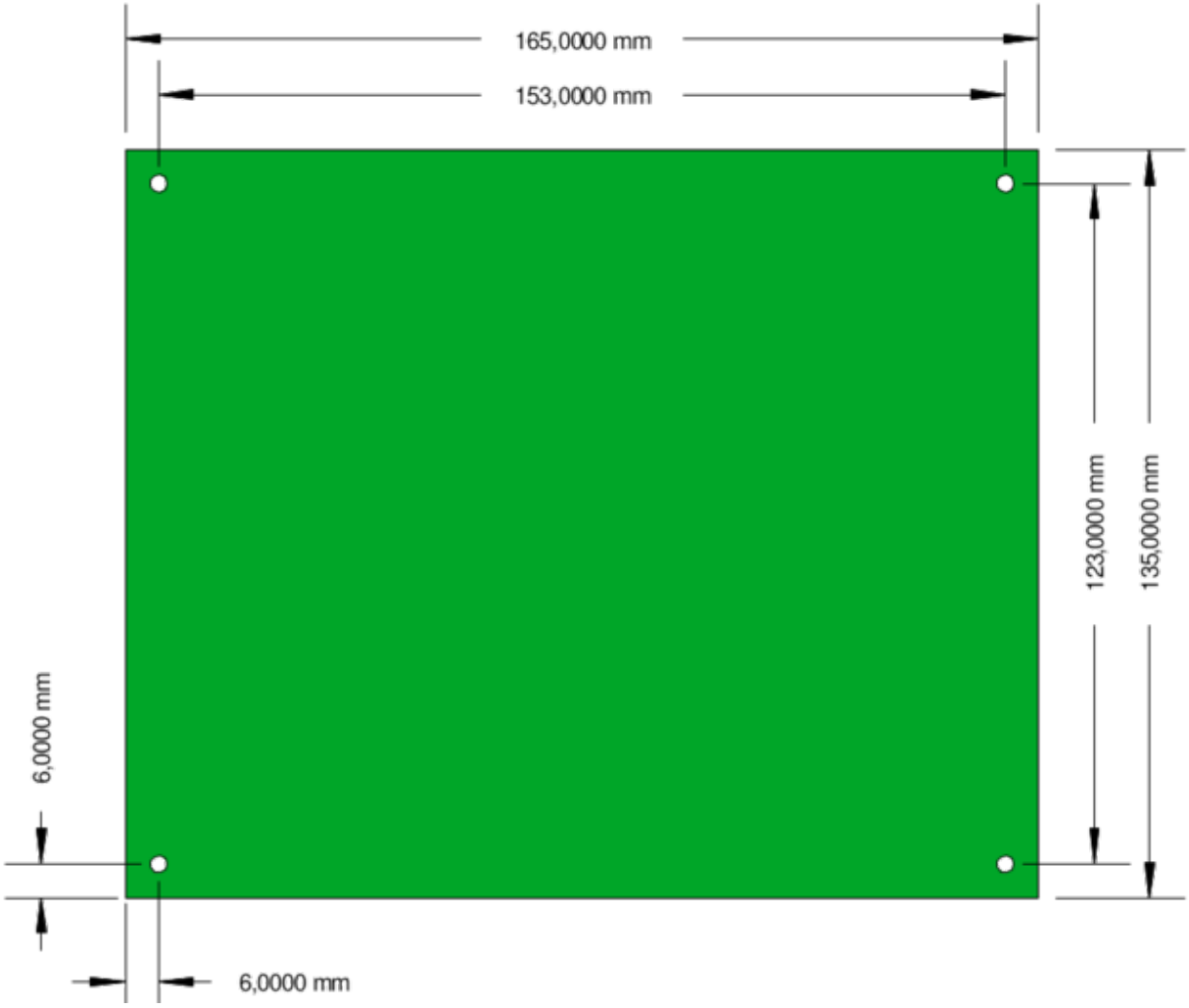


2.2 Feature Set

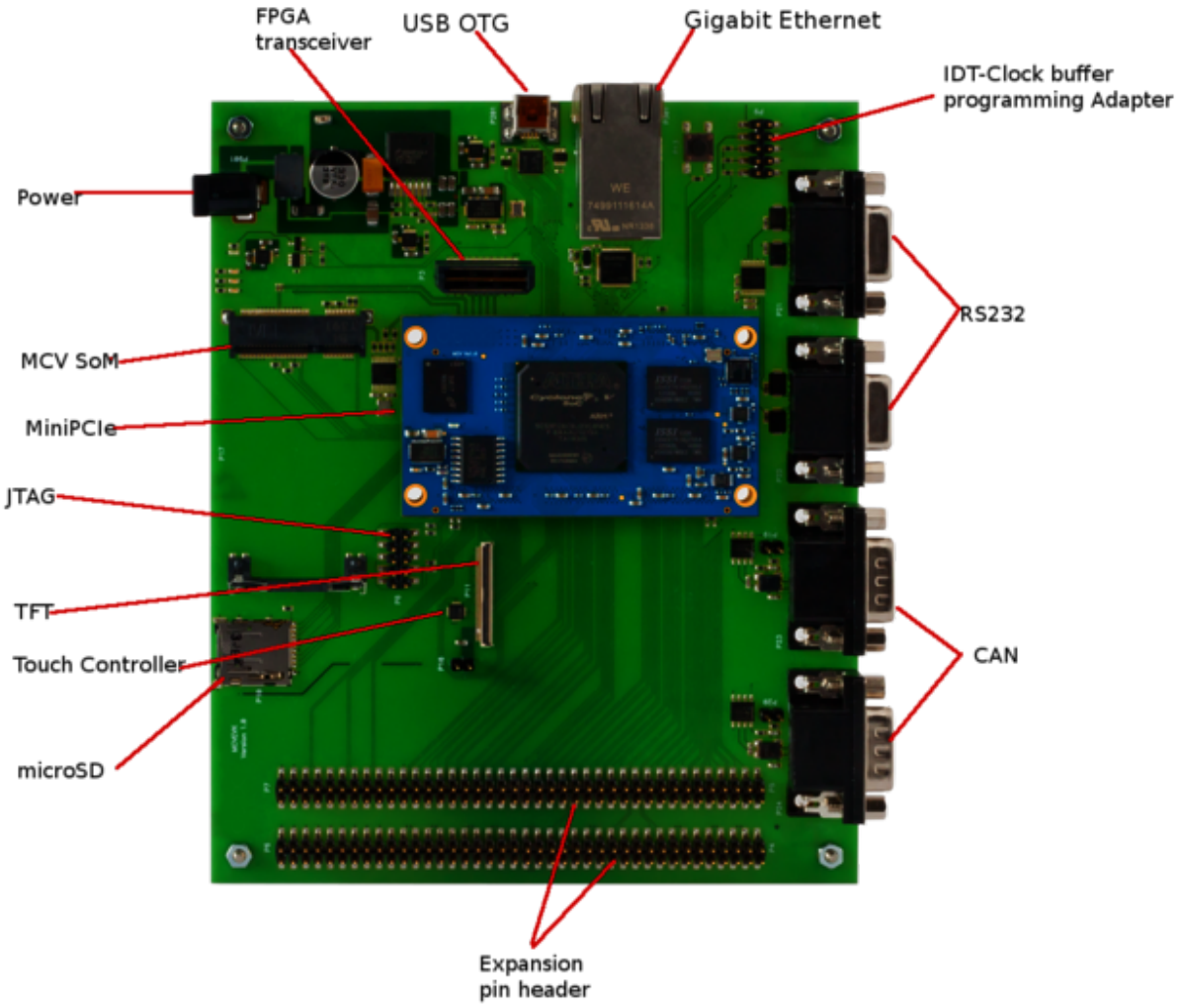
For supporting development projects and fast prototyping in the best possible way MCVEVK supplies

- 1x HPS Gigabit Ethernet on a RJ45 connector
- HPS USB on a micro-USB connector
- 2x UART on a DUSB-9 connector each
- 2x CAN on a DUSB-9 connector each
- TFT with Touch
- Pin Header for FPGA
- miniPCIe slot
- microSD-card slot

2.3 Dimensions



2.4 Parts Location



CHAPTER

THREE

RESOURCES

3.1 Ethernet

MCVEVK offers the EMAC0 Ethernet Port in RGMII mode of the Cyclone V SoC-FPGA. The port can be accessed via the RJ45 connector P301 supported by a Lantiq PEF7071 Phy. The LED D301 shows Gigabit connectivity.

3.2 UART

The two UARTs of the SoC-FPGA HPS are available on a RS232 signal level.

The interface jumpers can be set vertical or honrizontal. The following table shows the signal for horizontal jumer setting, in case of vertical jumper settings RX and TX signals are swapped accordingly.

3.2.1 UART1 – HPS (P21)

Pin	Function	Connector	FPGA Pin
2	RX	P2-138	A22 – HPS_GPIO49
3	TX	P2-132	B21 – HPS_GPIO50
5	GND		

3.2.2 UART2 – HPS (P22)

Pin	Function	Connector	FPGA Pin
2	RX	P1-77	AE12
3	TX	P1-75	AD12
5	GND		

3.3 USB-OTG

MCVEVK supports an USB-OTG port. The TI TUSB1210 USB-OTG Phy drives the physical connection, it is connected to the HPS of the SoC-FPGA by using the ULPI interface running at 1.8V. The respective connector on MCVEVK could be found at position P201.

3.4 CAN

Two CAN ports are available on MCVEVK. The signals on the DSUB connector can optionally be terminated by 120 Ohms.

Function	Connector-Pin	FPGA Pin
CAN0-TX	P2-129	H17 – HPS_GPIO62
CAN0-RX	P2-137	A17 – HPS_GPIO61
CAN1-TX	P2-135	J18 – HPS_GPIO54
CAN1-RX	P2-130	A20 – HPS_GPIO53

3.4.1 CAN1 (P23)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.4.2 CAN2 (P24)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.5 Boot Select

Connector P32 offers the selection of the boot-media as follows:

closed	FPGA boot
open	eMMC boot

3.6 IDT Clock-Buffer

Pin header P9 on the MCVEVK provides the programming and select signals for the IDT Clock buffer on the MCV SoM:

- the SEL[2..0] Signals are equipped with Pull-ups, with no Jumper inserted the default clock set is 7.
- the VBAT Signal is provided on pin 8 of the pin header. An external voltage has to be provided to pin 8 or at least the connection between pin 8 and 10 of the pin header has to be set.
- in case no voltage is provided to VCCBAT, MCV will not work.

3.6.1 Connector P9

Function	Pin	Pin	Function
GND	1	2	SEL0
GND	3	4	SEL1
GND	5	6	SEL2
SDAT	7	8	VCCBAT
SCLK	9	10	VCC18

3.7 JTAG

P8 provides the JTAG signals of the SoC FPGA to the outer world. The JTAG connector complies with the standard Altera pinout, the USB-Blaster or the new USB-Blaster II can directly be connected. The following signals are available:

Function	Pin	Pin	Function
TCK	1	2	GND
TDO	3	4	VCC3V3
TMS	5	6	n.c.
n.c.	7	8	n.c.
TDI	9	10	GND

3.8 miniPCIe

MCVEVK supports a miniPCIe slot on connector P17 as follows:

Pin	Function	Connector	FPGA Pin
1	WAKEn	P1-55	AH6
7	CLK_REQn	P1-53	AH5
11	REFCLKn		
13	REFCLKp		
20	WDISABLE1n	P1-51	AG5
22	PERSTn	P1-49	AH4
23	GXB_RX_L0n	P2-11	AF1
25	GXB_RX_L0p	P2-9	AF2
30	I²C_CLK	P1-47	AH3
31	GXB_TX_L0n	P2-17	AD1
32	I²C_DAT	P1-45	AH2
33	GXB_TX_L0p	P2-15	AD2
51	WDISABLE2n	P1-41	Y5

The reference clocks for miniPCIe are generated using an IDT IDT5V41235:

Function	Connector	FPGA Pin
REFCLK0Lp	P2-3	V5
REFCLK0Ln	P2-5	V4

3.9 Pin Header

Four 40 pin pin header provide IO Pins of MCV. Several resistors are available to select the voltages of the IO-Banks 5A and 8A of the module. Per default the voltages are set to 3.3V.

VCCIO7B is used for the USB Phy and connected to 1.8V. All other HPS Banks are connected to 3.3V.

Voltage	2.5V	3.3V
VCCIO5A	R114	R5
VCCPD5A	R113	R4
VCCIO8A	R112	R3
VCCPD8A	R111	R2

Connector P4:

Function	FPGA	Pin	Pin	FPGA	Function
GND	1	2			VCC33
IOB4A34	AA19	3	4	AC22	IOB4A36
IOB4A35	AA18	5	6	AC23	IOB4A37
IOB4A38	AD23	7	8	AF27	IOB4A40
IOB4A39	AE22	9	10	AF28	IOB4A41
GND		11	12		VCC33
IOB4A42	AG28	13	14	AG26	IOB4A44
IOB4A43	AH27	15	16	AH26	IOB4A45
IOB4A0	Y15	17	18	AF25	IOB4A46
IOB4A1	AA15	19	20	AG25	IOB4A47
GND		21	22		VCC33
IOB4A2	U14	23	24	AG24	IOB4A48
IOB4A3	U13	25	26	AH24	IOB4A49
IOB4A52	AG21	27	28	AH23	IOB4A50
IOB4A53	AH21	29	30	AH22	IOB4A51
GND		31	32		VCC33
IOB4A12	AF21	33	34	AG19	IOB4A54
IOB4A13	AF22	35	36	AH19	IOB4A55
IOB4A58	AH17	37	38	AG18	IOB4A56
IOB4A59	AH16	39	40	AH18	IOB4A57

Connector P5:

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		VCC33
IOB5A8	Y16	3	4	AA24	IOB5A10
IOB5A9	W15	5	6	AA23	IOB5A11
IOB5A12	AC24	7	8	AF26	IOB5A14
IOB5A13	AB23	9	10	AE26	IOB5A15
GND		11	12		VCC33
IOB5A2	V16	13	14	AE25	IOB5A0
IOB5A3	V15	15	16	AD26	IOB5A1
IOB5A6	AA20	17	18	Y17	IOB5A4
IOB5A7	Y19	19	20	Y18	IOB5A5
GND		21	22		VCC33
IOB4A4	AE20	23	24	AE24	IOB4A6
IOB4A5	AD20	25	26	AE23	IOB4A7
IOB4A8	AD19	27	28	AG20	IOB4A10
IOB4A9	AE19	29	30	AF20	IOB4A11
GND		31	32		VCC33
IOB4A14	AF23	33	34	AF18	IOB4A16
IOB4A15	AG23	35	36	AH12	IOB4A17
IOB4A18	AG13	37	38	Y13	IOB4A20
IOB4A19	AF13	39	40	AA13	IOB4A21

Connector P6:

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		VCC33
IOB4A62	AG15	3	4	AF17	IOB4A60
IOB4A63	AH14	5	6	AG16	IOB4A61
IOB4A66	AG11	7	8	AG14	IOB4A64
IOB4A67	AH11	9	10	AH13	IOB4A65
GND		11	12		VCC33
IOB3B20	AF11	13	14	AE11	IOB3B18
IOB3B21	AF10	15	16	AD11	IOB3B19
IOB3B24	AF7	17	18	AD10	IOB3B22
IOB3B25	AG6	19	20	AE9	IOB3B23
GND		21	22		VCC33
HPS_GPI4 (1.5V)	R28	23	24	U25	HPS_GPI3 (1.5V)
HPS_GPIO51	T26	25	26	AC27	HPS_GPI12 (1.5V)
HPS_GPIO60	P26	27	28	T17	HPS_GPIO48
HPS_GPIO63	U15	29	30	U16	HPS_GPIO65
HPS_GPIO66	A21	31	32	C21	HPS_GPIO52
HPS_GPIO64	J17	33	34	B19	HPS_GPIO58
HPS_GPIO19 (1.8V)	C19	35	36	K18	HPS_GPIO20 (1.8V)
HPS_GPIO21 (1.8V)	B16	37 38		C17	HPS_GPIO35 (1.8V)
HPS_GPIO44	H16	39	40	A6	HPS_GPIO34 (1.8V)

Connector P7:

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		VCC33
IOB4A22	W14	3	4	AD17	IOB4A24
IOB4A23	V13	5	6	AE17	IOB4A25
IOB4A26	AF15	7	8	AG8	IOB4A28
IOB4A27	AE15	9	10	AH7	IOB4A29
GND		11	12		VCC33
IOB4A32	AG10	13	14	AG9	IOB4A30
IOB4A33	AH9	15	16	AH8	IOB4A31
IOB3B0		17	18		IOB3B1
HPS_GPI0		19	20		IOB3B2
GND		21	22		GND
IOB5B0 L10		23	24	E11	IOB8A0
IOB5B1 L9		25	26	D11	IOB8A1
IOB5B2 L8		27	28	E8	IOB8A2
IOB5B3 K8		29	30	D8	IOB8A3
GND		31	32		GND
IOB5B4 H5		33	34	C16	HPS_GPIO26 (1.8V)
IOB5B5 H6		35	36	B14	HPS_GPIO28 (1.8V)
HPS_GPIO27 (1.8V)	J16	37	38	C14	HPS_GPIO14 (1.8V)
HPS_GPIO33 (1.8V)	A8	39	40	A7	HPS_GPIO37

3.10 Pin Multiplexing

When used on the MCVEVK baseboard MCV supports the follwing pin multiplexing:

3.10.1 EMAC0

EMAC0	SoM pin	Function	FPGA pin
INT	P2 122	HPS_GPIO 59	B18
RX_CLK	P2 118	HPS_GPIO 10	G4
RX_CTL	P2 117	HPS_GPIO 8	F4
RXD0	P2 110	HPS_GPIO 5	C8
RXD1	P2 116	HPS_GPIO 11	C5
RXD2	P2 111	HPS_GPIO 12	E5
RXD3	P2 109	HPS_GPIO 13	D5
TX_CLK	P2 113	HPS_GPIO 0	E4
TX_CTL	P2 114	HPS_GPIO 9	C6
TXD0	P2 106	HPS_GPIO 1	C10
TXD1	P2 107	HPS_GPIO 2	F5
TXD2	P2 108	HPS_GPIO 3	C9
TXD3	P2 105	HPS_GPIO 4	C4
MDIO	P2 115	HPS_GPIO 6	D4
MDC	P2 112	HPS_GPIO 7	C7

3.10.2 USB1

USB 1	SoM pin	Function	FPGA pin
D0	P2 100	HPS_GPIO 15	A16
D1	P2 87	HPS_GPIO 16	J14
D2	P2 98	HPS_GPIO 17	A15
D3	P2 99	HPS_GPIO 18	D17
D4	P2 85	HPS_GPIO 22	J13
D5	P2 86	HPS_GPIO 23	A12
D6	P2 82	HPS_GPIO 24	J12
D7	P2 84	HPS_GPIO 25	A11
CLK	P2 83	HPS_GPIO 29	A8
NXT	P2 88	HPS_GPIO 32	J16
DIR	P2 81	HPS_GPIO 31	A7
STP	P2 95	HPS_GPIO 30	H16

3.10.3 CAN0

CAN 0	SoM pin	Function	FPGA pin
RX	P2 137	HPS_GPIO 61	A17
TX	P2 129	HPS_GPIO 62	H17

3.10.4 CAN1

CAN 1	SoM pin	Function	FPGA pin
RX	P2 130	HPS_GPIO 53	A20
TX	P2 124	HPS_GPIO 54	J18

3.10.5 UART0

UART0	SoM pin	Function	FPGA pin
RX	P2 138	HPS_GPIO 49	A22
TX	P2 132	HPS_GPIO 50	B21

3.10.6 UART1

UART1	SoM pin	Function	FPGA pin
RX	P2 77	IO B3 B16	AE12
TX	P2 75	IO B3 B17	AD12

3.10.7 I2C0

I2C0	SoM pin	Function	FPGA pin
SDA	P2 126	HPS_GPIO 55	A19
SCL	P2 139	HPS_GPIO 56	C18
TOUCH_INT	P2 124	HPS_GPIO 57	A18

3.10.8 LCD

FPGA-LCD	SoM pin	Function	FPGA pin
LCD_R0	P1 30	IO B3 A6	AA11
LCD_R1	P1 32	IO B3 A5	AD5
LCD_R2	P1 34	IO B3 A4	AE6
LCD_R3	P1 36	IO B3 A3	AD4
LCD_R4	P1 38	IO B3 A2	AC4
LCD_R5	P1 40	IO B3 A1	AA4
LCD_G0	P1 42	IO B3 A0	AB4
LCD_G1	P1 46	IO B3 B15	AF9
LCD_G2	P1 48	IO B3 B14	AE8
LCD_G3	P1 50	IO B3 B13	AF8
LCD_G4	P1 52	IO B3 B12	AE7
LCD_G5	P1 54	IO B3 B11	AF4
LCD_B0	P1 56	IO B3 B10	AE4
LCD_B1	P1 58	IO B3 B9	AF6
LCD_B2	P1 60	IO B3 B8	AF5
LCD_B3	P1 64	IO B3 B7	W11
LCD_B4	P1 66	IO B3 B6	V11
LCD_B5	P1 68	IO B3 B5	U11
LCD_DE	P1 72	IO B3 B3	W12
LCD_DIM	P1 70	IO B3 B4	T11
LCD_CLK	P1 28	IO B3 A7	Y11

3.10.9 Connector P4

FPGA pin	Function	SoM pin	P 4	SoM pin	Function	FPGA pin
	GND		1 | 2		Vcc	
AA19	IO B4 A34	P1 155	3 | 4	P1 151	IO B4 A36	AC22
AA18	IO B4 A35	P1 153	5 | 6	P1 149	IO B4 A37	AC23
AD23	IO B4 A38	P1 147	7 | 8	P1 143	IO B4 A40	AF27
AE22	IO B4 A39	P1 145	9 | 10	P1 141	IO B4 A41	AF28
	GND		11 | 12		Vcc	
AG28	IO B4 A42	P1 137	13 | 14	P1 133	IO B4 A44	AG26
AH27	IO B4 A43	P1 135	15 | 16	P1 131	IO B4 A45	AH26
Y15	IO B4 A0	P1 156	17 | 18	P1 129	IO B4 A46	AF25
AA15	IO B4 A1	P1 154	19 | 20	P1 127	IO B4 A47	AG25
	GND		21 | 22		Vcc	
U14	IO B4 A2	P1 152	23 | 24	P1 125	IO B4 A48	AG24
U13	IO B4 A3	P1 150	25 | 26	P1 123	IO B4 A49	AH24
AG21	IO B4 A52	P1 115	27 | 28	P1 119	IO B4 A50	AH23
AH21	IO B4 A53	P1 113	29 | 30	P1 117	IO B4 A51	AH22
	GND		31 | 32		Vcc	
AF21	IO B4 A12	P1 130	33 | 34	P1 111	IO B4 A54	AG19
AF22	IO B4 A13	P1 128	35 | 36	P1 109	IO B4 A55	AH19
AH17	IO B4 A58	P1 101	37 | 38	P1 107	IO B4 A56	AG18
AH16	IO B4 A59	P1 99	39 | 40	P1 105	IO B4 A57	AH18

3.10.10 Connector P5

FPGA pin	Function	SoM pin	P 5		SoM pin	Function	FPGA pin
	GND		1	2			Vcc
Y16	IO B5 A8	P1 173	3	4	P1 169	IO B5 A10	AA24
W15	IO B5 A9	P1 171	5	6	P1 167	IO B5 A11	AA23
AC24	IO B5 A12	P1 165	7	8	P1 161	IO B5 A14	AF26
AB23	IO B5 A13	P1 163	9	10	P1 159	IO B5 A15	AE26
	GND		11	12		Vcc	
V16	IO B5 A2	P1 170	13	14	P1 174	IO B5 A0	AE25
V15	IO B5 A3	P1 168	15	16	P1 172	IO B5 A1	AD26
AA20	IO B5 A6	P1 162	17	18	P1 166	IO B5 A4	Y17
Y19	IO B5 A7	P1 160	19	20	P1 164	IO B5 A5	Y18
	GND		21	22		Vcc	
AE20	IO B4 A4	P1 148	23	24	P1 144	IO B4 A6	AE24
AD20	IO B4 A5	P1 146	25	26	P1 142	IO B4 A7	AE23
AD19	IO B4 A8	P1 138	27	28	P1 134	IO B4 A10	AG20
AE19	IO B4 A9	P1 136	29	30	P1 132	IO B4 A11	AF20
	GND		31	32			Vcc
AF23	IO B4 A14	P1 126	33	34	P1 120	IO B4 A16	AF18
AG23	IO B4 A15	P1 124	35	36	P1 118	IO B4 A17	AH12
AG13	IO B4 A18	P1 116	37	38	P1 112	IO B4 A20	Y13
AF13	IO B4 A19	P1 114	39	40	P1 110	IO B4 A21	AA13

3.10.11 Connector P6

FPGA pin	Function	SoM pin	P 6		SoM pin	Function	FPGA pin
	GND		1	2		Vcc	
AG15	IO B4 A62	P1 93	3	4	P1 97	IO B4 A60	AF17
AH14	IO B4 A63	P1 91	5	6	P1 95	IO B4 A61	AG16
AG11	IO B4 A66	P1 83	7	8	P1 89	IO B4 A64	AG14
AH11	IO B4 A67	P1 81	9	10	P1 87	IO B4 A65	AH13
	GND		11	12		Vcc	
AF11	IO B3 B20	P1 69	13	14	P1 73	IO B3 B18	AE11
AF10	IO B3 B21	P1 67	15	16	P1 71	IO B3 B19	AD11
AF7	IO B3 B24	P1 59	17	18	P1 65	IO B3 B22	AD10
AG6	IO B3 B25	P1 57	19	20	P1 63	IO B3 B23	AE9
	GND		21	22		Vcc	
R28	HPS_GPI 4	P2 148	23	24	P2 154	HPS_GPI 3	U25
A21	HPS_GPIO 51	P2 134	25	26	P2 152	HPS_GPI 12	AC27
J17	HPS_GPIO 60	P2 133	27	28	P2 136	HPS_GPIO 48	C21
C19	HPS_GPIO 63	P2 127	29	30	P2 128	HPS_GPIO 65	B19
C16	HPS_GPIO 66	P2 123	31	32	P2 131	HPS_GPIO 52	K18
B16	HPS_GPIO 64	P2 121	33	34	P2 125	HPS_GPIO 58	C17
A14	HPS_GPIO 19	P2 94	35	36	P2 97	HPS_GPIO 20	E16
A13	HPS_GPIO 21	P2 90	37	38	P2 96	HPS_GPIO 35	B14
B12	HPS_GPIO 44	P2 71	39	40	P2 92	HPS_GPIO 34	C14

3.10.12 Connector P7

FPGA pin	Function	SoM pin	P 7		SoM pin	Function	FPGA pin
	GND		1	2		Vcc	
W14	IO B4 A22	P1 108	3	4	P1 102	IO B4 A24	AD17
V13	IO B4 A23	P1 106	5	6	P1 100	IO B4 A25	AE17
AF15	IO B4 A26	P1 98	7	8	P1 94	IO B4 A28	AG8
AE15	IO B4 A27	P1 96	9	10	P1 92	IO B4 A29	AH7
	GND		11	12		Vcc	
AG10	IO B4 A32	P1 84	13	14	P1 90	IO B4 A30	AG9
AH9	IO B4 A33	P1 82	15	16	P1 88	IO B4 A31	AH8
T12	IO B3 B0	P1 78	17	18	P1 76	IO B3 B1	T13
V24	HPS_GPI 0	P2 156	19	20	P1 74	IO B3 B2	V12
	GND		21	22		GND	
L10/ Y24	IO B5 B0	P1 24	23	24	P1 21	IO B8 A0	E11
L9 / W24	IO B5 B1	P1 22	25	26	P1 19	IO B8 A1	D11
L8 /AB26	IO B5 B2	P1 20	27	28	P1 17	IO B8 A2	E8
K8 /AA26	IO B5 B3	P1 18	29	30	P1 15	IO B8 A3	D8
	GND		31	32		GND	
H5 / W21	IO B5 B4	P1 16	33	34	P2 93	HPS_GPIO 26	C15
H6 / W20	IO B5 B5	P1 14	35	36	P2 91	HPS_GPIO 28	D15
A9	HPS_GPIO 27	P2 80	37	38	P2 89	HPS_GPIO 14	J15
A6	HPS_GPIO 33	P2 79	39	40	P2 70	HPS_GPIO 37	A5

3.10.13 PCI Express

FPGA-PCIe	SoM pin	Function	FPGA pin
PCIE_WAKE n	P1 55	IO B3 B26	AH6
PCIE_CLKREQ n	P1 53	IO B3 B27	AH5
PCIE_WDISABLE1 n	P1 51	IO B3 B28	AG5
PCIE_WDISABLE2 n	P1 41	IO B3 A8	Y5
PCIE_PERST n	P1 49	IO B3 B29	AH4
PCIE_I2C_CLK	P1 47	IO B3 B30	AH3
PCIE_I2C_DAT	P1 45	IO B3 B31	AH2

3.11 Reset Button

Button P13 is connected to the HPS_RSTn signal of MCV.

3.12 LCD Interface

Many applications in the world of applications based on ARN architecture require display support. MCVEVK offers a TFT display interface, the MCV reference implementation offers a display controller IP. The TFT interface is implemented on the followinig signals:

Pin	Function	Connector	FPGA Pin
1			
Continued on next page			

Table 3.1 – continued from previous page

Pin	Function	Connector	FPGA Pin
2			
3			
4	Backlight		
5	Backlight		
6	Backlight		
7	VCC33		
8			
9	LCD_DE	P1-72	W12
10	Touch XP1		
11	Touch YP1		
12	LCD_DIM	P1-70	T11
13	LCD_B5	P1-68	U11
14	LCD_B4	P1-66	V11
15	LCD_B3	P1-64	W11
16	GND		
17	LCD_B2	P1-60	AF5
18	LCD_B1	P1-58	AF6
19	LCD_B0	P1-56	AE4
20	GND		
21	LCD_G5	P1-54	AF4
22	LCD_G4	P1-52	AE7
23	LCD_G3	P1-50	AF8
24	GND		
25	LCD_G2	P1-48	AE8
26	LCD_G1	P1-46	AF9
27	LCD_G0	P1-42	AB4
28	GND		
29	LCD_R5	P1-40	AA4
30	LCD_R4	P1-38	AC4
31	LCD_R3	P1-36	AD4
32	GND		
33	LCD_R2	P1-34	AE6
34	LCD_R1	P1-32	AD5
35	LCD_R0	P1-30	AA11
36	Touch XMI		
37	Touch YMI		
38	LCD_CLK	P1-28	Y11
39	GND		
40			

3.13 Touch Controller

The Touch Controller uses an I²C interface to connect to the FPGA. The interface is available on the following location:

Function	Connector	FPGA Pin
SDAT	P2-126	A19 – HPS_GPIO55
SCLK	P2-139	C18 – HPS_GPIO56
INTn	P2-124	A18 – HPS_GPIO57

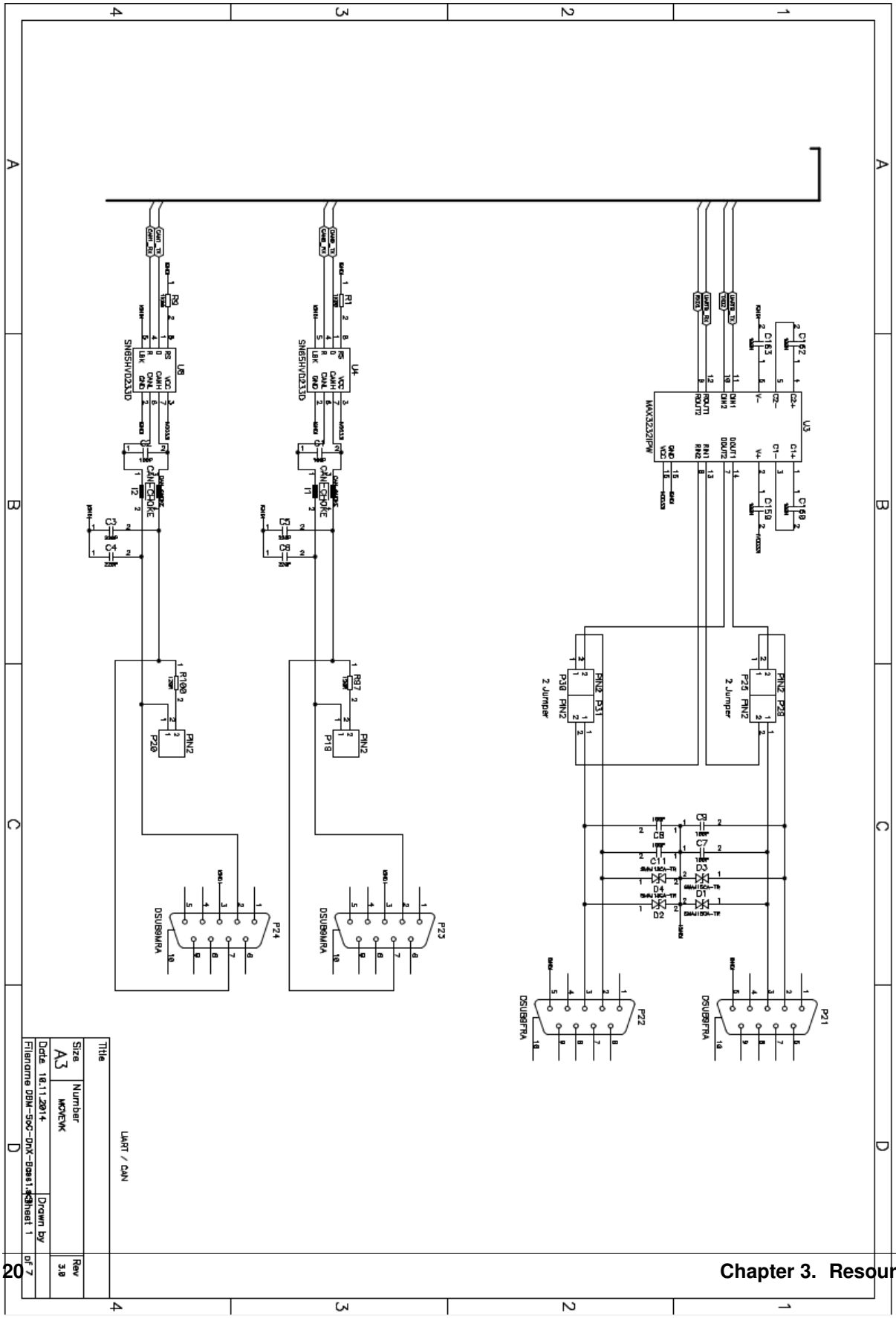
3.14 Transceiver Pin Header

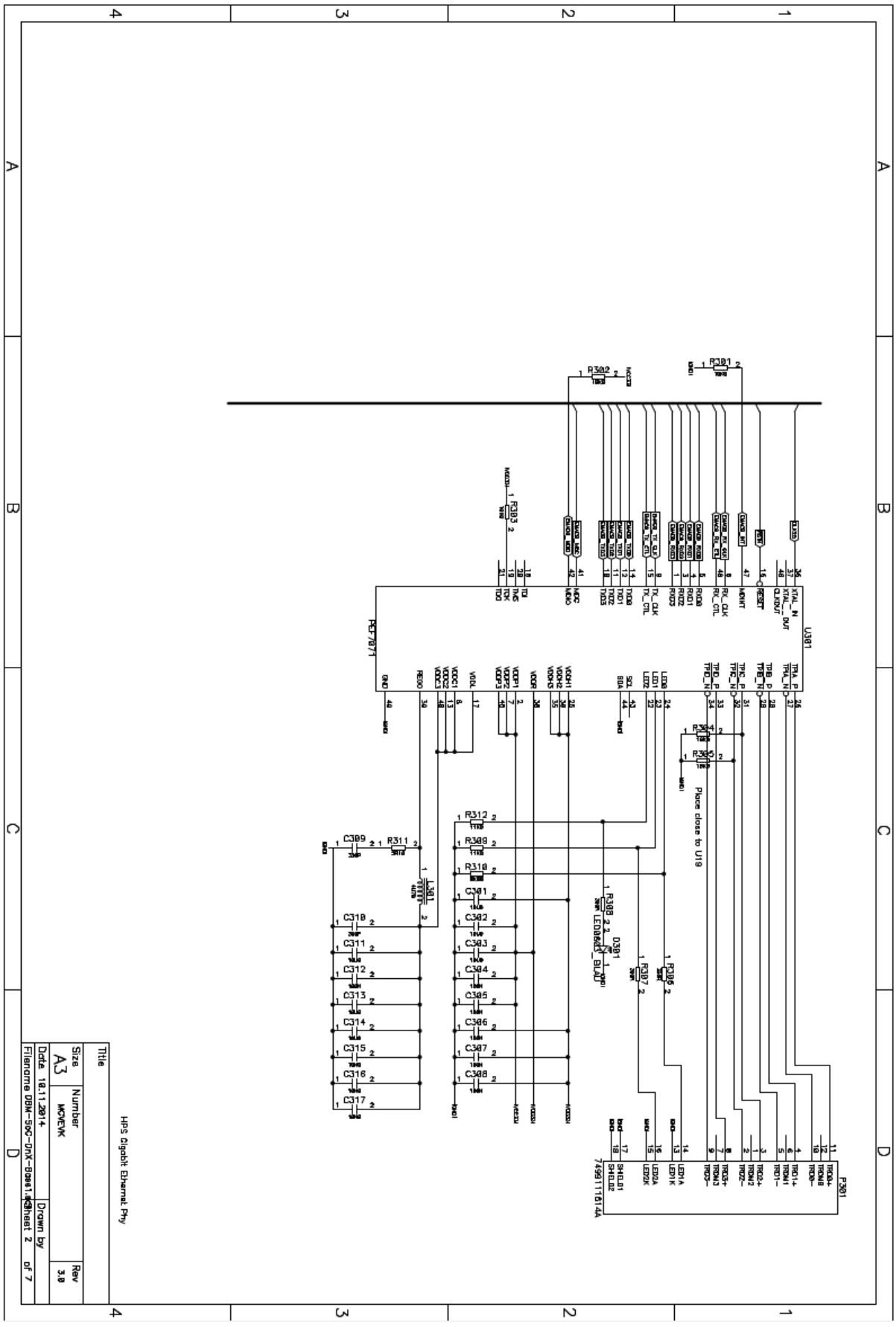
Connector P3 supplies the SoC FPGA transceiver signals on a Samtec QTH-030-03-F-D-A pinheader.

P3 provides the following pin out:

Function	FPGA Pin	Pin	Pin	FPGA	Function
GND		1	2		GND
REFCLK1Lp	P8	3	4		
REFCLK1Ln	N8	5	6		
GND		7	8		GND
GXB_RX_L3p	P2	9	10		
GXB_RX_L3n	P1	11	12		
GND		13	14		GND
GXB_TX_L3p	M2	15	16		
GXB_TX_L3n	M1	17	18		
GND		19	20		GND
GXB_RX_L4p	K2	21	22	AB2	GXB_RX_L1p
GXB_RX_L4n	K1	23	24	AB1	GXB_RX_L1n
GND		25	26		GND
GXB_TX_L4p	H2	27	28	Y2	GXB_TX_L1p
GXB_TX_L4n	H1	29	30	Y1	GXB_TX_L1n
GND		31	32		GND
GXB_RX_L5p	F2	33	34	V2	GXB_RX_L2p
GXB_RX_L5n	F1	35	36	V1	GXB_RX_L2n
GND		37	38		GND
GXB_TX_L5p	D2	39	40	T2	GXB_TX_L2p
GXB_TX_L5n	D1	41	42	T1	GXB_TX_L2n
GND		43	44		GND
		45	46		
		47	48		
GND		49	50		GND
		51	52		
		53	54		
GND		55	56		GND
CLKextC		57	58		CLKextA
CLKextD		59	60		CLKextB

3.15 Schematics




U301
88E1111
R301
R302
R303
R304
R305
R306
R307
R308
R309
R310
R311
R312
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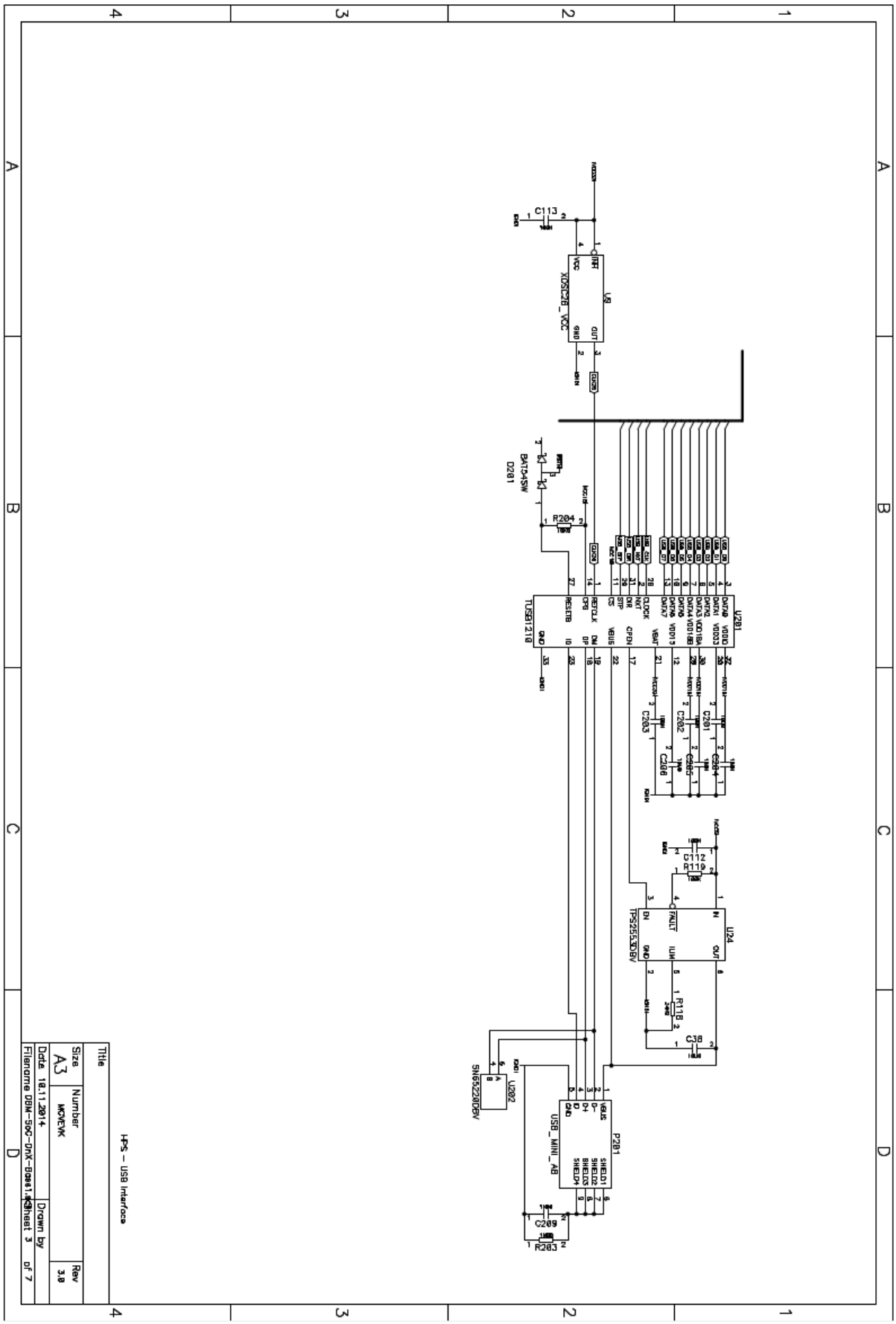
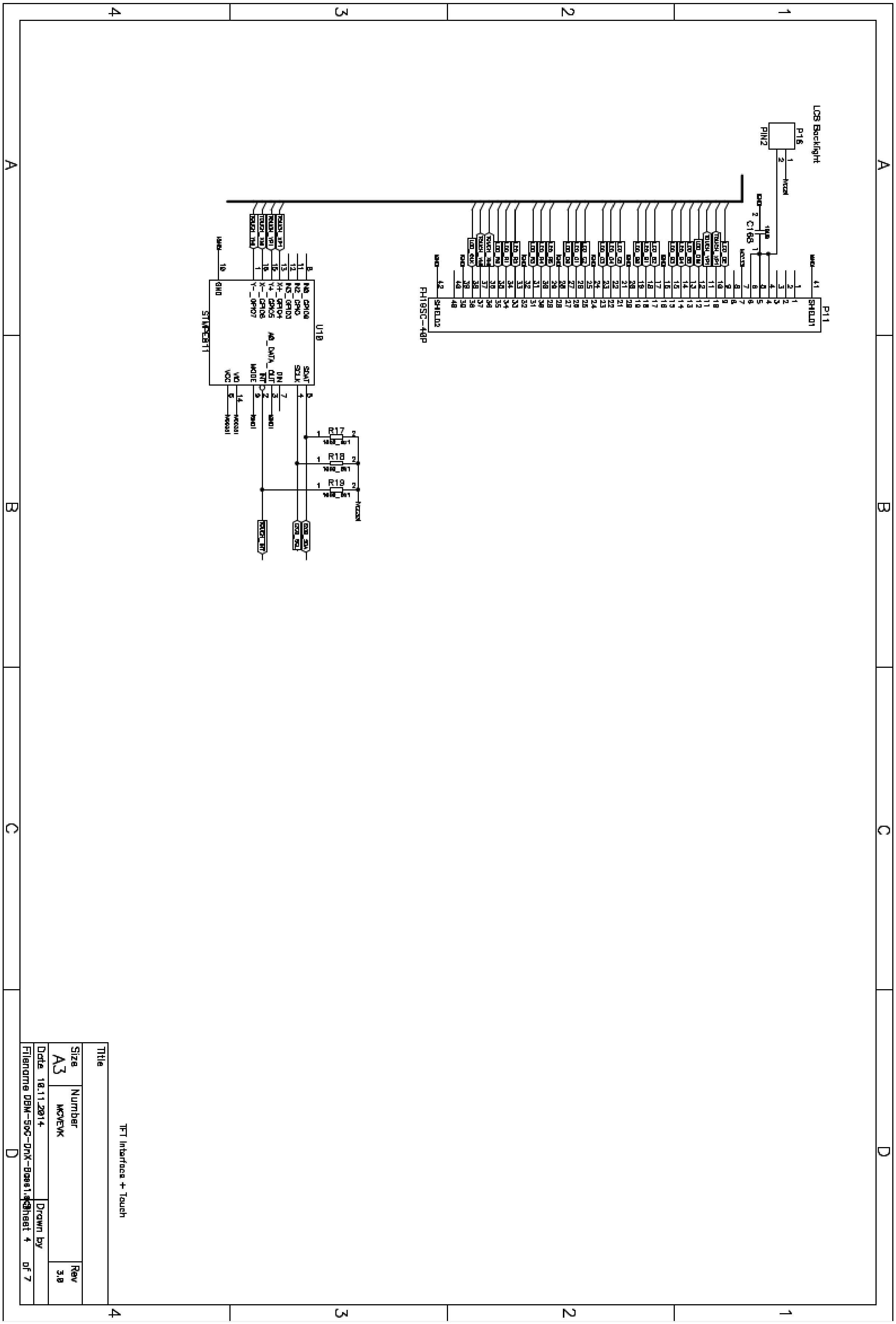
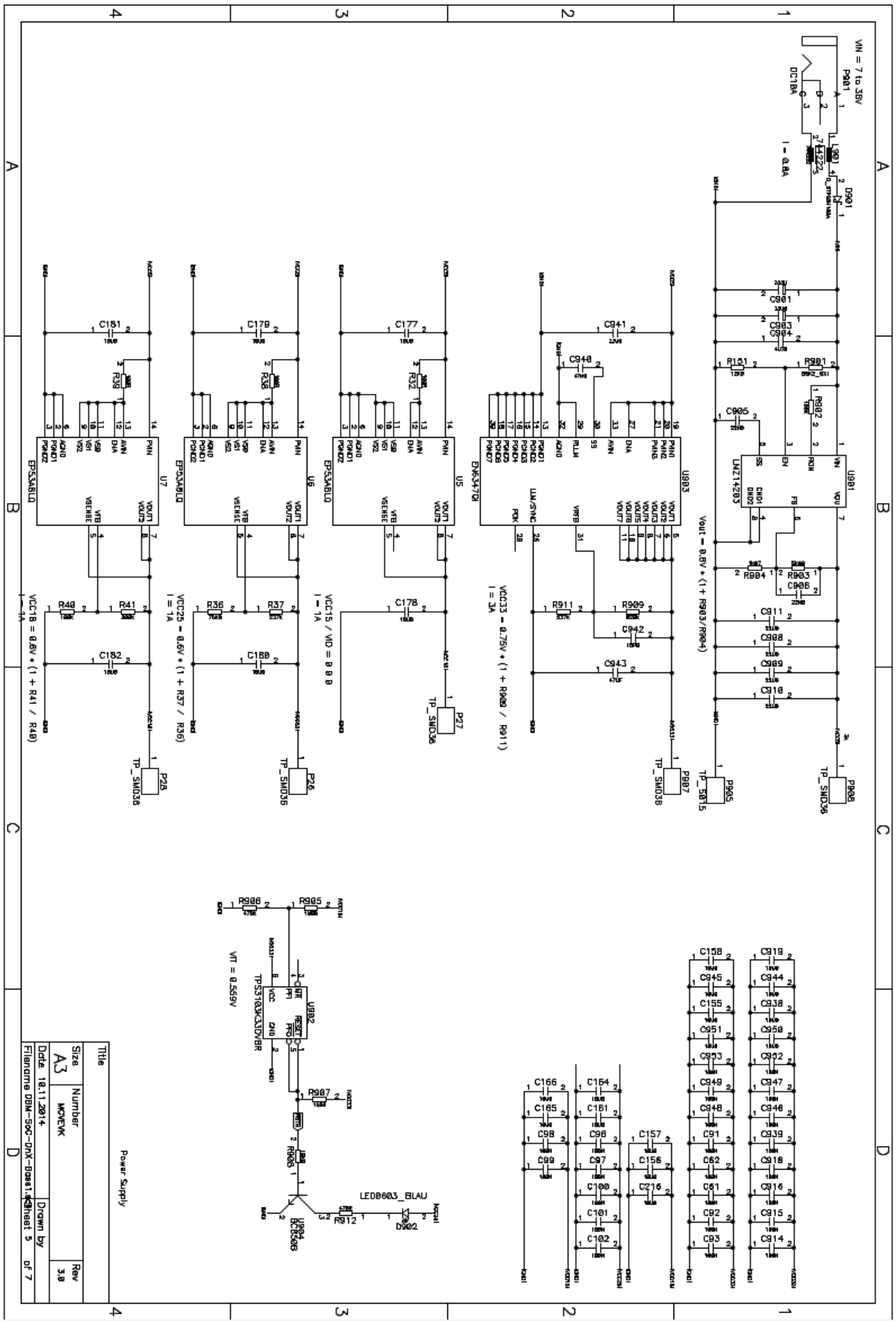
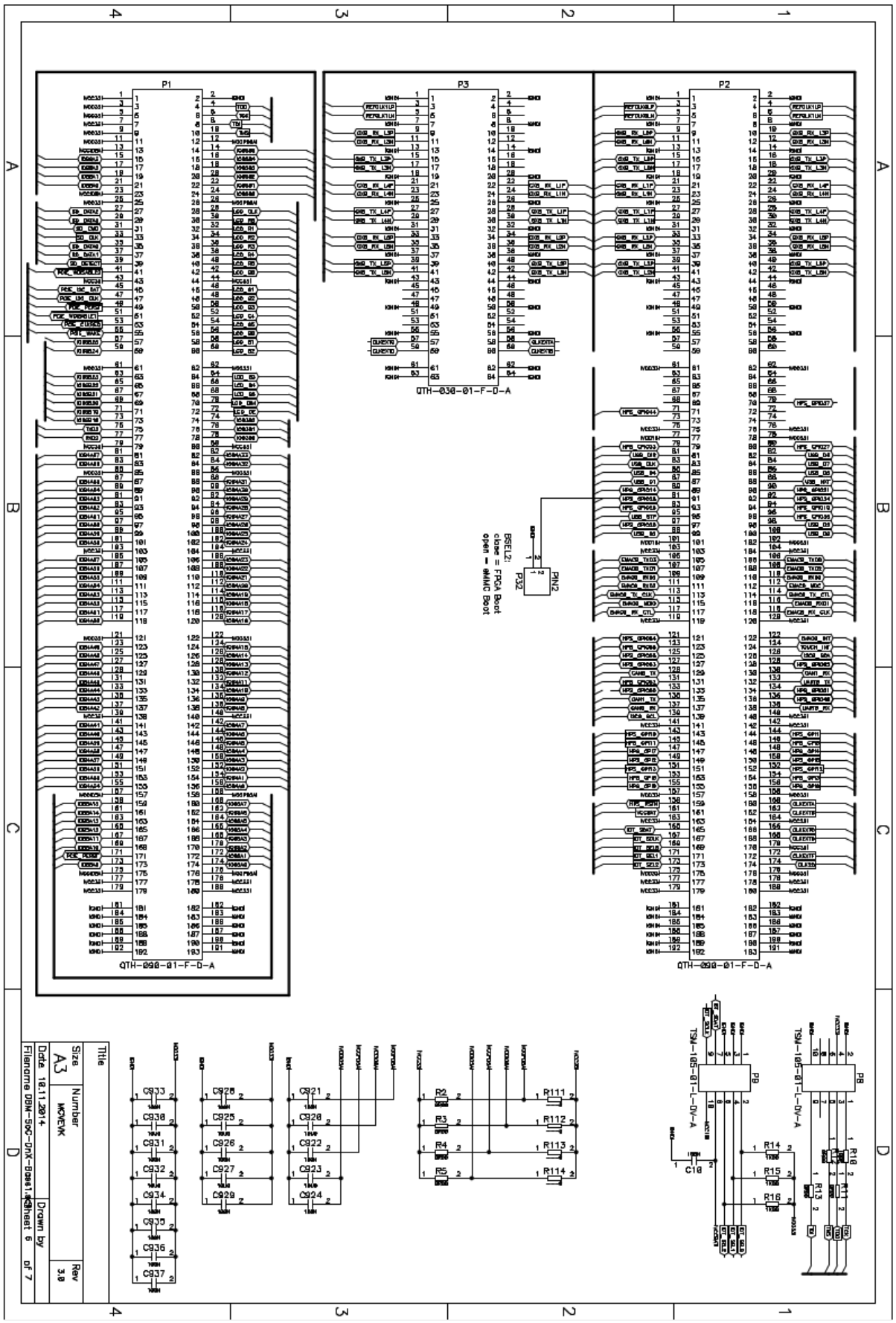
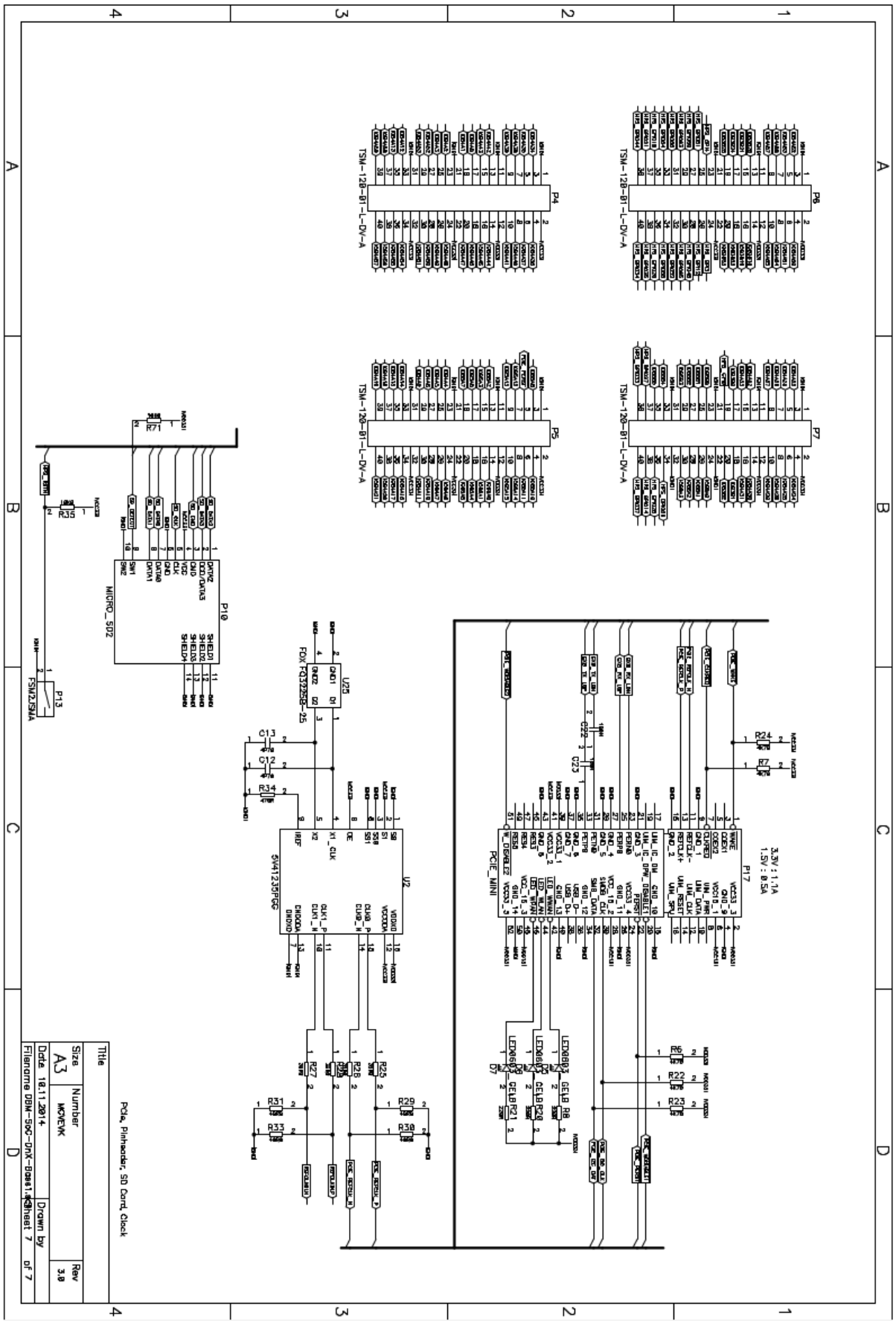
C303
C304
C305
C306
C307
C308
C309
C310
C311
C312
C313
C314
C315
C316
C317
C318
L301
D301
P301
Place close to U19
HPS Gigabit Ethernet Phy
Title
Size
A3
Number
MCVEVK
Rev
3.0
Date: 18.11.2014
Drawn by:
Filename: DBM-SoC-DnX-Base1.SchDoc
Sheet 2 of 7


HPS – USB Interface
Title
Size
A3
Number
MCVEVK
Rev
3.0
Date
18.11.2014
Drawn by
Filename
DBM-SoC-DnX-Base1.SchDoc
Sheet
3
of
7
U8
XC6SC28_VCC
C113
D201
BAT54SW
R204
U201
TUSB1210
C201
C202
C203
C204
C205
C206
C112
R119
U24
TPS2553DBV
R118
C38
U202
SN65220DBV
P201
USB_MINI_AB
C209
R203


LCD Backlight
P16
PIN2
C168
P11
SHIELD1
SHIELD2
FH19SC-40P
U18
STMPE811
R17
R18
R19
Title
TFT Interface + Touch
Size
A3
Number
MCVEVK
Rev
Date 10.11.2014
Drawn by
Sheet 4 of 7


VIN = 7 to 35V
Vout = 0.8V * (1 + R903/R904)
VCC18 = 0.8V * (1 + R41 / R40)
VCC25 = 0.6V * (1 + R37 / R36)
VCC15 / VID = 0 0 0
VCC033 = 0.75V * (1 + R905 / R911)
VTT = 0.569V
LED0603_BLAU
Power Supply
Size A3
Number MCVEVK
Rev 3.0
Date 18.11.2014
Drawn by
Filename DBM-SVC-DnX-Base1.SchDoc
Sheet 5 of 7


P1
QTH-090-01-F-D-A
P3
QTH-030-01-F-D-A
P2
QTH-090-01-F-D-A
P32
PIN2
BSEL2:
close = FPGA Boot
open = eMMC Boot
P9
TSW-105-01-L-DV-A
C933
C930
C931
C932
C934
C935
C936
C937
C928
C925
C926
C927
C929
C921
C920
C922
C923
C924
R2
R3
R4
R5
R111
R112
R113
R114
C10
R14
R15
R16
R18
R13
R11
Title
Size
A3
Number
MCVEVK
Rev
3.0
Date 18.11.2014
Drawn by
Filename DBM-SMC-DnX-Base1.4
Sheet 6 of 7


PCIe, Pinheader, SD Card, Clock
Title
Size
A3
Number
MCVEVK
Rev
3.0
Date: 18.11.2014
Drawn by:
Filename: DBM-SVC-DNX-Base1.SchDoc
Sheet 7 of 7
3.3V : 1.1A
1.5V : 0.5A

3.16 Layout Diagram