MAX Hardware Manual

Release 1

ARIES Embedded GmbH

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

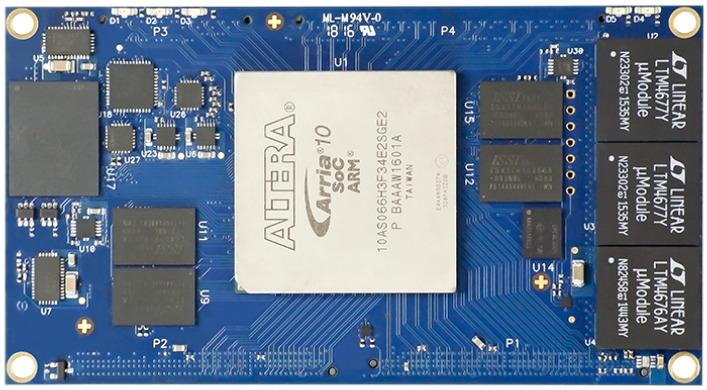
1.6 Change Log

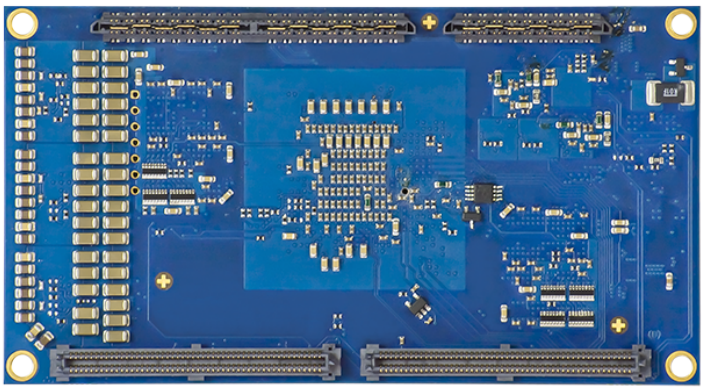
Revision	Date	Revised	Comment
1.0	01.04.2019	aw	Initial creation
1.1	24.07.2020	aw	Missing signals P2 added

CHAPTER

TWO

OVERVIEW





The MAX System on Module supports Intels® Arria® 10 FPGA family and provides the architecture on a very compact embedded board. The Arria 10 SoC-FPGA in F34 footprint (1152 pins) provides 23 transceivers with data rate up to 17.4 GBit/s, connected via Samtec high speed connectors to the baseboard. The MAX SoM can be populated optionally with 480KLE, 570KLE and 660KLE Arria 10 SoC-FPGAs.

In terms of external memory two DDR3 SDRAM banks (32 bit wide) with up to 4GByte each bank are available. One memory bank is dedicated to the Hard Processor System (HPS), the 2nd memory bank is dedicated to the FPGA. A 1GBit QSPI configuration flash device can be used to configure the FPGA, for Operating System and application software 4GByte of eMMC NAND Flash are available.

MAX operates based on a single voltage power supply of 12V. All necessary on-board voltages are generated on MAX. For monitoring of essential system parameter a dedicated FPGA provides the values for current, voltage and temperature via I²C.

For most flexible clocking two programmable clock sources are implemented.

4 Samtec connectors connect MAX to the baseboard. Two SEAF connector, 200 pins each, provide the FPGA I/O signals, two QRF8 connectors provide he 24 transceiver channels to the application board. MAX offers 232 I/O pins as well as 52 HPS pins.

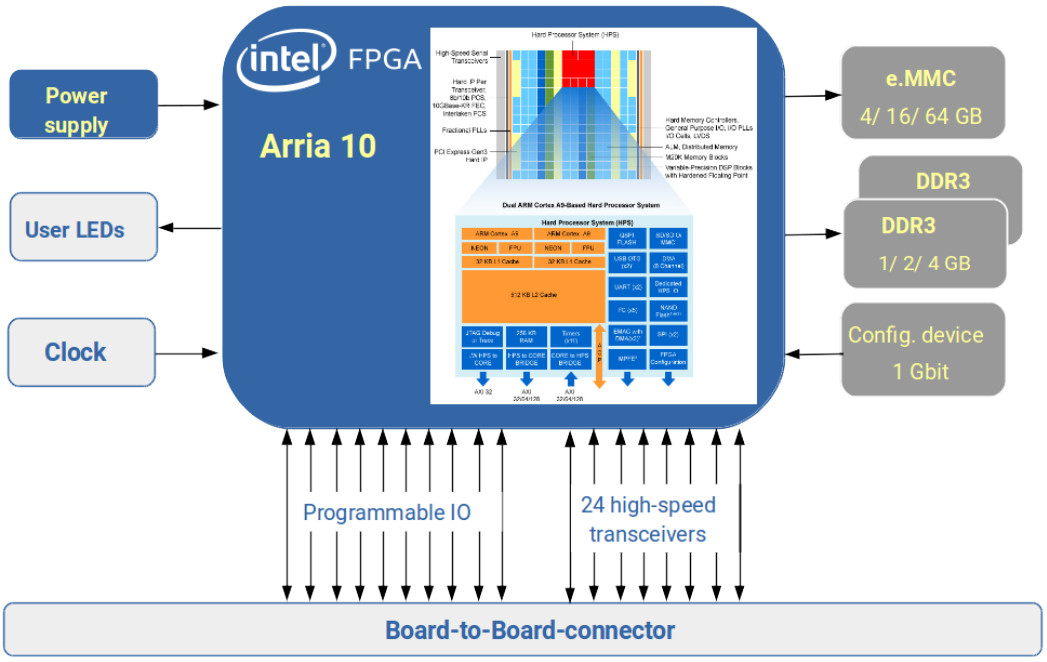
The SoM is shipped with a preprogrammed e-MMC NAND Flash containing:

- Preloader based on the example HPS System
- U-boot
- Linux kernel
- Linux root-file-system

The flash can easily be reprogrammed using the Linux environment on the board.

For each board a unique MAC address is provided. It is programmed to the board and available as a label on the SoM.

2.1 Block Diagram

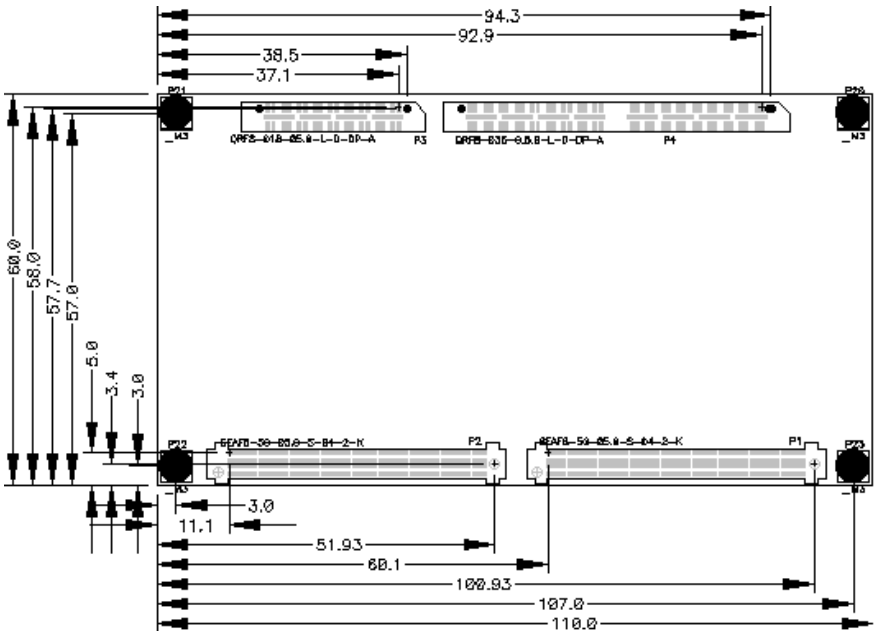


2.2 Feature Set

MAX provides the following features

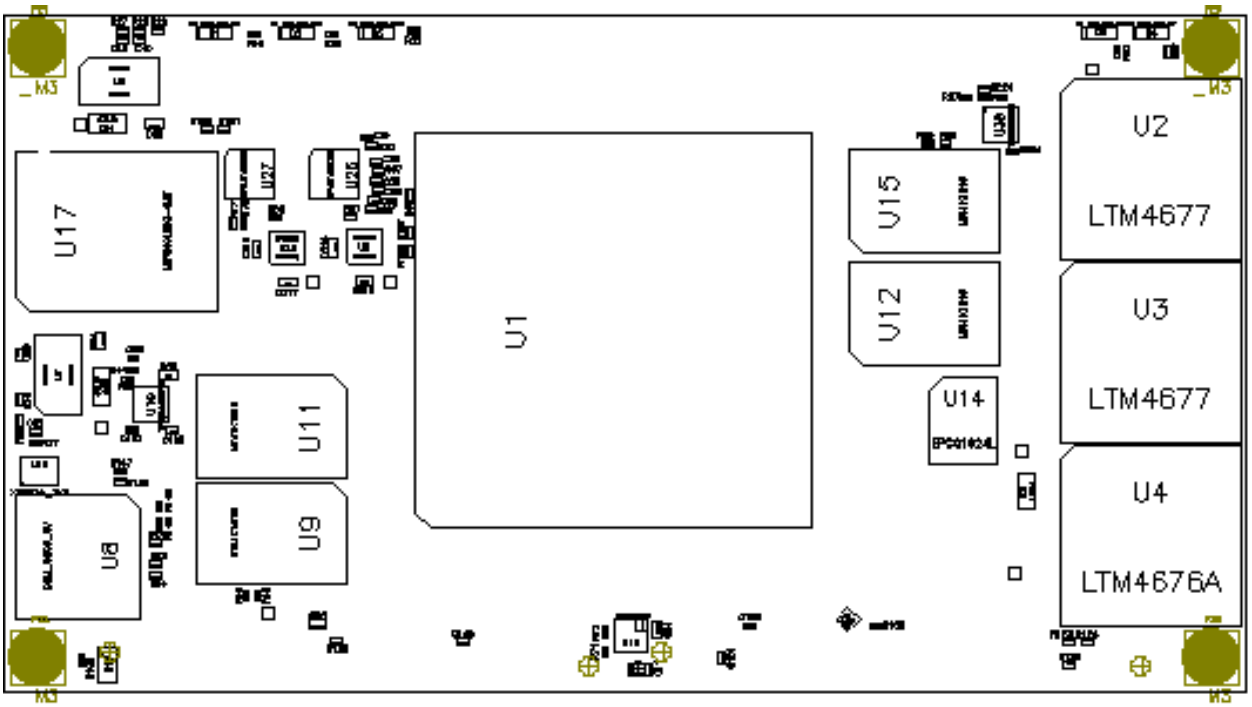
- Arria 10 SoC device
  - 10AS066E
  - 10AS057E
  - 10AS048E
  - F 34 package
- 1 Gbit Configuration Flash
- Dual 1,2 or 4 GByte x32 DDR3 Memory
- 4..64 GByte e.mmc Flash (32G default)
- Programmable Clock Generation
- 24 Transceiver 10Gbit/s
- 272 I/O Pins on pin header
- System Controller for Power Sequencing
- on-board power supply
- dimension: 110 x 60mm

2.3 Dimensions

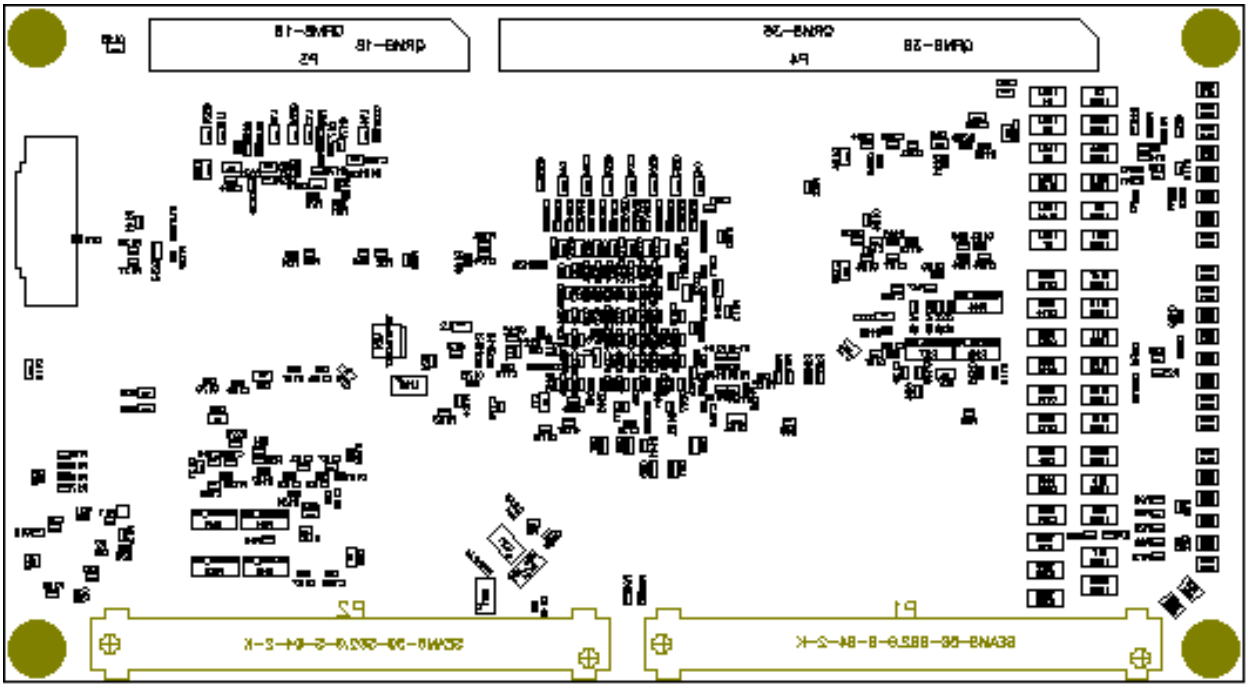


2.4 Parts Location

2.4.1 Components Top Side

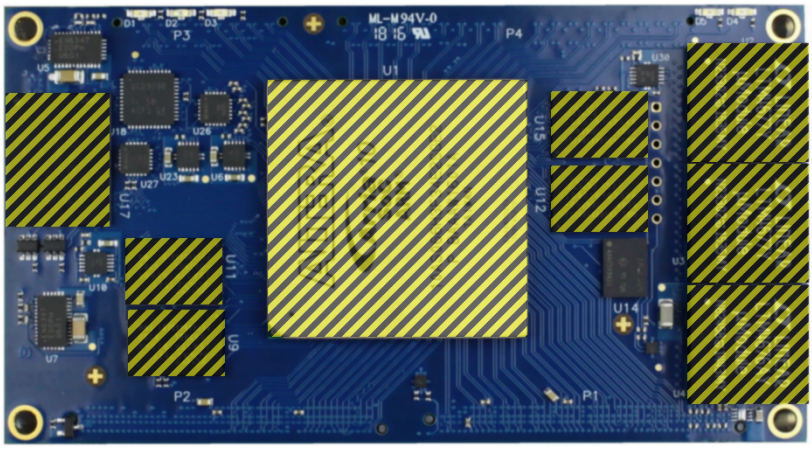


2.4.2 Components Bottom Side



2.5 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on MAX it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

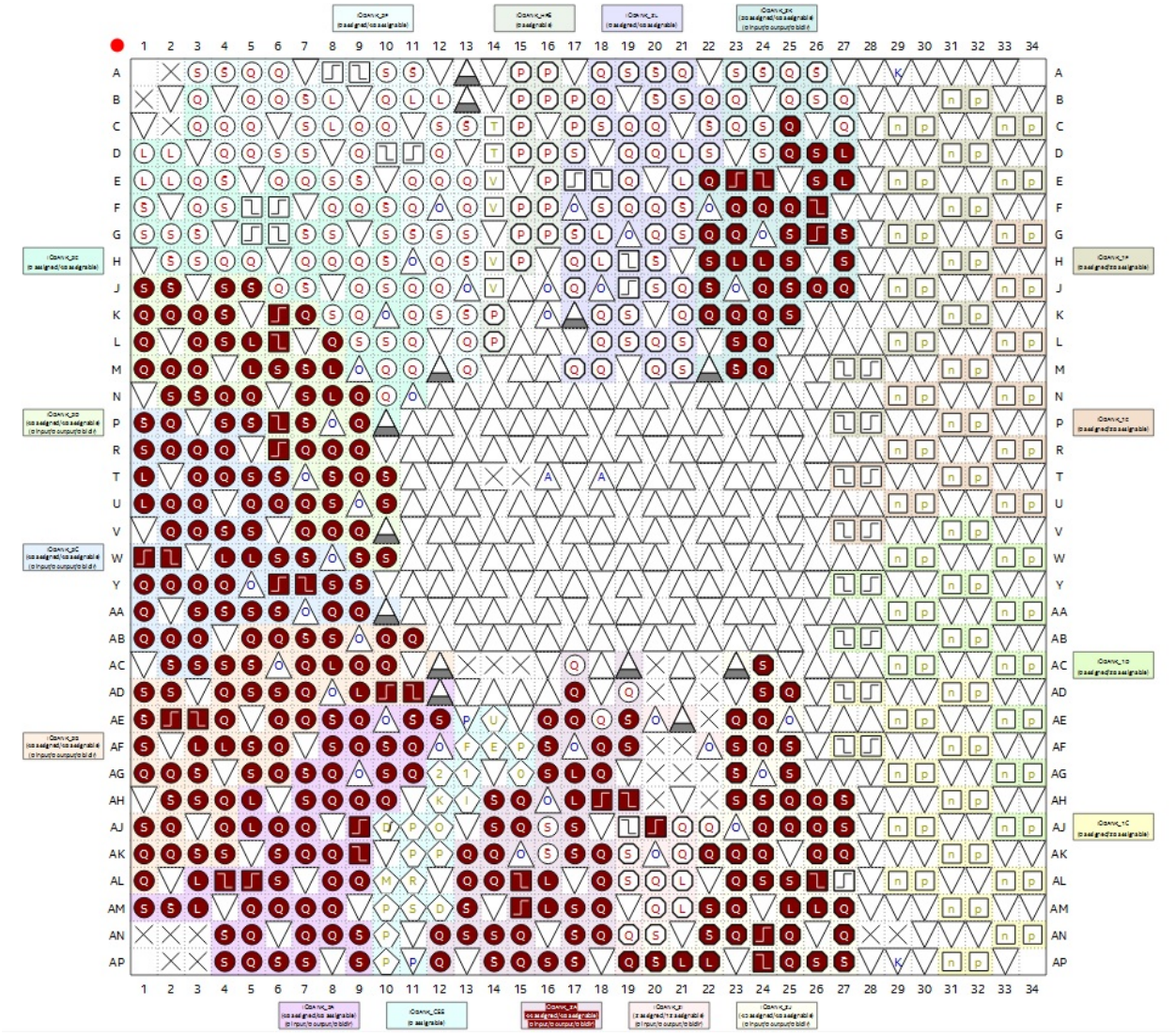
THREE

RESOURCES

3.1 I/O Voltages

3.1.1 FPGA I/O-Banks

The FPGA I/O banks are visualized in the following graphic:



3.1.2 IO-Bank usage / voltages

The following table shows the voltages of the IO-Banks, accordingly:

IO-Bank	Voltage	VREF	Max	Usage
2A	external	GND	1.8V	External I/O
2I	1.8V			MAX10
2J	1.5V	0.75		DDR3
2K	1.5V	0.75		DDR3
2L	external		3.0V	External IO
3A	external	external	1.8V	External IO
3B	external	external	1.8V	External IO
3C	external	external	1.8V	External IO
3D	external	external	1.8V	External IO
3E	1.5V	0.75V		DDR3
3F	1.5V	0.75V		DDR3
HPS	3.0V		3.0V	HPS / I O

3.2 FPGA Configuration

The JTAG signals of the SoC-FPGA are routed to the baseboard connector. As default boot option the board is configured to boot from the QSPI configuration device. The JTAG Signals are working with a 1.8V IO Standard. VCCPGM is connected to 1.8V

3.2.1 FPGA Configuration select with MSEL

The MSEL pins can be selected by implementing different buid-time-options using 1K Ohm resistors. The default setting is booting from QSPI Flash (AS Standard = '011').

MSEL	VCC18	GND
0	R134	R140
1	R133	R139
2	R138	R135

3.2.2 Clocking

The MAX SoM is equipped with two IDT programmable clock generators 5P49V5935. One device generates the core clocks while the second generates the Transceiver Reference clocks. The Timing Commander Software can be used to generate the respective frequencies and program them into the devices. To program the IDT devices, the Programmer Board for VersaClock 5 can be used. Make sure to provide the respective I²C signal on a pin header on the baseboard.

3.2.2.1 Main clock device U27

The main clock device U27 generates the frequencies for the HPS, the memory subsystems, the USR_CLK for configuration, a 1.8V and LVDS based ref clock into the FPGA. These frequencies are programmed into the devices OTP cells and are available at power up. The I²C signals are available on the service connector or the device can be programmed from the MAX10. The IDT device is clocked by an integrated crystal of 25MHz.

IO-pin	Clock	Voltage
24 / Out0	HPS Cock 25MHz	1.8V
20 / Out1	CLKAp	LVDS
19 / Out1B	CLKAn	LVDS
17 / Out2	CLKB	1.8V
16 / Out2B	USR_CLK	1.8V
14 / Out3	DDR1_REFCLKp (250MHz)	1.8V
13 / Out3B	DDR1_REFCLKn	1.8V
11 / Out4	DDR2_REFCLKp (250MHz)	1.8V
12 / Out4B	DDR2_REFCLKn	1.8V

3.2.2.2 Second clock device U26

The second clock generator is used to provide the respective frequencies to the transceiver clock reference inputs. This device is not programmed by default, but can be reprogrammed on demand from the MAX10 device or from the I²C signals routed to the service header. The input frequency of the IDT device can be switched between the on-chip 25MHz oscillator or an external differential clock input available on the pin header P3. The IDT_CLKSEL pin is connected to the pin- header. This signal has in integrated Pull-down to select the on-chip source. To switch to external Clock Input, set this signal to HIGH.

IO-pin	Clock	Voltage
20 / Out1	GXBL_1EBTP	LVPECL
19 / Out1B	GXBL_1EBTN	LVPECL
17 / Out2	GXBL_1FBTP	LVPECL
16 / Out2B	GXBL_1FBTN	LVPECL
14 / Out3	GXBL_1DBTP	LVPECL
13 / Out3B	GXBL_1DBTN	LVPECL
11 / Out4	GXBL_1CBTP	LVPECL
12 / Out4B	GXBL_1CBTN	LVPECL

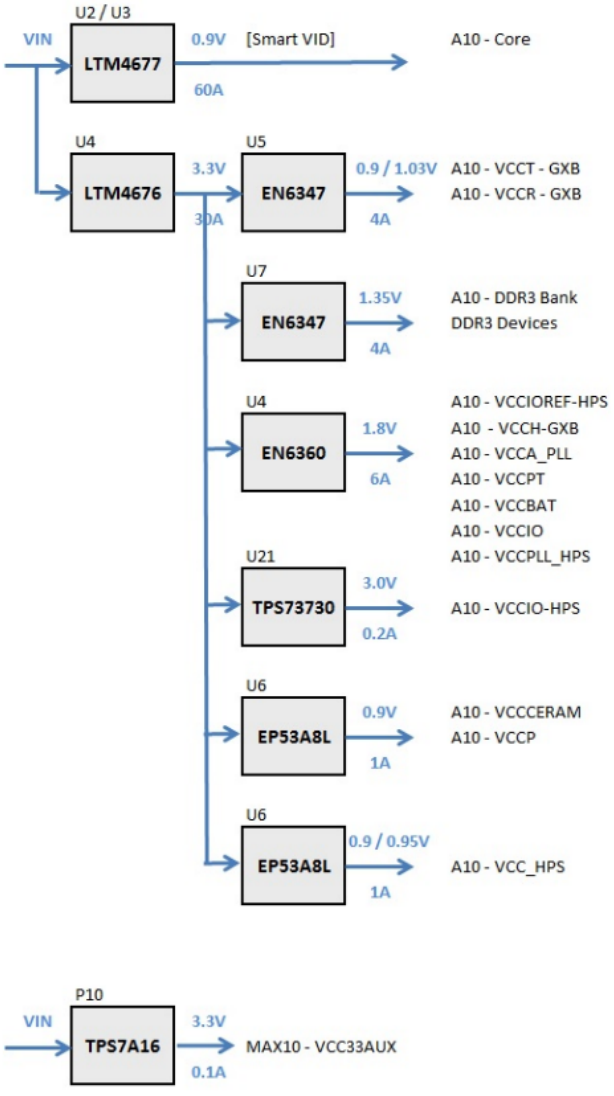
3.2.2.3 FPGA Clock Sources

Signal	FPGA Pin	Description
HPS_CLK	B16	25MHz HPS Ref Clock
CLKA	AH18 / AH19	100MHz FPGA system Clock
CLKB	AJ20	100MHz Clock
USRCLK	AK16	100MHz USR Clock
DDR1 Refclk	D10 / D11	250MHz DDR Refclk
DDR2 Refclk	E23 / E24	250MHz DDR Refclk
REFCLK_GLXBL_1CB	AF28 / AF27	REFCLK Transceiver / Connector P4
REFCLK_GLXBL_1CBT	AD28 / AD27	REFCLK Transceiver / IDT U26
REFCLK_GLXBL_1DB	AB28 / AB27	REFCLK Transceiver / Connector P4
REFCLK_GLXBL_1DBT	Y28 / Y27	REFCLK Transceiver / IDT U26
REFCLK_GLXBL_1EB	V28 / V27	REFCLK Transceiver / Connector P4
REFCLK_GLXBL_1EBT	T28 / T27	REFCLK Transceiver / IDT U26
REFCLK_GLXBL_1FB	P28 / P27	REFCLK Transceiver / Connector P4
REFCLK_GLXBL_1FBT	M28 / M27	REFCLK Transceiver / IDT U26

3.2.2.4 Power Supply

The single input voltage of the module is 12V. The 12V rail is used to generate the Core voltage, a 3.3V intermediate voltage and the 1.8V IO Voltage. Out of the 3.3V rail all other lower voltage rails are generated. A MAX10 device is used to power up and down the rails in the required order and generate a respective power-good signal, as well as an enable signal for power supply on the baseboard. The MAX10 monitors all voltages and provides an I²C interface to the Arria 10.

The following figure shows the structure of the power subsystem:



3.2.2.5 Arria 10 Voltage Rails

The following table shows the voltage rails with max. current load:

Voltage Rail	Description	Voltage	Current	Signal Name
VCC	Core Voltage Supply	Smart VID	60A	VCCCORE
VCCP	VCCP	Smart VID	0.8A	
VCCERAM	Memory Power Pins	0.9V/0.95V	0.3A	VCCP
VCCPT	Programmable power technology and I/O Predriver	1.8V	0.8A	VCC18
VCCA_PLL	PLL Analog Power	1.8V	0.25A	
VCC_PGM	Configuration Pins Power Supply	1.8V		
VCCR_GXB	Analog Power Transceiver (receiver)	0.95/1.03/ 1.12V	2.6A	VCCTR
VCCT_GXB	Analog Power Transceiver (transmitter)	0.95/1.03/ 1.12V	0.6A	
VCCH_GXB	Analog Power	1.8V	2A	VCC18
VCCL_HPS	HPS power Supply (1.2GHz: 0.9V/ 1.5GHz:0.95V) 0.9V/	0.9V/0.95V	0.8A	VCCHPS
VCCIO_HPS	HPS-IO supply	3.0V	0.1A	VCC30
VCCPLL_HPS	Analog power to HPS PLL	1.8V	0.025A	VCC18
VCCIOREF_HPS	HPS I/O predriver	1.8V		
VCCIO3F VCCIO2K/ 2J	DDR3 Memory banks	1.35V	0.5A	VCC135
VCCIO	FPGA IO Banks	external		

3.2.2.6 Power Sequencing

On startup the power rails are applied in the following order:

1. VCCCORE, VCCP
2. VCCTR, VCCPT, VCCHPS
3. VCC18
4. VCC135, VCC30

3.2.2.7 LTM467x I²C Interface

The Linear Technology Power Modules LTM4677 and LTM4676A provide an I²C interface for programming and monitoring. All three LTM467x devices are connected to the Max 10 device with the I²C interface. The following table shows the I²C bus address settings for the respective device.

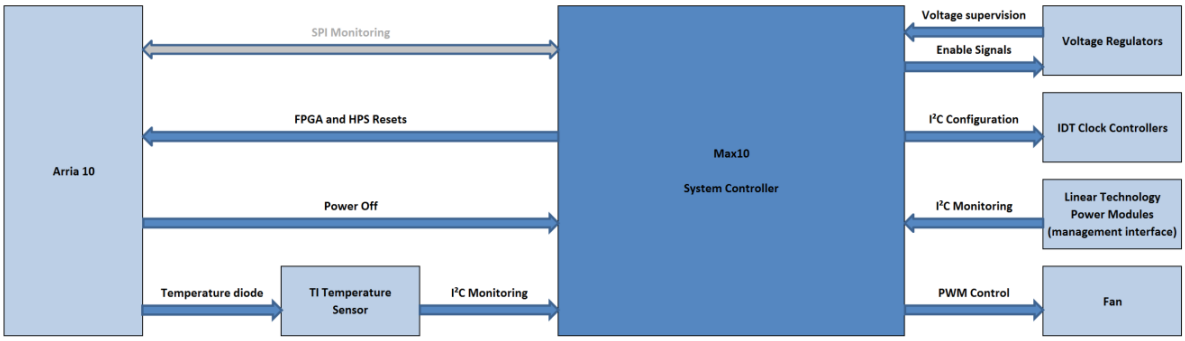
Device	I²C Bus Address	Function
U2	0x40	Core Voltage
U3	0x41	Core Voltage
U4	0x42	3.3V / 1.8V

The following table shows the I²C signals MAX10 connections.

Function	MAX10 Pin	Signal Name
I²C Data	E12	LTC_SDA
I²C Clock	F13	LTC_SCL
Alert Signal	F12	LTC_WP

3.2.2.8 Max10 System Controller

The System Controller is implemented by using a MAX10 FPGA. It takes care of the Voltage Rail supervision and power on/off sequence, as well as the fan control and reset signals. Via I²C interfaces it can access the Arria10 temperature diode and the parameter from the Linear Technology Modules. Also the IDT Clock distribution devices are programmed via I²C upon every start. The user can power down the MAX SoM manually from the Arria10 side, via a dedicated signal. A SPI interface is implemented between MAX10 and Arria10 and should be used in a future release of the firmware to give access to voltage and temperature data.



3.2.2.9 System Controller (U8) FPGA connection

Function	Arria 10 Pin	MAX10 Pin
SPI-CLK	AJ16	J9
SPI-nSS	AC17	J10
SPI-MOSI	AE18	G12
SPI-MISO	AJ19	K10
nPOWER_DOWN	AD19	H8
POWER_GOOD	AC24	L12
HPS_nPOR	K14	E5

3.2.2.10 Power Enable for Baseboard

The SEQ_OK signal can be used to power up the baseboard power rails. This signal is active high. External Power Supplies should be started when the SEQ_OK signal goes high and should be disabled as soon as the SEQ_OK signal is low.

3.2.2.11 Module power ON

The EXT_OFF signal is used to switch off the power supply of the module. The EXT_OFF signal has a 10K pull_up to VCC33_AUX. To switch off the module connect the EXT_OFF signal to GND. To power up the module release this signal.

3.2.2.12 Reset Signals

The Power_Good signal is connected to the HPS_NPOR and the FPGA_Resetn inputs. The HPS_RSTn signal is available at connector P1.

Function	Pin	Signal Name
Power Good	K14	HPS_NPOR
Power Good	AC24	FPGA_RSTn
Warm Reset	L14	HPS_RSTn

Power good signal is an open_drain signal with a pullup to 1.8V. All power supplies of the board are connected to this signal and a baseboard power good signal should be connected with an open_drain output, too.

The Warm Reset signal is an input and output of the HPS System. It is available on the baseboard connector with a 1K pull-up resistor to 3.0V on the module.

3.2.2.13 Temperature Measurement

The Arria 10 device is equipped with a Temperature diode. A TMP401 (U24) device is used to measure the temperature of the Arria 10 die and provides an internal temperature sensor. The device provides an I²C interface and two programmable outputs. The I²C bus and the programmable Alert signals are connected to the Max 10 system controller. The TMP401 has the I²C address 0x4C.

Function	MAX10 Pin	Signal Name
I²C Data	B10	TI_SDA
I²C Clock	B9	TI_SCL
Temp Alert 1	A9	LTERM1
Temp Alert 2	A8	LTERM2

3.2.2.14 VBAT

The VBAT signal is routed to connector P1 and must be connected to a supply voltage to start the FPGA. This pin can be connected to a 1.5V or 1.8V power rail. Please Refer to the Altera Arria 10 Device Datasheet

If VBAT is not connected to any voltage, the FPGA will not be accessible!!!

3.3 HPS Subsystem

3.3.1 BSEL Settings

Three dedicated HPS IO pins are used to select the boot source of the processor system. The default value is '101' (0x5) to boot from eMMC. The BSEL Pins are available on connector P2 can be used to overwrite the default settings. Please make sure that these Pins are NOT driven from external components during the Reset phase. The follwing table shows the default settings of the BSEL signals.

BSEL	Signal	Default Resistor
0	HPS_GPIO2_7	Pull-up
1	HPS_GPIO_2_6	Pull-down
2	HPS_SDIO_CLK	Pull-up

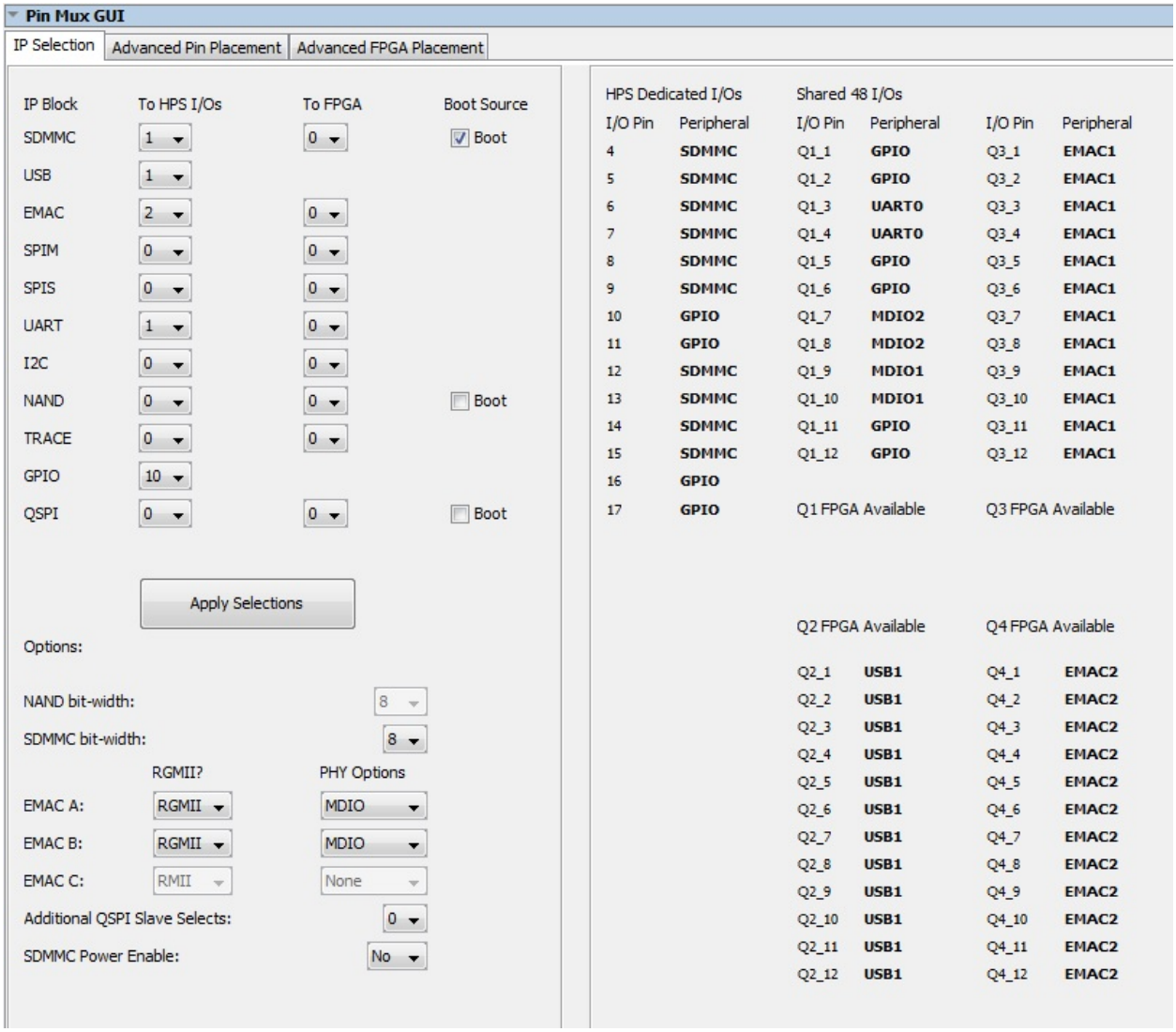
Table 6-4: BOOTSEL Field Values and Flash Device Selection

BOOTSEL Field Value	Flash Device
0x0	Reserved
0x1	FPGA (HPS-to-FPGA bridge)
0x2	1.8 V NAND flash memory
0x3	3.0 V NAND flash memory
0x4	1.8 V SD/MMC flash memory with external transceiver
0x5	3.0 V SD/MMC flash memory with internal transceiver
0x6	1.8 V quad SPI flash memory
0x7	3.0 V quad SPI flash memory

3.3.2 Peripheral Pin Multiplexing

The Peripheral Pin Multiplexing of the HPS Peripheral has to include the respective setting for the eMMC flash device on the module. All other signals are connected to the pin header and can be set accordingly to the requirements on the baseboard.

The following figure shows an example of the HPS Peripheral Pin multiplexing for the MAX SoM.



3.3.3 DDR3 Memory

The MAX Module is equipped with two DDR3 32bit memory banks. Each bank can be equipped with two 4Gbit, 8Gbit or 16Gbit devices which results in 1Gbyte, 2Gbyte or 4Gbyte Memory per bank. Please keep in mind that the larger devices have reduced frequency ranges. Respective presets for the memory settings are available in the MAX installer.

3.4 Memory Bank 1

Memory Bank1 is located in IOBANK 3E / 3F. The pin locations are optimized for the Hard Memory Controller. In Qsys select the “Arria 10 External Memory Interfaces”.

Function	Pin	Signal Name
DDR1 Reference Clock input from IDT U27	D11/D10	DDR1_REFCLK
DDR1 Clock Output	D6 / D7	DDR1_CK0
DDR1 Clock Enable		DDR1_CKE[1..0]
DDR1 Chip Select		DDR1_CSn[1..0]
DDR1 On Die Termination		DDR1_ODT[1..0]
DDR1 Reset		DDR1_RSTn
DDR1 Write Enable	D5	DDR1_WEn
DDR1 RAS	E11	DDR1_RASn
DDR1 CAS	C12	DDR1_CASn
DDR1 Address		DDR1_A[15..0]
DDR1 Bank Address		DDR1_BA[2..0]
DDR1 Data		DDR1_DQ[31...0]
DDR1_Data Strobe		DDR1_DQS[3..0]
DDR1_Data Mask		DDR1_DM[3..0]

3.5 Memory Bank 2

Memory Bank2 is located in IOBANK 2K / 2J. The pin locations are optimized for the Hard Memory Controller. This memory Controller is related to the HPS and can be linked directly to the Arria 10 HPS. In Qsys select the “Arria 10 External Memory Interfaces for HPS”.

Function	Pin	Signal Name
DDR2 Reference Clock input from IDT U27	E23/E24	DDR2_REFCLK
DDR2 Clock Output	L23/M23	DDR2_CK0
DDR2 Clock Enable		DDR2_CKE[1..0]
DDR2 Chip Select		DDR2_CSn[1..0]
DDR2 On Die Termination		DDR2_ODT[1..0]
DDR2 Reset		DDR2_RSTn
DDR2 Write Enable	M24	DDR2_WEn
DDR2 RAS	F23	DDR2_RASn
DDR2 CAS	E26	DDR2_CASn
DDR2 Address		DDR2_A[15..0]
DDR2 Bank Address		DDR2_BA[2..0]
DDR2 Data		DDR2_DQ[31...0]
DDR2_Data Strobe		DDR2_DQS[3..0]
DDR2_Data Mask		DDR2_DM[3..0]

3.6 eMMC Flash

The eMMC flash device provides a standard MMC interface, that is supported by the SoC system. The Micron eMMC Flash device is available from 4 Gbyte up to 64Gbyte.The MMC interface provides an eight bit parallel interface, which is connected to the HPS System.

eMMC (U17) FPGA connection

Function	FPGA Pin
HPS-SDIO-CLK	D15
HPS-SDIO-CMD	C17
HPS-SDIO-D0	B15
HPS-SDIO-D1	B17
HPS-SDIO-D2	D16
HPS-SDIO-D3	A16
HPS-SDIO-D4	G16
HPS-SDIO-D5	A15
HPS-SDIO-D6	C15
HPS-SDIO-D7	F16
nRST	

3.7 QSPI Flash

An Altera EPCQ1024L flash device is used to configure the FPGA. The QSPI-Flash is connected to the ASx4 configuration interface. To configure the FPGA via active serial configuration scheme, the MSEL pins must be set accordingly. The QSPI Flash is only visible to the FPGA, if the MSEL Signals are set to AS configuration mode. A 100MHz User clock signal is available on FPGA pin AK16. This can be used for the configuration of the FPGA.

QSPI (U14) FPGA Connection

Function	FPGA Pin (ASx4)
CS0n	AN10
DCLK	AJ10
DATA0	AJ11
DATA1	AK12
DATA2	AK11
DATA3	AF15

3.8 User LEDs

The MAX SoM provides two user LEDs which are located on the top / right side of the module.

Function	FPGA
User_LED1(D4)	AL21
User_LED2(D5)	AK19

3.9 External Connections

Function	Description
IOB2A[40..0]	IOBANK 2A
VCCIO2A	Power Supply for IOBANK 2A
VREFB2A	Reference Voltage for IOBANK 2A
IOB3A[47..0]	IOBANK 3A
VCCIO3A	Power Supply for IOBANK 3A
VREFB3A	Reference Voltage for IOBANK 3A
IOB3B[47..0]	IOBANK 3B

Continued on next page

Table 3.1 – continued from previous page

VCCIO3B	Power Supply for IOBANK 3B
VREFB3B	Reference Voltage for IOBANK 3B
IOB3C[47..0]	IOBANK 3C
VCCIO3C	Power Supply for IOBANK 3C
VREFB3C	Reference Voltage for IOBANK 3C
IOB3D[47..0]	IOBANK 3D
VCCIO3D	Power Supply for IOBANK 3D
VREFB3D	Reference Voltage for IOBANK 3D
FAN	FAN connection. This signal is an open_drain output to drive the FAN.
JTAG	JTAG Connection of the FPGA
VCCBAT	Supply for Key storage
+12V	12V power supply. The power supply of the module should source up to 8A @ 12V
IDT_CLKIN	Second clock input to IDT Versaclock clock driver
IDT_SCL1 / SDA1	IDT1 I²C programming interface
IDT_SCL2 / SDA2	IDT2 I²C programming interface
TI_SCL / TI_SDA	TI I²C programming interface
HPSIO0_[23..0]	HPSIO Bank0
HPSIO1_[23..0]	HPSIO Bank 1
HPSIO2_[6,7,12,13]	HPSIO Bank 2 [3.0V]
VCC18out 2A	Output from Module
VCC33out 1A	Output from Module
Power_Good	Open_Drain power good signal – should be used from external Power supply as open Drain. Pull-up to 1.8V on module
EXT_OFF	Active Low signal to shut down the modules power supply. To start the module release this signal.
SEQ_OK	Active high signal. Shows that all power supplies on the module are switched on. This signal can be used to power up power supplies on the baseboard.
HPS_RSTn	Active Low reset signal of the HPS. This signal is a bidirectional signal. The baseboard can drive this signal low to reset the CPU. The CPU can drive this signal too, on Warm Reset or debug reset
GND	All GND signals are connected on the module. To provide a low impedance gnd connection, all GND signals should be connected on the baseboard, too. The four mounting pads are connected to GND, too.

3.9.1 Mating Connectors

The stacking height between Baseboard and Module PCB is 7mm.

On a baseboard for the MAX SoM, such as i.e. MAXEVK, the following type of mating connectors shall be used on the baseboard:

Part Number	Connector Location	Signal Type
SEAF8-50-05.0-S-04-2-K	P1	I/O
SEAF8-50-05.0-S-04-2-K	P2	I/O
QRF8-018- 05.0-L-D-DP-A	P3	High Speed
QRF8-036-05.0-L-D-DP-A	P4	High Speed

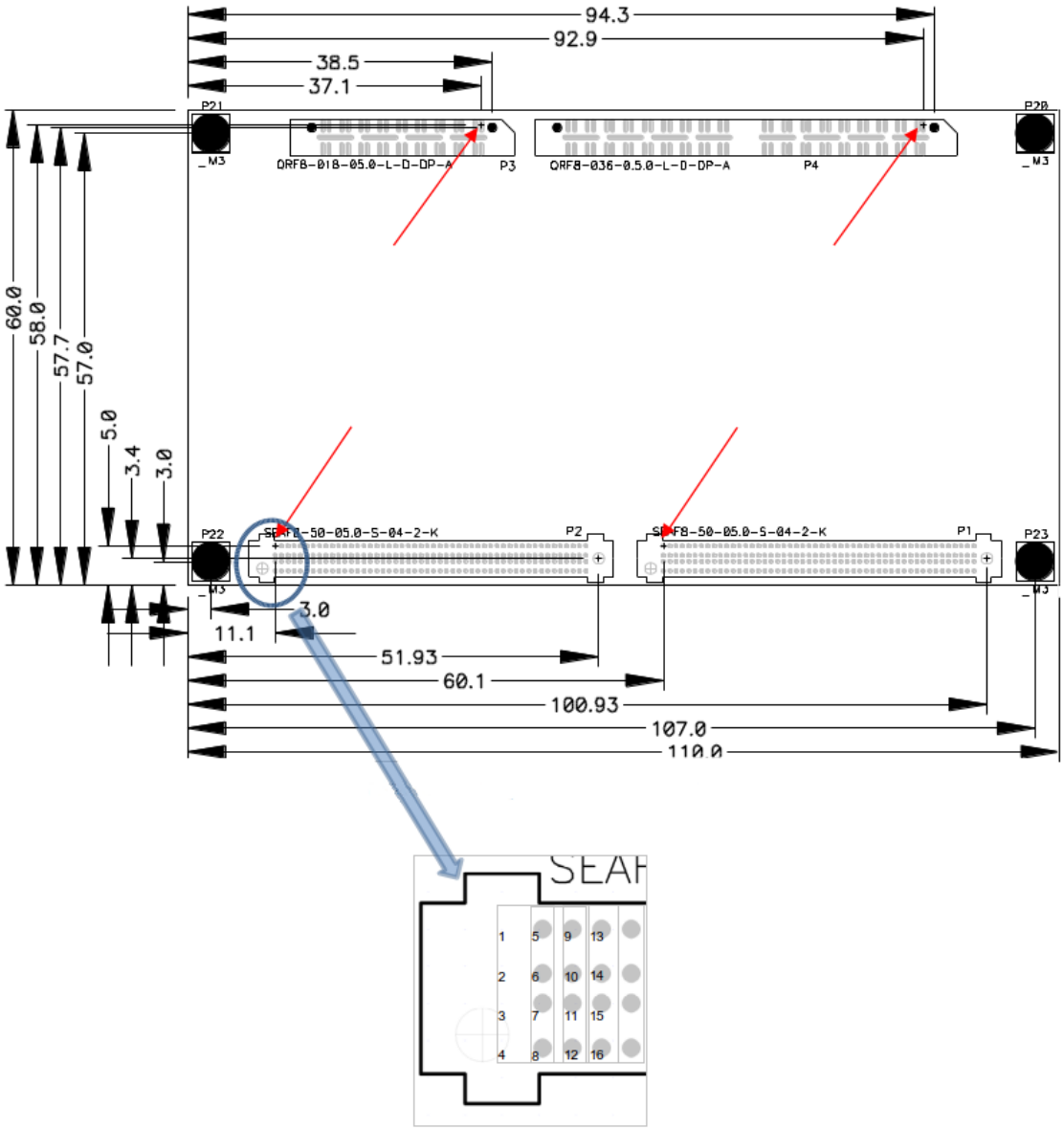


Figure 10

3.9.2 Connector P1

#	FPGA	Function	#	FPGA	Function	#	FPGA	Function	#	FPGA	Function
1		TI_SCL	2		GND	3		SEQ_OK	4		GND
5		TI_SDA	6	AC5	IOB3B2	7		POWER _Good	8	AD1	IOB3B6
9		GND	10	AC4	IOB3B3	11		GND	12	AD2	IOB3B7

Continued on next page

Table 3.2 – continued from previous page

#	FPGA	Function	#	FPGA	Function	#	FPGA	Function	#	FPGA	Function
13	AB7	IOB3B0	14	AD4	IOB3B10	15	AE3	IOB3B4 clk3b0n	16	AB5	IOB3B14
17	AB8	IOB3B1	18	AE4	IOB3B11	19	AE2	IOB3B5 clk3b0p	20	AB6	IOB3B15
21	AB11	IOB3B8	22		VCCIO3B	23	AF4	IOB3B12 clk3bout0p	24		GND
25	AB10	IOB3B9	26	AC7	IOB3B18	27	AF3	IOB3B13 clk3bout0n	28	AE1	IOB3B22
29		VCCIO3B	30	AD7	IOB3B19	31		GND	32	AF1	IOB3B23
33	AE7	IOB3B16	34	AD6	IOB3B26	35	AG3	IOB3B20	36	AG2	IOB3B30
37	AE6	IOB3B17	38	AD5	IOB3B27	39	AH3	IOB3B21	40	AG1	IOB3B31
41	AC10	IOB3B24	42		VREFB3B	43	AH4	IOB3B28	44		GND
45	AC9	IOB3B25	46	AF6	IOB3B34	47	AJ4	IOB3B29	48	AH2	IOB3B38
49		VCCIO3B	50	AG6	IOB3B35	51		GND	52	AJ1	IOB3B39
53	AD9	IOB3B32 clk3bout1n	54	AF5	IOB3B42	55	AJ2	IOB3B36	56	AK1	IOB3B46
57	AC8	IOB3B33 clk3bout1p	58	AG5	IOB3B43	59	AK2	IOB3B37	60	AL1	IOB3B47
61	AD11	IOB3B40 clk3b1n	62		GND	63	AK3	IOB3B44	64		GND
65	AD10	IOB3B41 clk3b1p	66	AG7	IOB3A2	67	AK4	IOB3B45	68	AM2	IOB3A6
69		GND	70	AH7	IOB3A3	71		GND	72	AM1	IOB3A7
73	AJ6	IOB3A0	74	AH5	IOB3A10 clk3aout1n	75	AL4	IOB3A4 clk3a0n	76	AL3	IOB3A14 clk3aout0n
77	AJ7	IOB3A1	78	AJ5	IOB3A11 clk3aout1p	79	AL5	IOB3A5 clk3a0p	80	AM3	IOB3A15 clk3aout0p
81	AE8	IOB3A8	82		VCCIO3A	83	AM5	IOB3A12	84		GND
85	AF8	IOB3A9	86	AK8	IOB3A18	87	AM6	IOB3A13	88	AN4	IOB3A22
89		VCCIO3A	90	AK7	IOB3A19	91		GND	92	AP4	IOB3A23
93	AG8	IOB3A16	94	AK9	IOB3A26 clk3a1n	95	AK6	IOB3A20	96	AN5	IOB3A30
97	AH8	IOB3A17	98	AJ9	IOB3A27 clk3a1p	99	AL6	IOB3A21	100	AP5	IOB3A31
101	AE9	IOB3A24	102		VREFB3A	103	AM7	IOB3A28	104		GND
105	AF9	IOB3A25	106	AH9	IOB3A34	107	AN7	IOB3A29	108	AP6	IOB3A38
109		VCCIO3A	110	AH10	IOB3A35	111		GND	112	AP7	IOB3A39
113	AF10	IOB3A32	114	AL8	IOB3A42	115	AG11	IOB3A36	116	AM8	IOB3A46
117	AG10	IOB3A33	118	AL9	IOB3A43	119	AF11	IOB3A37	120	AN8	IOB3A47
121	AE11	IOB3A40	122		GND	123	AN9	IOB3A44	124		GND
125	AE12	IOB3A41	126	AK13	IOB2A2	127	AP9	IOB3A45	128	AP12	IOB2A6
129		GND	130	AL13	IOB2A3	131		GND	132	AN12	IOB2A7
133	AH14	IOB2A0	134	AK14	IOB2A10	135	AL15	IOB2A4	136	AM13	IOB2A14
137	AJ14	IOB2A1	138	AL14	IOB2A11	139	AM15	IOB2A5	140	AN13	IOB2A15
141	AH15	IOB2A8	142		VCCIO2A	143	AM16	IOB2A12	144		GND
145	AJ15	IOB2A9	146	AF16	IOB2A18 PR_DONE	147	AL16	IOB2A13	148	AP14	IOB2A22
149		VCCIO2A	150	AG16	IOB2A19 nPERSTL1	151		GND	152	AN14	IOB2A23

Continued on next page

Table 3.2 – continued from previous page

#	FPGA	Function	#	FPGA	Function	#	FPGA	Function	#	FPGA	Function
153	AK17	IOB2A16	154	AN17	IOB2A26	155	AG18	IOB2A20	156	AP15	IOB2A30
157	AJ17	IOB2A17	158	AM17	IOB2A27	159	AF18	IOB2A21	160	AN15	IOB2A31
161	AP17	IOB2A24	162		VCCIO2A	163	AN18	IOB2A28	164		GND
165	AP16	IOB2A25	166	AL18	IOB2A34	167	AM18	IOB2A29	168	AH17	IOB2A32
169		VCCIO2A	170	AK18	IOB2A35	171		GND	172	AG17	IOB2A33
173		VCCBAT	174	AE17	IOB2A38 PR_READY	175		EXT_OFFn	176	AE19	IOB2A36
177		JTAG_TRST	178	AE16	IOB2A39 nPERSTL0	179		JTAG_TDO	180	AF19	IOB2A37
181		JTAG_TMS	182		JTAG_TCK	183		JTAG_TDI	184		GND
185		GND	186		GND	187		GND	188		GND
189		+12V	190		+12V	191		+12V	192		+12V
193		+12V	194		+12V	195		+12V	196		+12V
197		+12V	198		+12V	199		+12V	200		+12V

3.9.3 Connector P2

#	FPGA	Function	#	FPGA	Function	#	FPGA	Function	#	FPGA	Function
1		MSEL2	2		IDT_SCL1	3		FAN	4		IDT _CLK-SEL
5		MSEL1	6		IDT_SDA1	7		FAN	8		BSEL2_HPS _SDIO_CLK
9		GND	10		IDT_SCL2	11		GND	12	F20	HPSIO1_3
13		MSEL0	14		IDT_SDA2	15	C19	HPSIO1_22	16	E19	HPSIO1_7
17		HPS_RSTn	18		GND	19	E18	HPSIO1 _1Clk2l1n	20		GND
21	H18	HPSIO0 _19clk2l out0n	22	C18	HPSIO1_12	23	F19	HPSIO1_6	24	D22	HPSIO1_8
25	K21	HPSIO0_6	26	D17	HPSIO1_13	27	E17	HPSIO1 _0clk2l1p	28	E21	HPSIO1 _4clk2l out1p
29		VCCIO2L	30	F21	HPSIO0_17	31		GND	32	D21	HPSIO1 _5clk2 lout1n
33	H20	HPSIO0_13	34	G21	HPSIO0_16	35	G20	HPSIO1_2	36	D19	HPSIO1_23
37	J20	HPSIO0_12	38		VCC18 out	39	C22	HPSIO1_9	40		GND
41	K19	HPSIO0_8	42	J21	HPSIO0_7	43	B22	HPSIO1_18	44	D20	HPSIO1_11
45	L19	HPSIO0_9	46	F18	HPSIO0_20	47	A21	HPSIO1_19	48	C20	HPSIO1_10
49		VCCIO2L	50	G18	HPSIO0 _18Clk2 lout0p	51		GND	52	B21	HPSIO1_20
53	L21	HPSIO0_5	54	G17	HPSIO0_21	55	B20	HPSIO1_21	56	A20	HPSIO1_17
57	M21	HPSIO0_4	58		VCC18 out	59	A19	HPSIO1_16	60		VCC33 out
61	L20	HPSIO0_10	62	H17	HPSIO0_15	63	B18	HPSIO1_15	64	E16	BSEL0 HP-SIO2_7
65	M20	HPSIO0_11	66	J17	HPSIO0_14	67	A18	HPSIO1_14	68	H15	HPSIO2_13
69		GND	70	H19	HPSIO0 _23clk2l0n	71		GND	72	F15	HPSIO2_12

Continued on next page

Table 3.3 – continued from previous page

#	FPGA	Function	#	FPGA	Function	#	FPGA	Function	#	FPGA	Function
73	K18	HPSIO0_2	74	J19	HPSIO0 _22Clk2l0p	75	L18	HPSIO0_3	76	G15	BSEL1 HP-SIO2_6
77	M17	HPSIO0_0	78		GND	79	M18	HPSIO0_1	80		VCC33 out
81	T10	IOB3D0	82	P9	IOB3D2	83	R7	IOB3D4	84	L8	IOB3D6
85	U10	IOB3D1	86	N9	IOB3D3	87	R8	IOB3D5	88	K7	IOB3D7
89		VCCIO3D	90	R9	IOB3D10	91		GND	92	L6	IOB3D14 clk3d0n
93	M8	IOB3D8 clk3dout1n	94	T9	IOB3D11	95	J5	IOB3D12	96	K6	IOB3D15 clk3d0p
97	N8	IOB3D9 clk3dout1p	98		VCCIO3D	99	J4	IOB3D13	100		GND
101	P7	IOB3D16	102	L5	IOB3D18 clk3dout0n	103	K4	IOB3D20	104	J2	IOB3D22
105	N7	IOB3D17	106	M5	IOB3D19 clk3dout0p	107	L4	IOB3D21	108	J1	IOB3D23
109		VCCIO3D	110	M7	IOB3D26	111		GND	112	K2	IOB3D30
113	T8	IOB3D24	114	M6	IOB3D27	115	K3	IOB3D28	116	K1	IOB3D31
117	U8	IOB3D25	118		VREFB3D	119	L3	IOB3D29	120		GND
121	V8	IOB3D32	122	P6	IOB3D34 clk3d1n	123	M3	IOB3D36	124	L1	IOB3D38
125	V9	IOB3D33	126	R6	IOB3D35 clk3d1p	127	M2	IOB3D37	128	M1	IOB3D39
129		VCCIO3D	130	W9	IOB3D42	131		GND	132	N3	IOB3D46
133	U7	IOB3D40	134	W10	IOB3D43	135	N5	IOB3D44	136	N2	IOB3D47
137	V7	IOB3D41	138		GND	139	N4	IOB3D45	140		GND
141		GND	142	P5	IOB3C2	143		GND	144	R2	IOB3C6
145	R4	IOB3C0	146	P4	IOB3C3	147	R3	IOB3C4	148	P2	IOB3C7
149	T4	IOB3C1	150		VCCIO3C	151	T3	IOB3C5	152		GND
153	Y9	IOB3C8	154	T6	IOB3C10	155	V4	IOB3C12	156	P1	IOB3C14
157	Y8	IOB3C9	158	T5	IOB3C11	159	V5	IOB3C13	160	R1	IOB3C15
161		VCCIO3C	162	U5	IOB3C18	163		GND	164	T1	IOB3C22 clk3cout1n
165	AA9	IOB3C16	166	U6	IOB3C19	167	V3	IOB3C20	168	U1	IOB3C23 clk3cout1p
169	AA8	IOB3C17	170		VREFB3C	171	U3	IOB3C21	172		GND
173	W7	IOB3C24	174	W5	IOB3C26 clk3cout0n	175	Y7	IOB3C28 Clk3c0n	176	U2	IOB3C30
177	W6	IOB3C25	178	W4	IOB3C27 clk3cout0p	179	Y6	IOB3C29 clk3c0p	180	V2	IOB3C31
181		VCCIO3C	182	Y4	IOB3C34	183		GND	184	W2	IOB3C38 clk3c1n
185	AA6	IOB3C32	186	Y3	IOB3C35	187	Y2	IOB3C36	188	W1	IOB3C39 clk3c1p
189	AA5	IOB3C33	190	Y4	VCCIO3C	191	Y1	IOB3C37	192	W2	GND
193	AB3	IOB3C40	194	AA4	IOB3C42	195	AA1	IOB3C44	196	AC2	IOB3C46
197	AB2	IOB3C41	198	AA3	IOB3C43	199	AB1	IOB3C45	200	AC3	IOB3C47

3.9.4 Connector P3

Connector P3 provides 8 transceiver pairs and the external clock input to the IDT VersaClock 5 device.

Function	FPGA	#	#	FPGA	Function
IDT_CLKINp		35	36		
IDT_CLKINn		33	34		
GXBL_1F_TX5p	B32	31	32	C30	GXBL_1F_RX5p
GXBL_1F_TX5n	B31	29	30	C29	GXBL_1F_RX5n
GXBL_1F_TX4p	D32	27	28	E30	GXBL_1F_RX4p
GXBL_1F_TX4n	D31	25	26	E29	GXBL_1F_RX4n
GXBL_1F_TX3p	F32	23	24	G30	GXBL_1F_RX3p
GXBL_1F_TX3n	F31	21	22	G29	GXBL_1F_RX3n
GXBL_1F_TX2p	H32	19	20	J30	GXBL_1F_RX2p
GXBL_1F_TX2n	H31	17	18	J29	GXBL_1F_RX2n
GXBL_1F_TX1p	C34	15	16	K32	GXBL_1F_RX1p
GXBL_1F_TX1n	C33	13	14	K31	GXBL_1F_RX1n
GXBL_1F_TX0p	E34	11	12	L30	GXBL_1F_RX0p
GXBL_1F_TX0n	E33	9	10	L29	GXBL_1F_RX0n
GXBL_1E_TX5p	G34	7	8	M32	GXBL_1E_RX5p
GXBL_1E_TX5n	G33	5	6	M31	GXBL_1E_RX5n
GXBL_1E_TX4p	J34	3	4	N30	GXBL_1E_RX4p
GXBL_1E_TX4n	J33	1	2	N29	GXBL_1E_RX4n

3.9.5 Connector P4

Connector P4 provides 16 transceiver pairs and 4 Reference clock inputs.

Function	FPGA	#	#	FPGA	Function
GXBL_1E_TX3p	L34	71	72	P32	GXBL_1E_RX3p
GXBL_1E_TX3n	L33	69	70	P31	GXBL_1E_RX3n
GXBL_1E_TX2p	N34	67	68	R30	GXBL_1E_RX2p
GXBL_1E_TX2n	N33	65	66	R29	GXBL_1E_RX2n
GXBL_1E_TX1p	R34	63	64	T32	GXBL_1E_RX1p
GXBL_1E_TX1n	R33	61	62	T31	GXBL_1E_RX1n
GXBL_1E_TX0p	U34	59	60	U30	GXBL_1E_RX0p
GXBL_1E_TX0n	U33	57	58	U29	GXBL_1E_RX0n
GXBL_1EBp	V28	55	56	P28	GXBL_1FBp
GXBL_1EBn	V27	53	54	P27	GXBL_1FBn
GXBL_1D_TX5p	W34	51	52	V32	GXBL_1D_RX5p
GXBL_1D_TX5n	W33	49	50	V31	GXBL_1D_RX5n
GXBL_1D_TX4p	AA34	47	48	W30	GXBL_1D_RX4p
GXBL_1D_TX4n	AA33	45	46	W29	GXBL_1D_RX4n
GXBL_1D_TX3p	AC34	43	44	Y32	GXBL_1D_RX3p
GXBL_1D_TX3n	AC33	41	42	Y31	GXBL_1D_RX3n
GXBL_1D_TX2p	AE34	39	40	AA30	GXBL_1D_RX2p
GXBL_1D_TX2n	AE33	37	38	AA29	GXBL_1D_RX2n
GXBL_1D_TX1p	AG34	35	36	AB32	GXBL_1D_RX1p
GXBL_1D_TX1n	AG33	33	34	AB31	GXBL_1D_RX1n
GXBL_1D_TX0p	AJ34	31	32	AC30	GXBL_1D_RX0p
GXBL_1D_TX0n	AJ33	29	30	AC29	GXBL_1D_RX0n
GXBL_1CBp	AF28	27	28	AB28	GXBL_1DBp
GXBL_1CBn	AF27	25	26	AB27	GXBL_1DBn
GXBL_1C_TX5p	AL34	23	24	AD32	GXBL_1C_RX5p
GXBL_1C_TX5n	AL33	21	22	AD31	GXBL_1C_RX5n

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Table 3.4 – continued from previous page

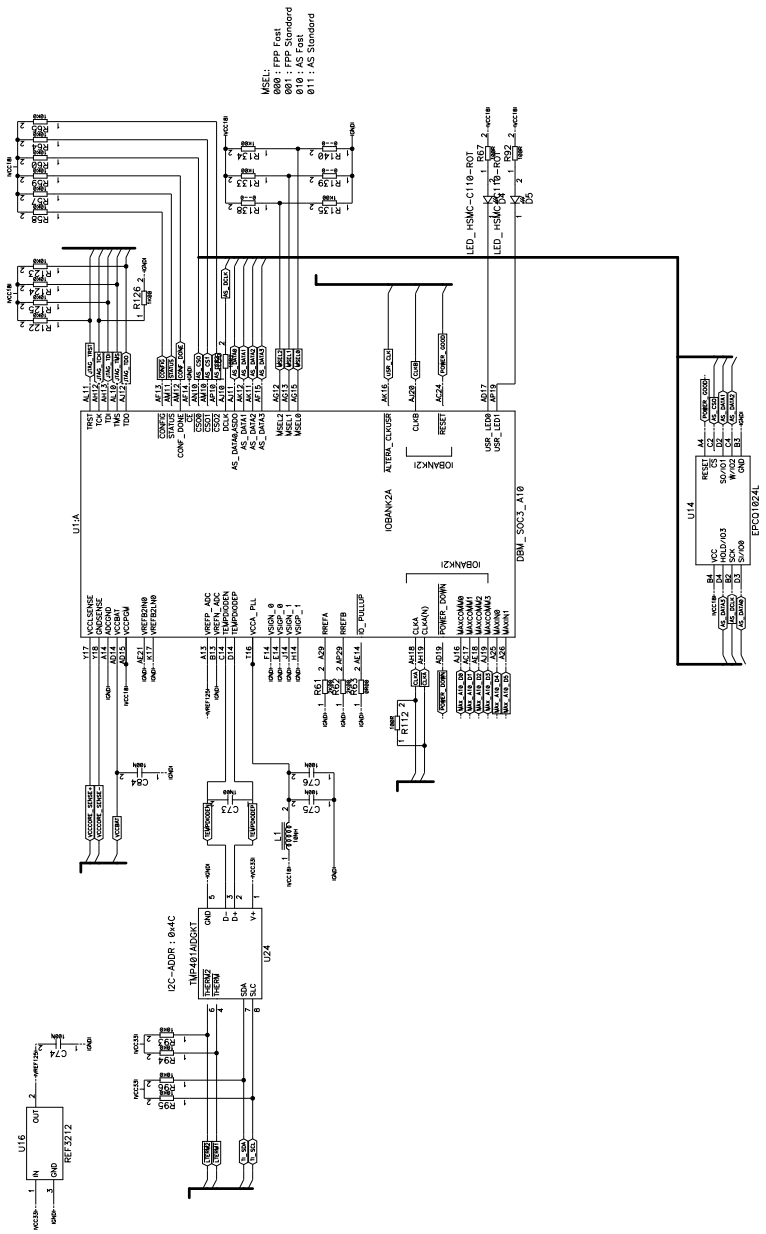
Function	FPGA	#	#	FPGA	Function
GXBL_1C_TX4p	AN34	19	20	AE30	GXBL_1C_RX4p
GXBL_1C_TX4n	AN33	17	18	AE29	GXBL_1C_RX4n
GXBL_1C_TX3p	AH32	15	16	AF32	GXBL_1C_RX3p
GXBL_1C_TX3n	AH31	13	14	AF31	GXBL_1C_RX3n
GXBL_1C_TX2p	AK32	11	12	AG30	GXBL_1C_RX2p
GXBL_1C_TX2n	AK31	9	10	AG29	GXBL_1C_RX2n
GXBL_1C_TX1p	AM32	7	8	AJ30	GXBL_1C_RX1p
GXBL_1C_TX1n	AM31	5	6	AJ29	GXBL_1C_RX1n
GXBL_1C_TX0p	AP32	3	4	AL30	GXBL_1C_RX0p
GXBL_1C_TX0n	AP31	1	2	AL29	GXBL_1C_RX0n

3.10 Schematics

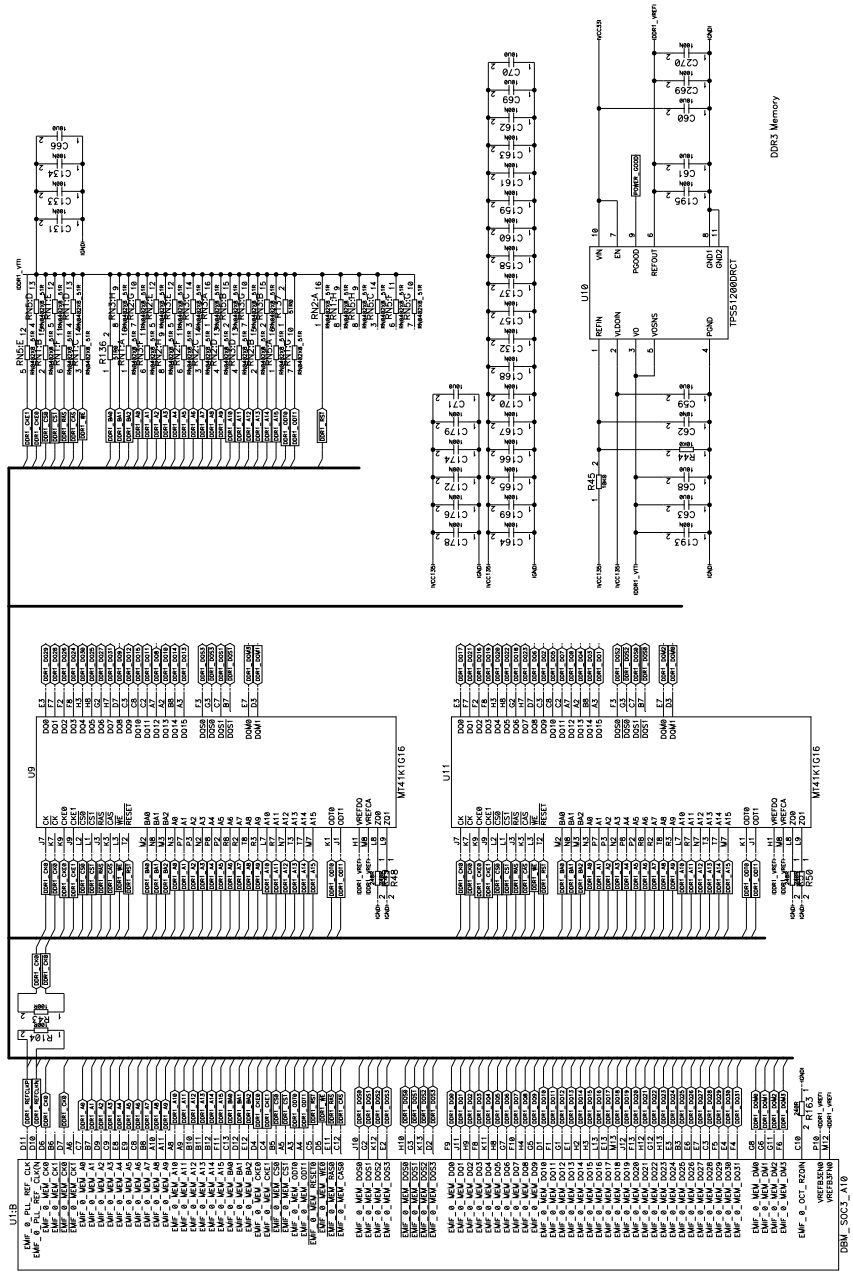
3.10.1 Library Component

A component for the MAX SoM is available on request that can be used for own baseboard developments.

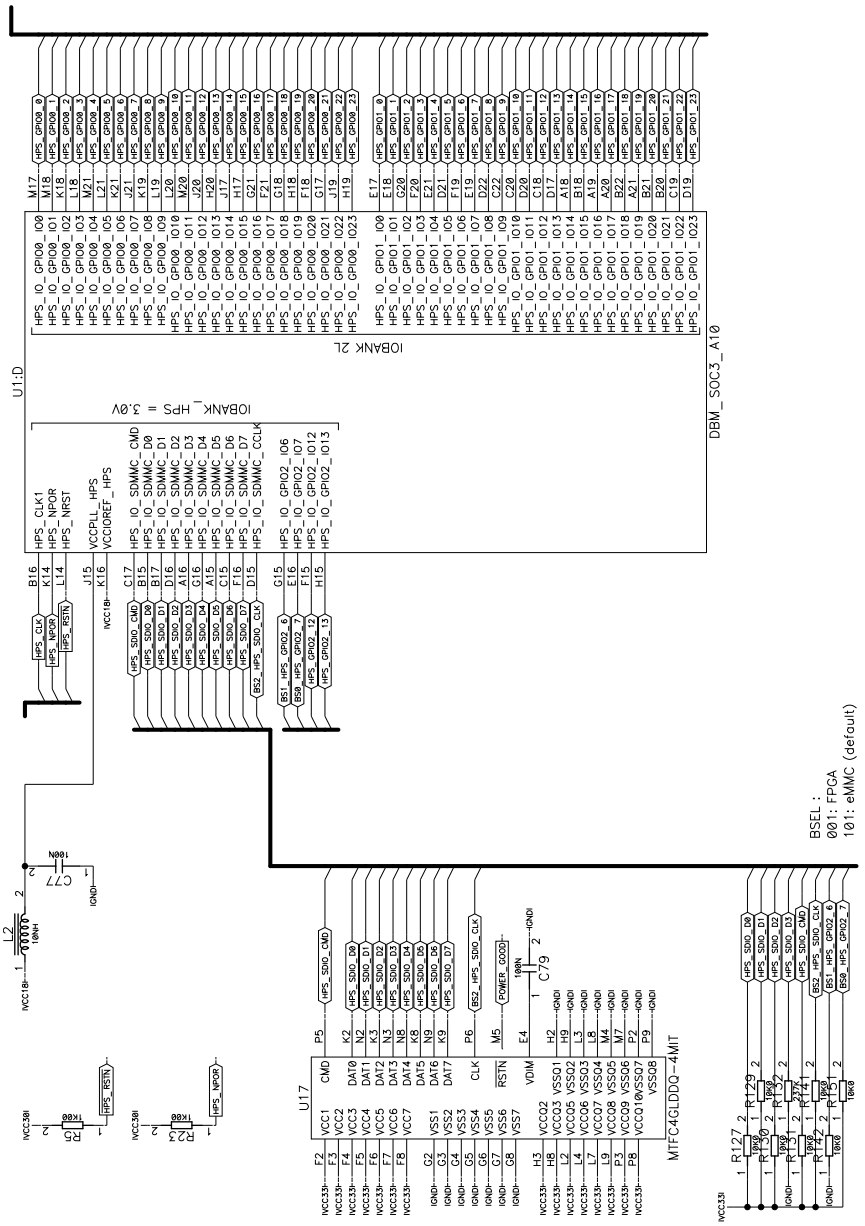
3.10.2 FPGA



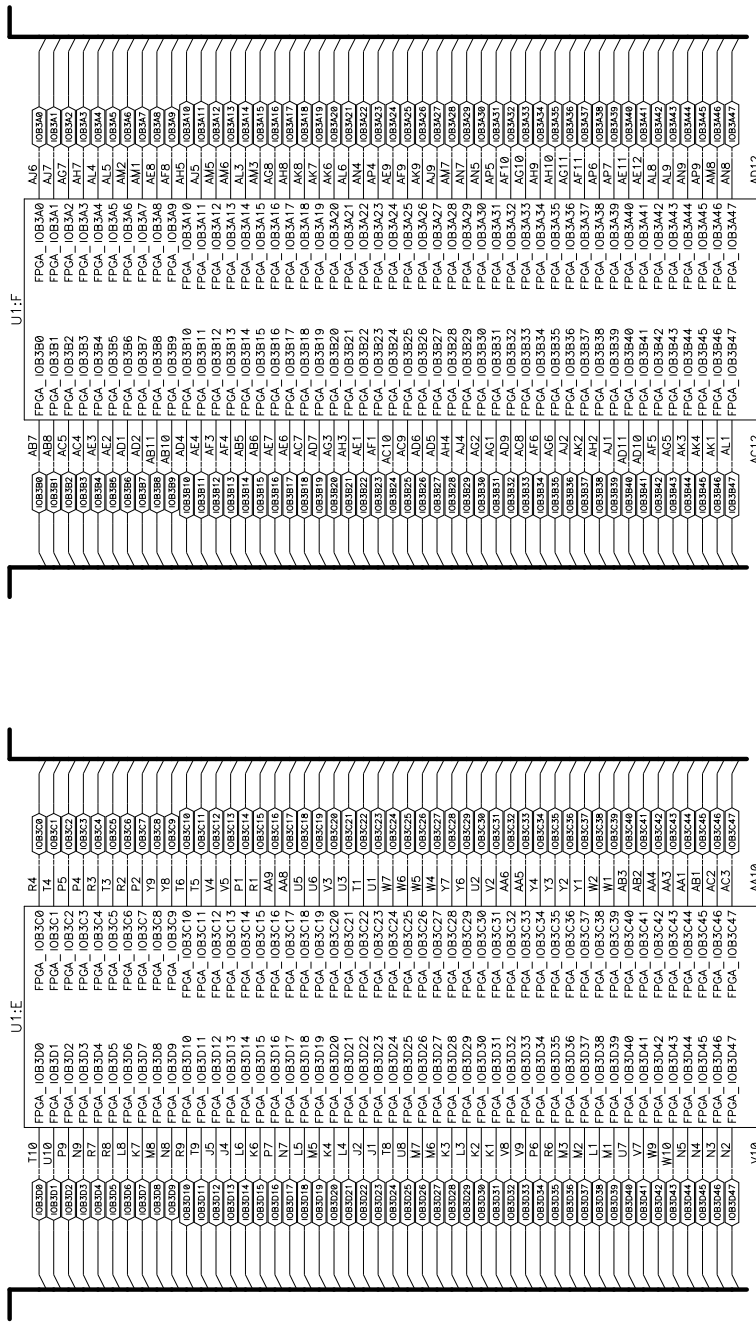
3.10.3 DDR3-HPS



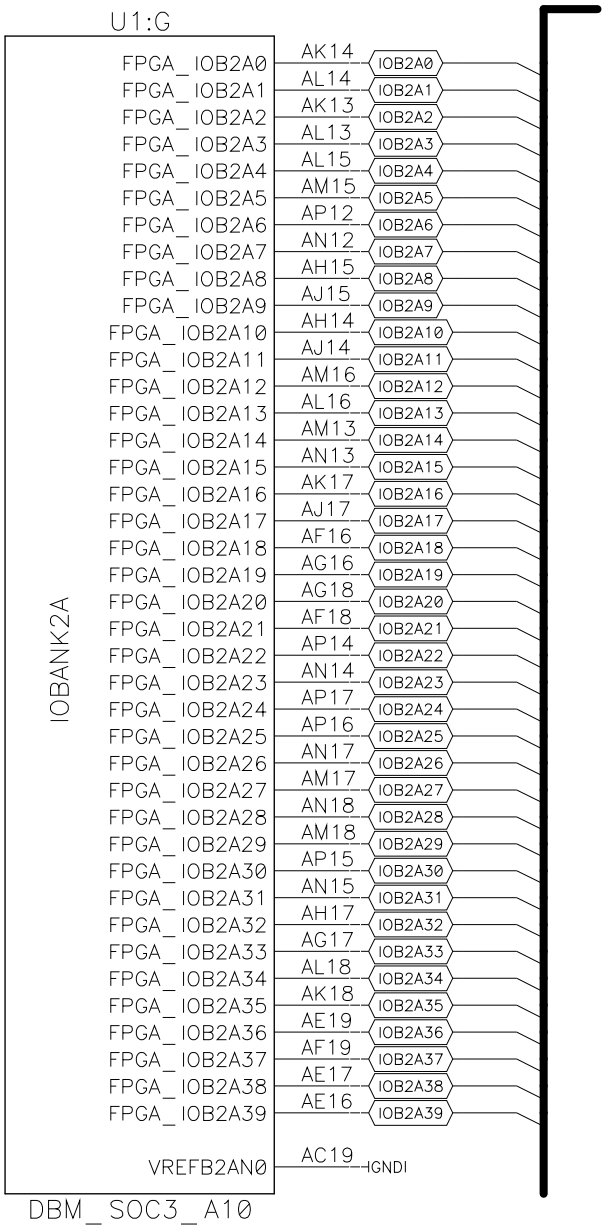
3.10.4 HPS



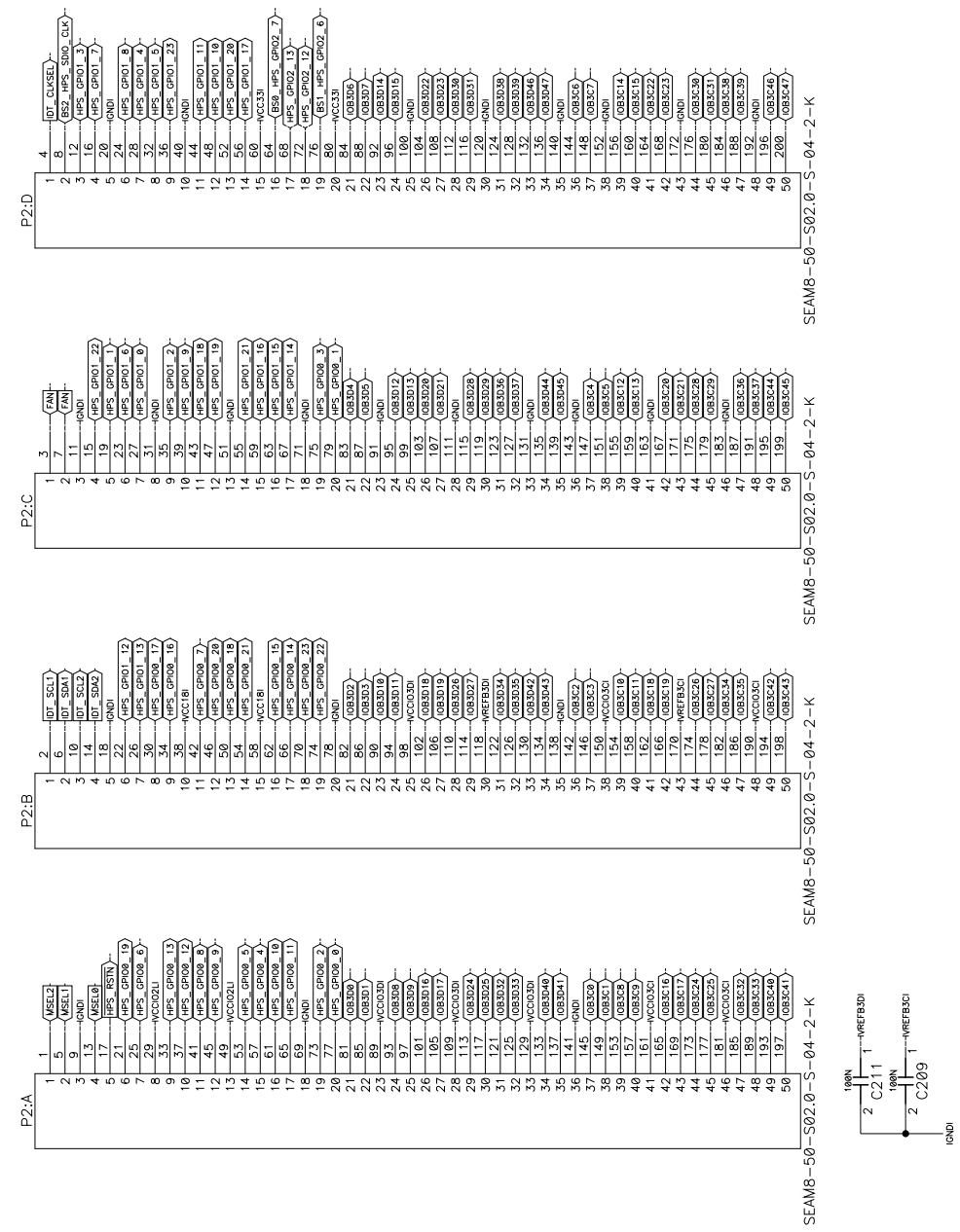
3.10.5 IO-BANK 3A, 3B, 3C, 3D



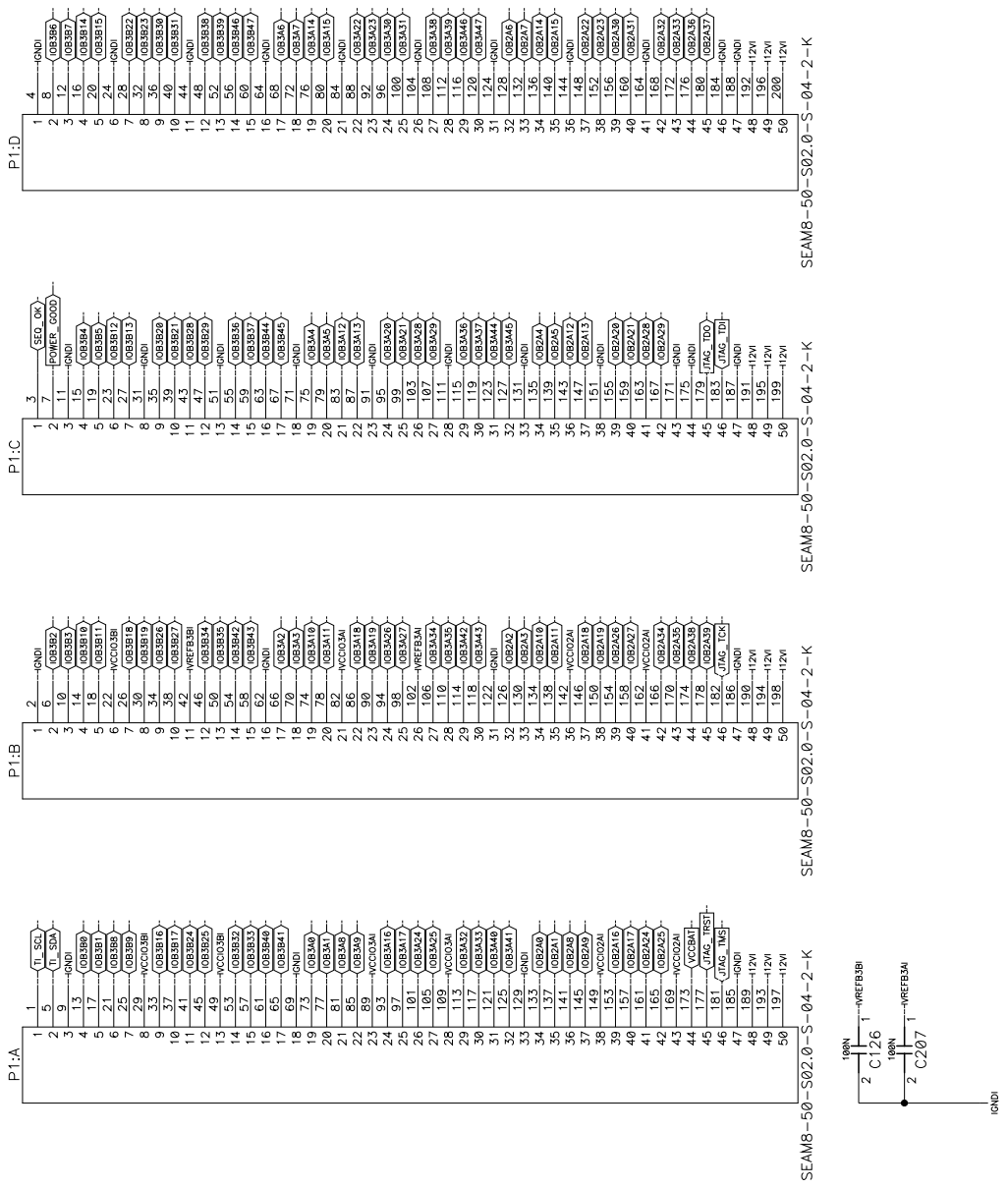
3.10.6 IO-BANK 2A



3.10.7 Pin Header P2



3.10.8 Pin Header P1

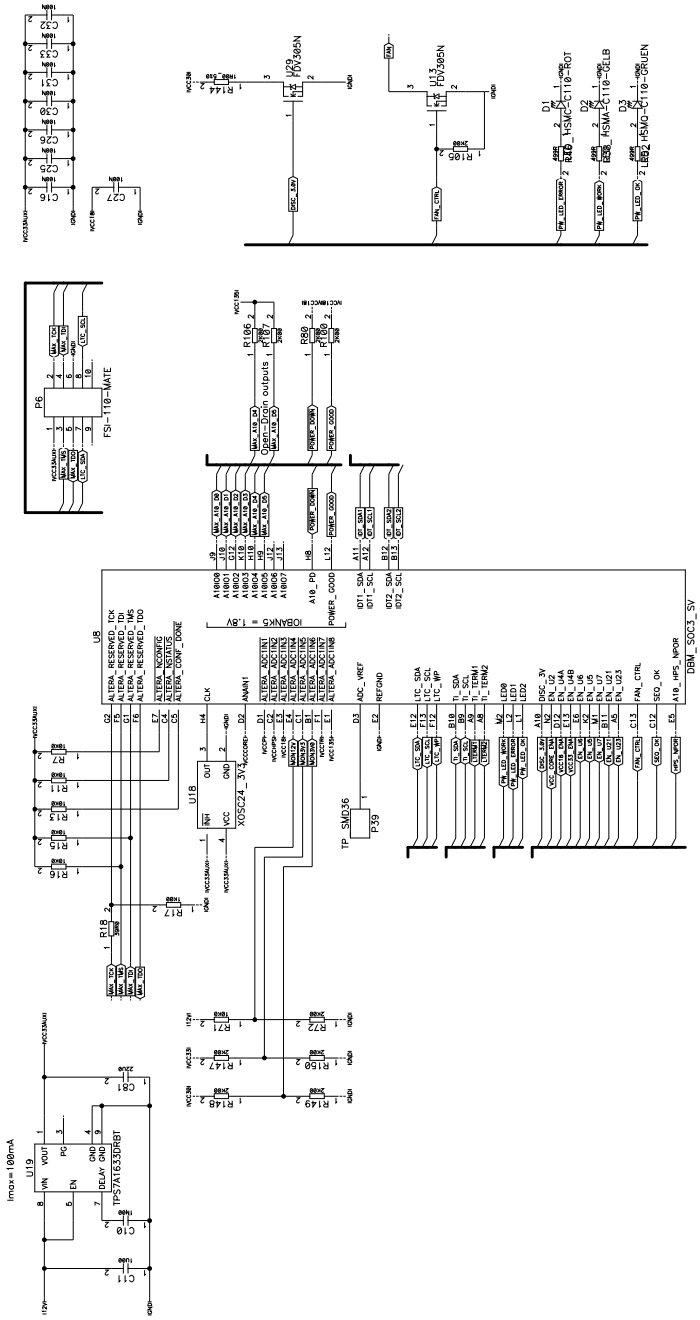


3.10.9 Hidden Power Pins

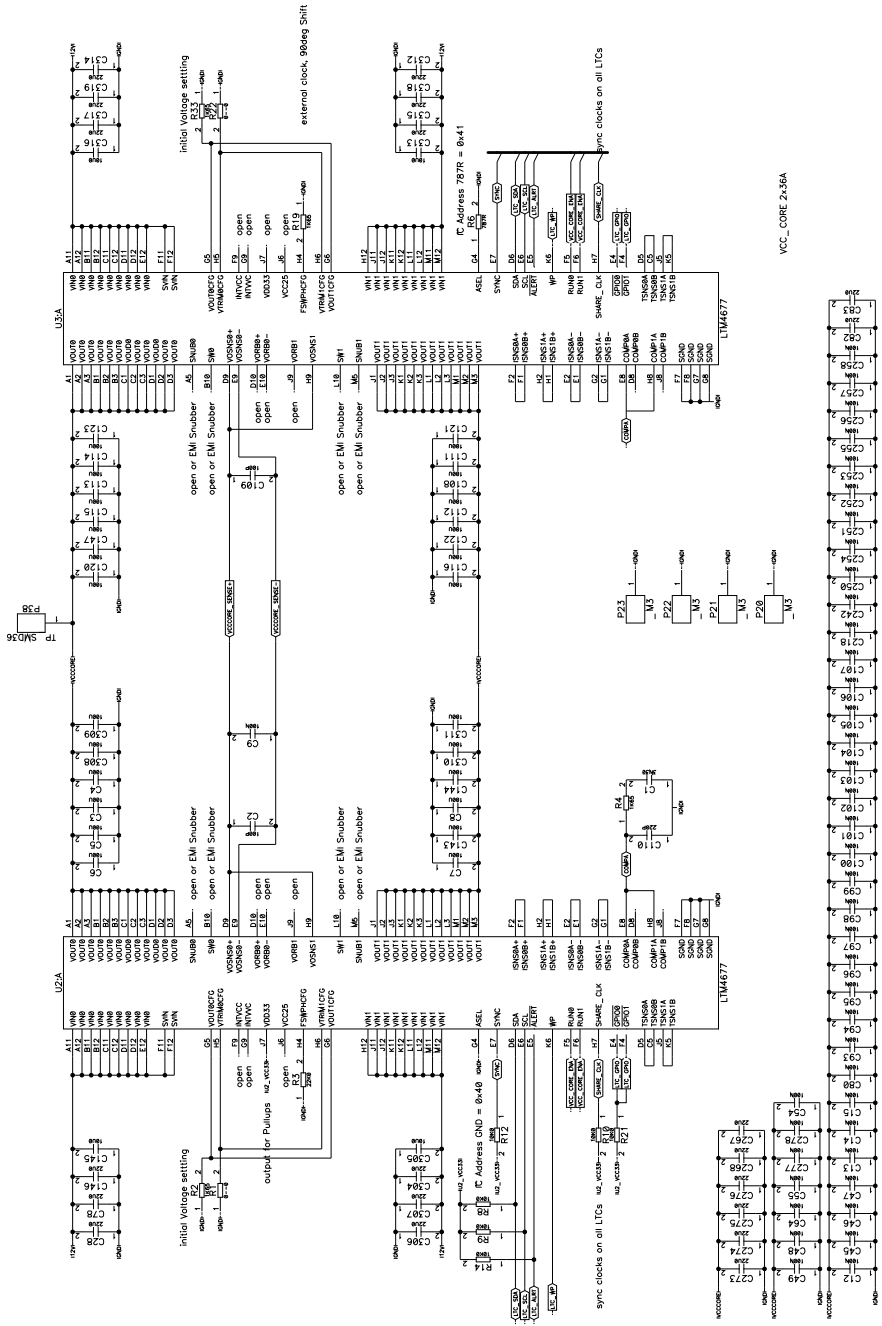
Power Table

Ref Des	Device(Type)	Package	GND	VCCIO2A	VCCCORE	VCCIO3D	VCC18	VCCIO3C	VCCIO3B	VCCIO3A	VCCIO2L	VCCP	VCC135	VCC30	VCCTR	VCCHPS	VCC33AUX
U1	DBM_SOC3_A10	BGA1152A	AP33,AP30,AP28,AP23,AP18,AP13,AP11,AP8,AN32,AN31,AN30,AN26,AN21,AN16,AN11,AN6,AM34,AM33,AM30,AM29,AM28,AM24,AM19,AM14,AM9,AM4,AL32,AL31,AL28,AL22,AL17,AL12,AL7,AL2,AK34,AK33,AK30,AK29,AK28,AK25,AK10,AK5,AJ32,AJ31,AJ28,AJ18,AJ13,AJ8,AJ3,AH34,AH33,AH30,AH29,AH28,AH21,AH11,AH6,AH1,AG32,AG31,AG28,AG27,AG26,AG19,AG14,AG4,AF34,AF33,AF30,AF29,AF26,AF7,AF2,AE32,AE31,AE26,AE15,AE13,AE5,AD34,AD33,AD30,AD29,AD26,AD23,AD21,AD18,AD13,AD3,AC32,AC31,AC25,AC16,AC11,AC1,AB34,AB33,AB30,AB29,AB26,AB19,AB4,AA32,AA31,AA26,AA25,AA22,AA17,AA12,AA2,Y34,Y33,Y30,Y29,Y26,Y25,Y20,Y15,Y10,W32,W31,W25,W23,W18,W13,W3,V34,V33,V30,V29,V26,V25,V21,V16,V11,V6,V1,U32,U31,U26,U24,U19,U14,U4,T34,T33,T30,T29,T26,T22,T17,T12,T2,R32,R31,R25,R20,R15,R10,R5,P34,P33,P30,P29,P26,P23,P18,P13,P3,N32,N31,N26,N21,N6,N1,M34,M33,M30,M29,M26,M25,M19,M14,M4,L32,L31,L25,L22,L17,L12,L7,L2,K34,K33,K30,K29,K28,K27,K26,K20,K15,K5,J32,J31,J28,J8,J3,H34,H33,H30,H29,H28,H26,H21,H16,H6,H1,G32,G31,G28,G14,G9,G4,F34,F33,F30,F29,F28,F27,F7,F2,E32,E31,E28,E25,E20,E15,E10,E5,D34,D33,D30,D29,D28,D23,D18,D13,D8,D3,C32,C31,C28,C26,C21,C16,C11,C6,C1,B34,B33,B30,B29,B28,B24,B19,B14,B9,B4,B2,A33,A32,A31,A30,A28,A27,A22,A17,A12,A7	AK15,AH16,AF17	AC21,AC18,AB25,AB24,AB23,AB21,AB18,AB17,AB14,AB13,AB12,AA24,AA23,AA19,AA18,AA16,AA13,AA11,Y24,Y23,Y22,Y21,Y19,Y16,Y14,Y13,Y12,Y11,W24,W22,W21,W20,W19,W17,W16,W15,W14,W12,W11,V24,V23,V22,V20,V19,V18,V17,V15,V14,V13,V12,U25,U21,U20,U16,U15,U12,U11,T25,T24,T23,T21,T20,T19,T13,T11,R24,R23,R22,R21,R19,R18,R17,R16,R14,R13,R12,R11,P25,P24,P22,P17,P14,P12,P11,N25,N24,N23,N18,N17,N16,N13,N12	U9,T7,P8	AK20,AF22,AE20,AC26,AA21,AA20,AA15,AA14,W26,R26,P21,P20,P19,P16,P15,L26	AA7,Y5,W8	AD8,AC6,AB9	AG9,AF12,AE10	J18,G19,F17	AB22,AB20,AB16,AB15,U23,U22,U18,U17,U13,N22,N20,N19,N15,N14	AJ23,AG24,AE25,N11,M9,K10,J23,J13,H11,G24,F22,F12	J16	AE28,AE27,AC28,AC27,AA28,AA27,W28,W27,U28,U27,R28,R27,N28,N27,L28,L27	M16,M15,L16,L15	
U8	DBM_SOC3_SV	BGA0169A	N13,N1,M6,L9,J4,H12,G7,F3,E11,D5,C3,B8,A13,A1				J11,H11										L8,L7,L6,K9,K4,K3,J3,H7,G11,G8,G6,G3,F11,F7,F2,D10,D4,C8,C7,C6
U9	MT41K1G16	BGA0096A	T9,T1,P9,P1,M9,M1,J8,J2,G9,G8,G1,F9,E8,E2,E1,D8,D1,B9,B3,B1,A9										R9,R1,N9,N1,K8,K2,H9,H2,G7,F1,E9,D9,D2,C9,C1,B2,A8,A1				
U11	MT41K1G16	BGA0096A	T9,T1,P9,P1,M9,M1,J8,J2,G9,G8,G1,F9,E8,E2,E1,D8,D1,B9,B3,B1,A9										R9,R1,N9,N1,K8,K2,H9,H2,G7,F1,E9,D9,D2,C9,C1,B2,A8,A1				
U12	MT41K1G16	BGA0096A	T9,T1,P9,P1,M9,M1,J8,J2,G9,G8,G1,F9,E8,E2,E1,D8,D1,B9,B3,B1,A9										R9,R1,N9,N1,K8,K2,H9,H2,G7,F1,E9,D9,D2,C9,C1,B2,A8,A1				
U15	MT41K1G16	BGA0096A	T9,T1,P9,P1,M9,M1,J8,J2,G9,G8,G1,F9,E8,E2,E1,D8,D1,B9,B3,B1,A9										R9,R1,N9,N1,K8,K2,H9,H2,G7,F1,E9,D9,D2,C9,C1,B2,A8,A1				

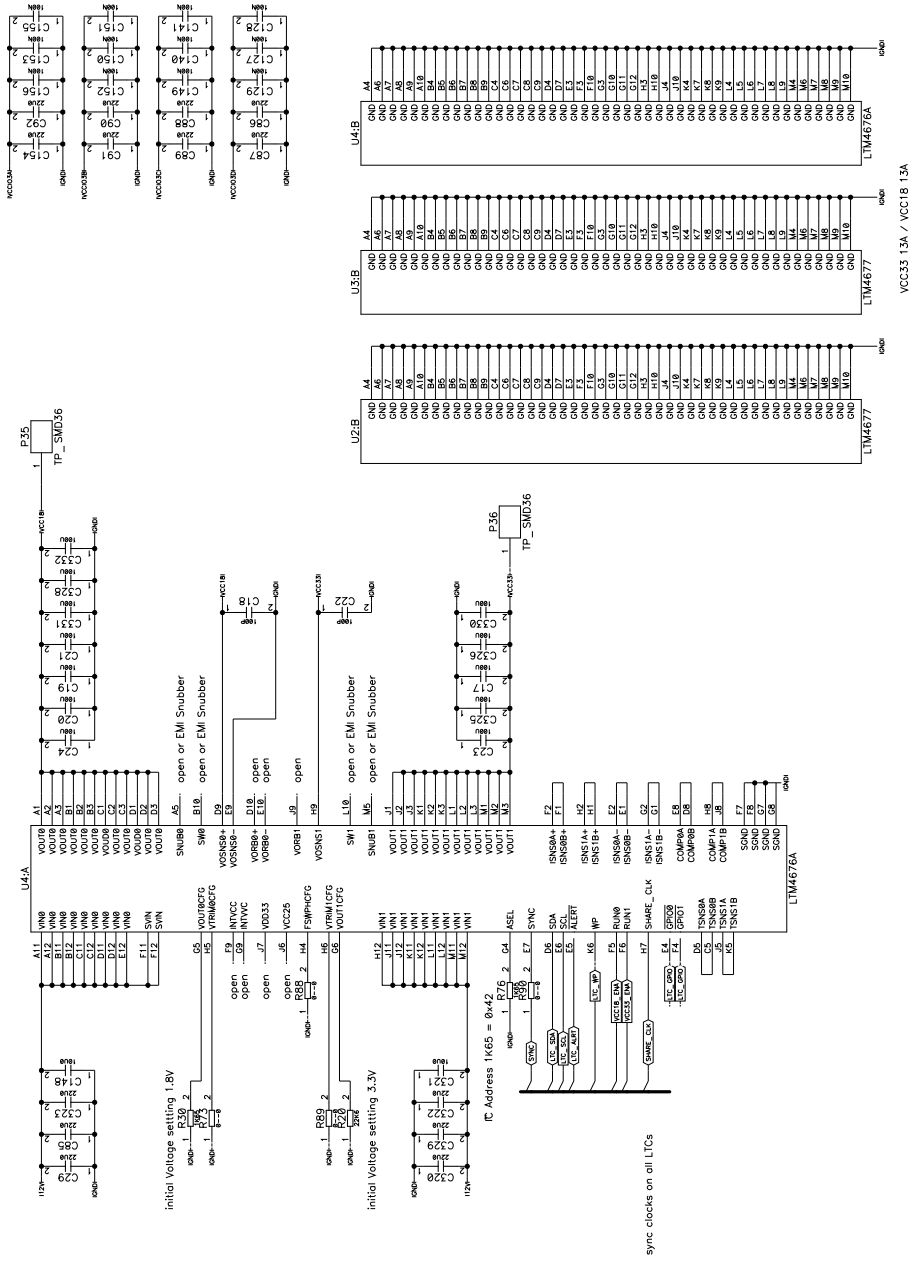
3.10.10 Power Supply 1



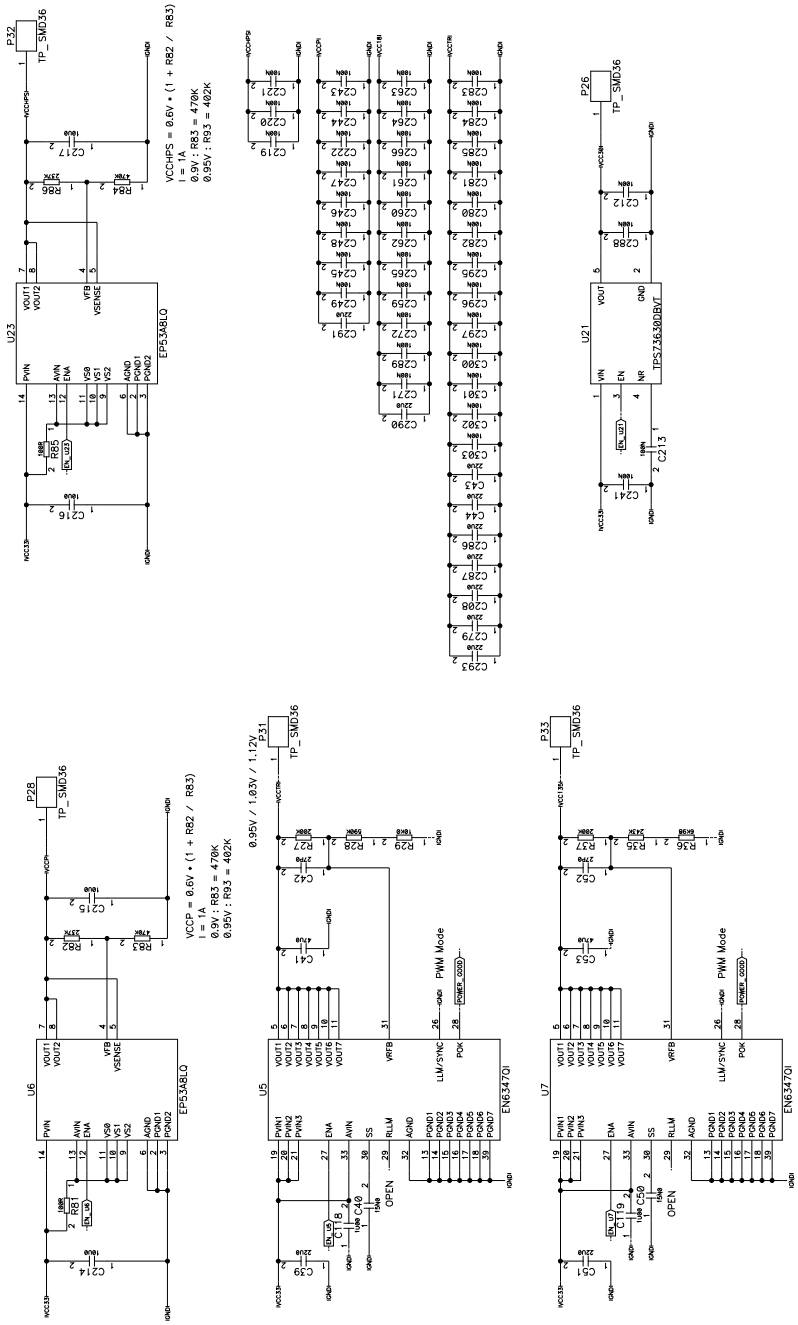
3.10.11 Power Supply 2



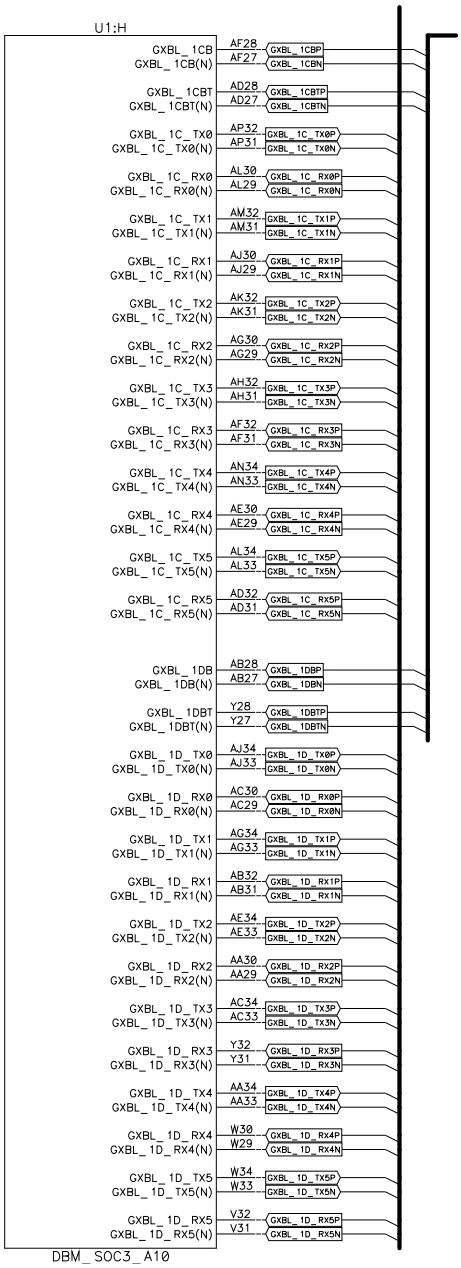
3.10.12 Power Supply 3



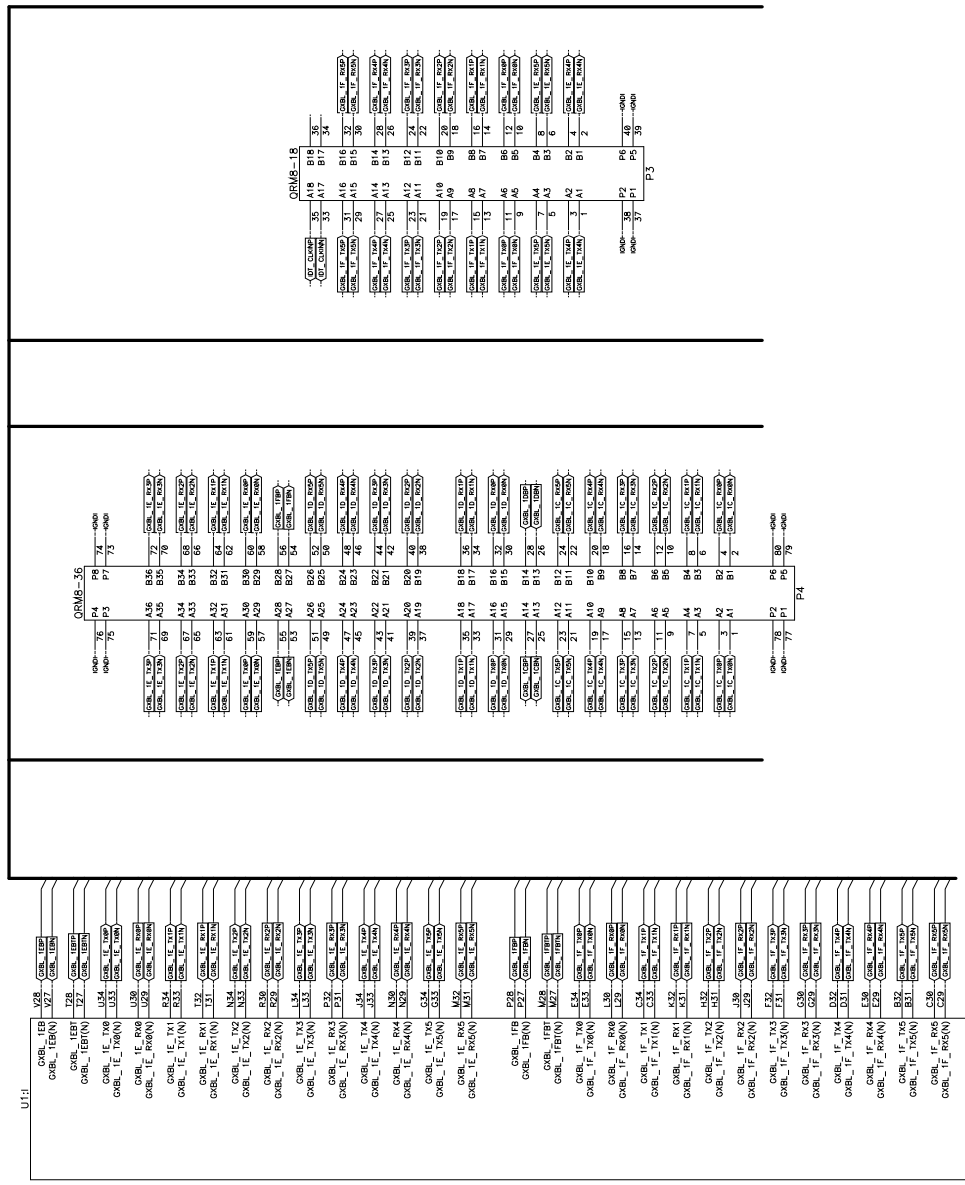
3.10.13 Power Supply 4



3.10.14 Transceiver C / D



3.10.15 Transceiver E / F Connector P3, P4



3.10.16 Clock Generation