MA5D4 System on Module

Users and Hardware Manual

V0.3
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1.1 Imprint

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2 MA5D4 System on Module

The MA5D4 supports high-performance, secure, and cost-sensitive industrial applications. High-speed computing needs are supported by ARM Neon and a 128kB L2 cache that increases the overall system performance. The MA5D4 System on Module is an ideal fit for low-cost user interface applications that require video playback. The high-grade security features allow you to protect any system against counterfeiting and software theft, while also enabling you to securely store and transfer data.

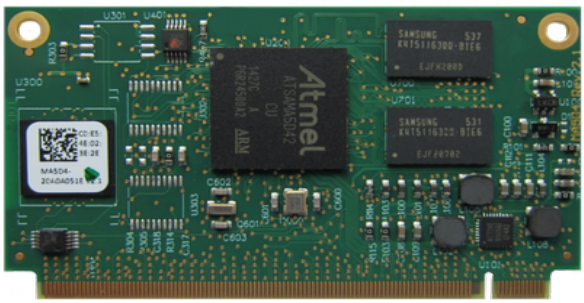

Figure 1: MA5D4 System on Module

The SAMA5D4 CPU supports

- ARM® Cortex®-A5 running at 600Mhz (945DMIPS).
- ARM Neon for high-precision computing and acceleration of complex algorithms including multimedia.
- 128KB of L2 cache for system performance.
- 720p hardware video decoder supporting H264/263, VP8, JPEG.
- Graphic LCD TFT controller with overlays for image composition.
- CMOS image sensor interface.
- Three High Speed USB ports (configurable as three hosts or two hosts and one device port).
- Dual EMAC 10/100 with IEEE1588 support.
- Advanced security features to prevent counterfeiting, secure communication, and system authentication:
  - On-the-fly encryption/decryption of code from external DDR.
  - Encryption engines supporting AES/3DES, RSA, ECC - TRNG, SHA.
  - Tamper detection pins.
  - Memory content protection (secure key storage).

2.1 Feature Set

The MA5D4 System on Module supports

- Atmel SAMA5D44 Cortex A5 @ 528MHz
- 128 – 512MB DDR2 RAM
- 4 MB MByte SPI NOR-Flash
- 4 – 32GB eMMC Flash (optionally 256MB NAND Flash)
- 720p hardware video decoder supporting H264/263, VP8, JPEG.
- 230-pin MXM2 edge connector supporting
  - HDMI
  - TFT controller, overlay support for image composition
  - resitive Touchscreen controller
  - Camera – CMOS image sensor interface
  - external bus A/D 25/16 bit
  - 2x 10/100MBit Ethernet, IEEE1588 support
  - 2xUSB Host / 1x USB OTG
  - 1x/2x CAN optionally
  - SD-card
- RTC
- ~500mW power dissipation
- size 70 x 40mm

2.2 Block Diagram

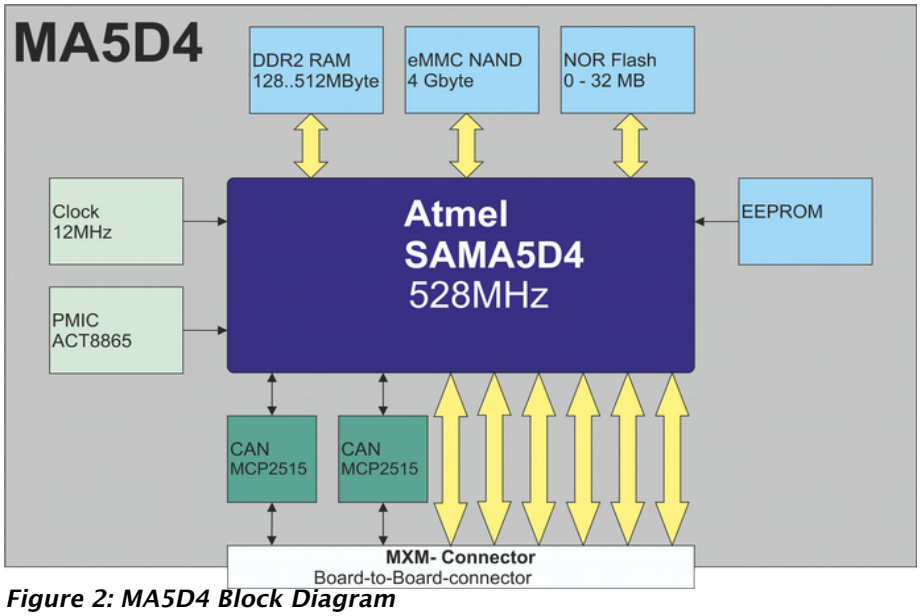

Figure 2: MA5D4 Block Diagram

2.3 Dimensions

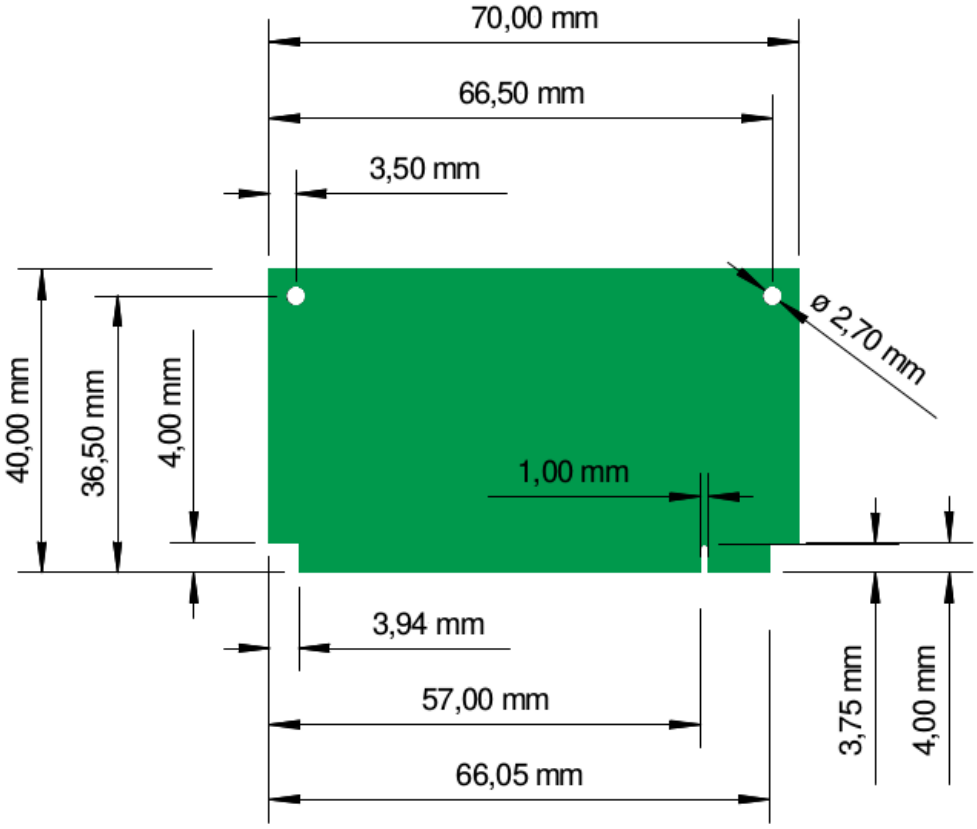

Figure 3: MA5D4 Dimensions

2.4 Components Location

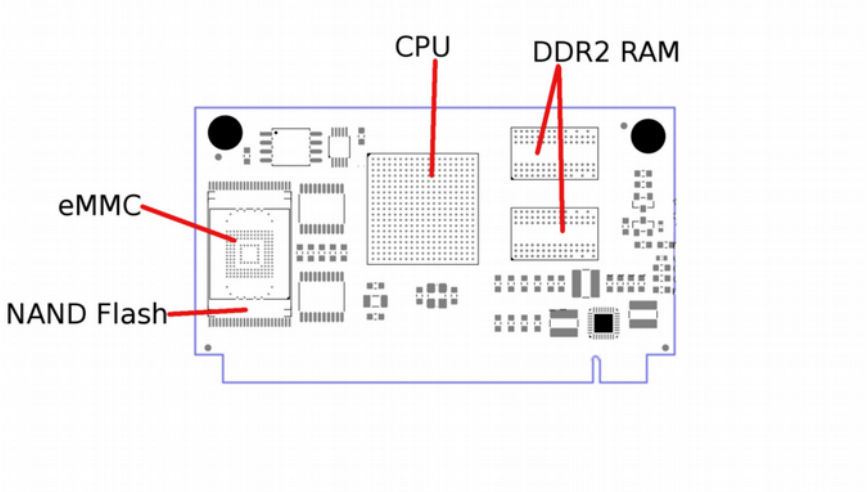

Figure 4: MA5D4 Components Location

2.5 Product Options

Example: MA5D4-2BA0A051E

Component	Option	Value
CPU	1	n.a.
MA5D4-**2**BA0A051I	2	SAMA5D42
	3	n.a.
	4	SAMA5D44
SPI NOR	0	n.p.
MA5D4-2**B**A0A051I	A	2 MBit
	B	4 MBit
eMMC NAND Flash	0	n.p.
MA5D4-2B**A**0A051I	A	4 GByte
	B	8 GByte
	C	16 GByte
	D	32 GByte
	E	64 GByte
NAND Flash	0	n.p.
MA5D4-2BA**0**A051I	1	128 MByte
	2	256 MByte
	3	512 MByte
DDR2 RAM	A	128 MByte
MA5D4-2BA0**A**051I	B	256 MByte
	C	512 MByte
CAN	0	n.p.
MA5D4-2BA0A**0**51I	A	1x CAN interface
	B	2x CAN interfaces
Speed	5	528 MHz
MA5D4-2BA0A0**5**1I		
RTC	0	n.p.
MA5D4-2BA0A05**1**I	1	RTC populated
temp.-range	0	0°C....+70°C
MA5D4-2BA0A051**I**	E	-25°C...+85°C
	I	-40°C...+85°C

2.6 Overview

2.6.1 SAMA5D4 Processor

The SAMA5D4 processor is based on a CortexA5 core. It integrates the ARM NEONTM SIMD engine for accelerated signal processing, multimedia and graphics as well as a 128 KB L2-Cache for high system performance. The device features the ARM TrustZone ® enabling a strong security perimeter for critical software, as well as several hardware security features. The device also features advanced user interface and connectivity peripherals.

The SAMA5D4 supports

- ARM Cortex-A5 Core
- ARM TrustZone
- NEON Multimedia Architecture
- 832 MIPS @ 528 MHz in worst conditions
- 32 Kbyte Data Cache, 32 Kbyte Instruction Cache
- 128 Kbyte L2 Cache
- Video Decoder (VDEC) supporting formats MPEG-4, H.264, H.263, VP8 and JPEG, and image postprocessing
- LCD TFT Controller with 4 overlays up to 2048x2048 or up to 720p in video format, with rotation and alpha blending
- ITU-R BT. 601/656 Image Sensor Interface (ISI)
- One USB Device High-Speed, Three USB Host High-Speed with On-chip Transceiver
- Two 10/100 Mbps Ethernet MAC Controllers with IEEE 1588 v2 support
- Up to 152 I/Os

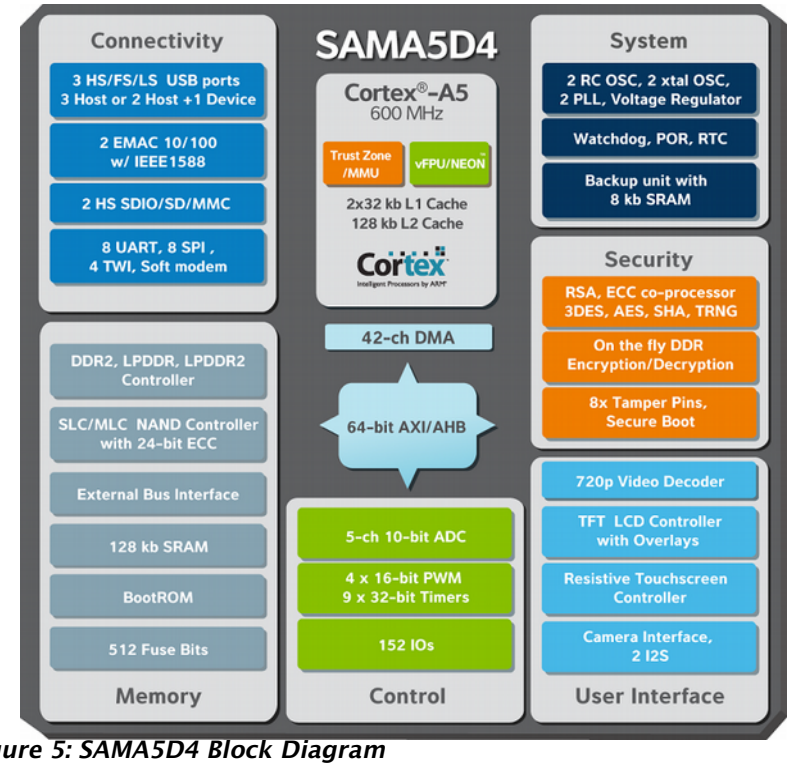

Figure 5: SAMA5D4 Block Diagram

The SAMA5D4 CPU is available as follows:

CPU	Video Decode	DDR2 RAM width
SAMA5D44	yes	32 bit
SAMA5D43	yes	16 bit
SAMA5D42	no	32 bit
SAMA5D41	no	16 bit

Table 1: SAMA5D4 Derivatives

On MA5D4 the SAMA5D44 and SAMA5D42 derivatives are supported.

2.6.2 DDR2 RAM

The SAMA5D4 CPU supports the following memory architecture:

- Memory Management Unit
- 32 Kbyte Data Cache, 32 Kbyte Instruction Cache
- 128 Kbyte L2 Cache
- One 128 Kbyte scrambled internal ROM single-cycle access at system speed, embedding Atmel boot loader/Atmel Secure boot loader
- One 128 Kbyte scrambled internal SRAM, single-cycle access at system speed
- High-bandwidth scramblable 16-bit or 32-bit Double Data Rate Multi-port Dynamic RAM Controller supporting
- 512 Mbyte 8-bank DDR2/LPDDR/LPDDR2, including partial areas “on-the-fly” AES encryption/decryption
- EBI (External Bus interface) supporting:
- 16-bit NAND flash controller, including 24-bit error correction code (PMECC) for 8-bit NAND Flash
- Independent Static Memory Controller (SMC) with datapath scrambling

The external DDR2 RAM is supported in 16-bit or 32-bit width:

- 512 Mbytes of address space on DDR CS and DDR/AES CS in 32-bit mode
- 256 Mbytes of address space on DDR CS and DDR/AES CS in 16-bit mode
- Supports 16-bit or 32-bit 8-banks DDR2, LPDDR and LPDDR2 memories

MA5D4 offers optionally 128MB, 256MB or 512MB DDR2 SDRAM in 32 Bit width.

MA5D4 uses the following DDR2 components:

DDR2 RAM Part Number	Organization
K4T51G163QQ-BIE6000	32Mx16
K4T1G164QG-BIE6000	64Mx16

Table 2: DDR2 RAM Components

The datasheet for these components can be achieved on the website of Samsung.

2.6.3 SPI Boot Flash

By default MA5D4 boots from the populated SPI NOR Flash. The SPI NOR Flash is connected to the SPI0 interface of the SAMA5D4 CPU using the CS0 Chip Select.

SPI NOR Part Number
AT25DF321A

Table 3: SPI NOR Components

The datasheet for these components can be achieved on the website of adesto® Technologies.

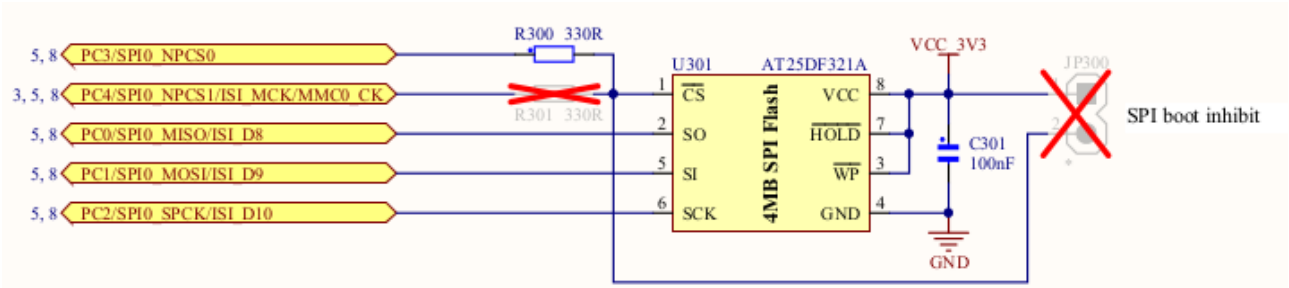

Figure 6: SPI NOR Flash

2.6.4 eMMC NAND Flash

By default MA5D4 is populated with 4GB eMMC NAND Flash memory. The eMMC NAND Flash is connected to the MMC0 interface of the CPU. The eMMC memory is connected using a connection width of 8 Bit.

The on-Board eMMC NAND Flash connected to the MMC0 interface can not be used for booting the CPU. Using an alternative boot-interface is recommended.

eMMC NAND Flash Part Number
MTFC4GMVEA-4M IT

Table 4: eMMC NAND Flash Components

The datasheet for these components can be achieved on the website of Toshiba.

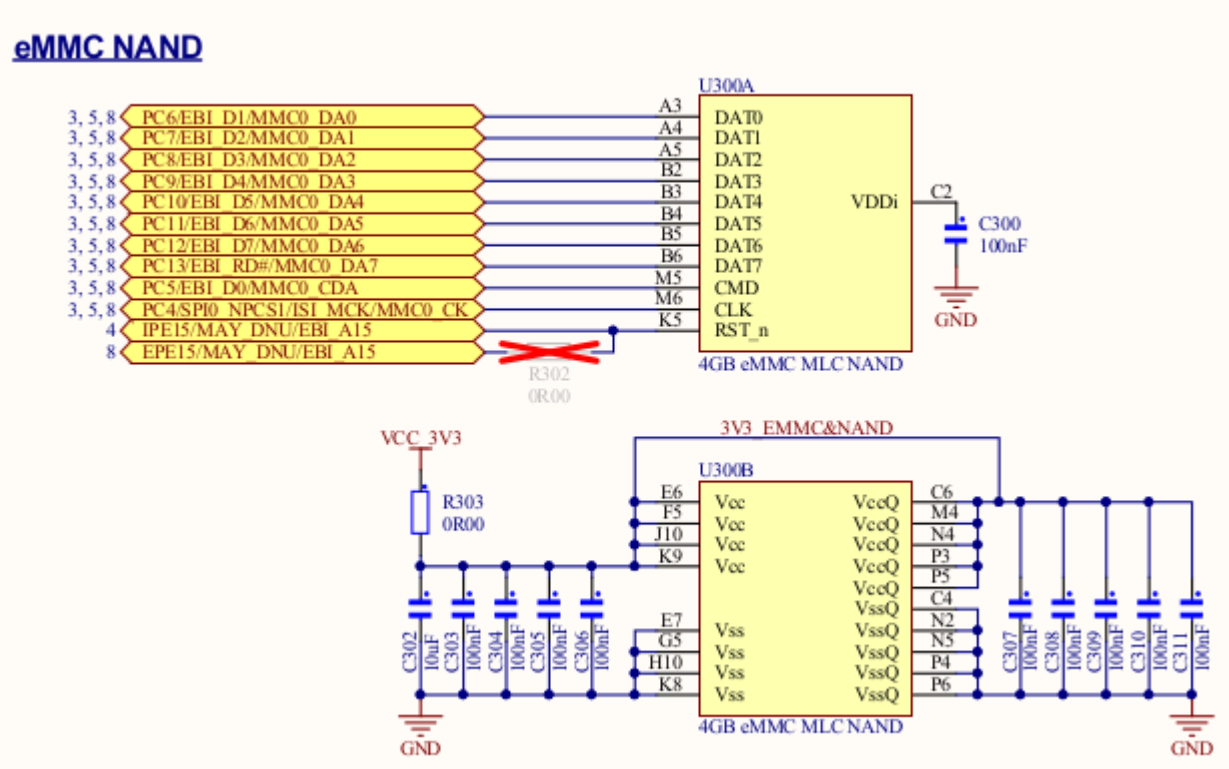

Figure 7: eMMC NAND Flash

2.6.5 NAND Flash

Optionally MA5D4 can be populated with NAND flash instead of eMMC NAND Flash memory. As this product option is not present in the default configuration please contact ARIES Embedded for more information.

2.6.6 CAN

Optionally MA5D4 supports up to 2 CAN interfaces.

CAN Interface	Chip Select	Interface SAMA5D4	Part Number
CAN1	NCS1	SPI1	MCP2515
CAN2	NCS2	SPI1	MCP2515

Table 5: CAN Interface Components

The datasheet for these components can be achieved on the website of Microchip.

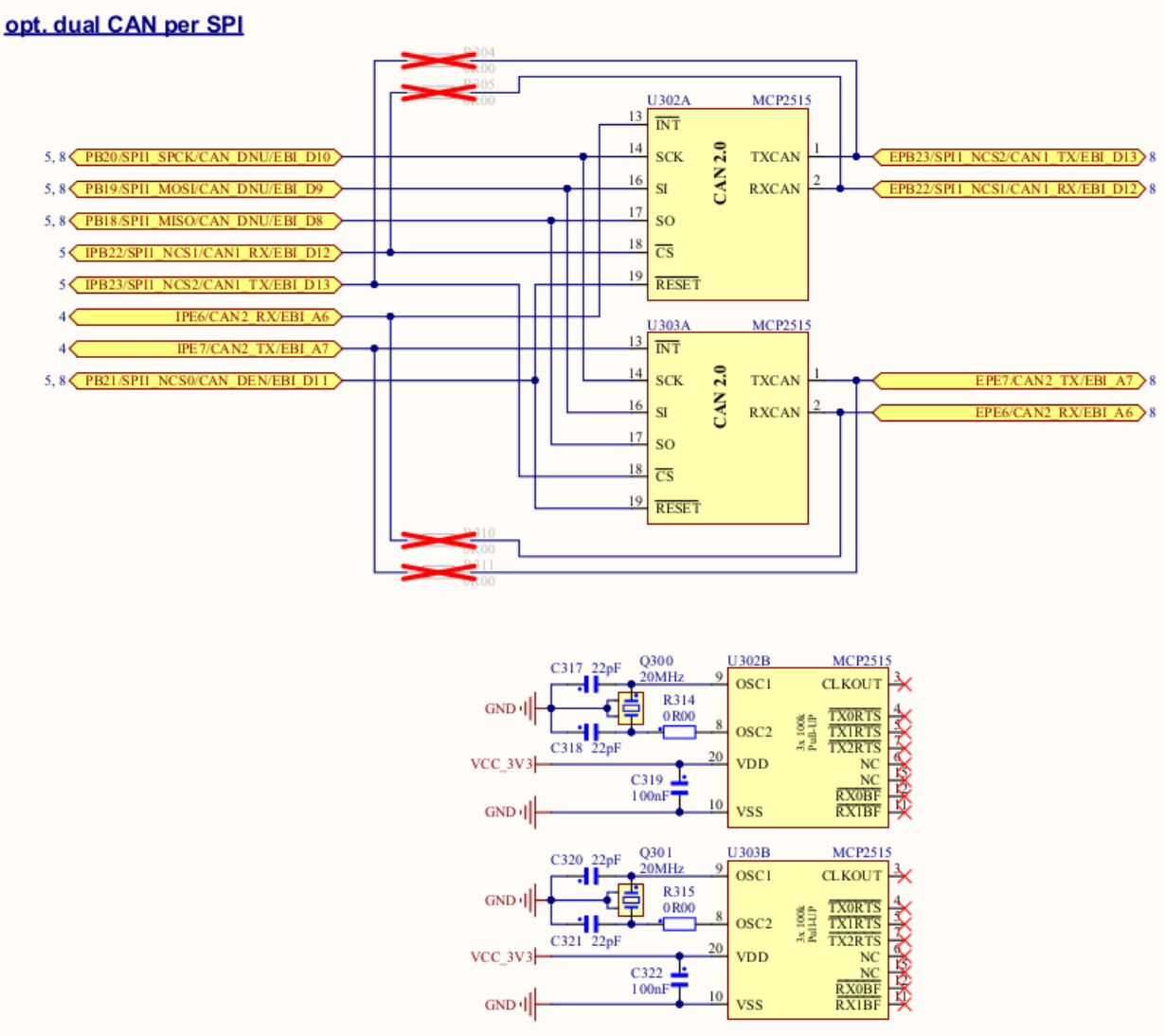

Figure 8: CAN Interface

More information on the signals of the CAN interfaces can be found in chapter '2.7.9 CAN'

2.6.7 PMIC

A ACT8865 is used for generating the necessary voltages as well as the power sequencing to run the MA5D4 board.

PMIC Part Number
ACT8865

Table 6: PMIC Part Number

The ACT8865 can be connected to the I2C0 interface. To prevent any failure of the PMIC device it can be disconnected from I2C0 and switched that way, that the I2C0 interface is available on the board to board connector accordingly.

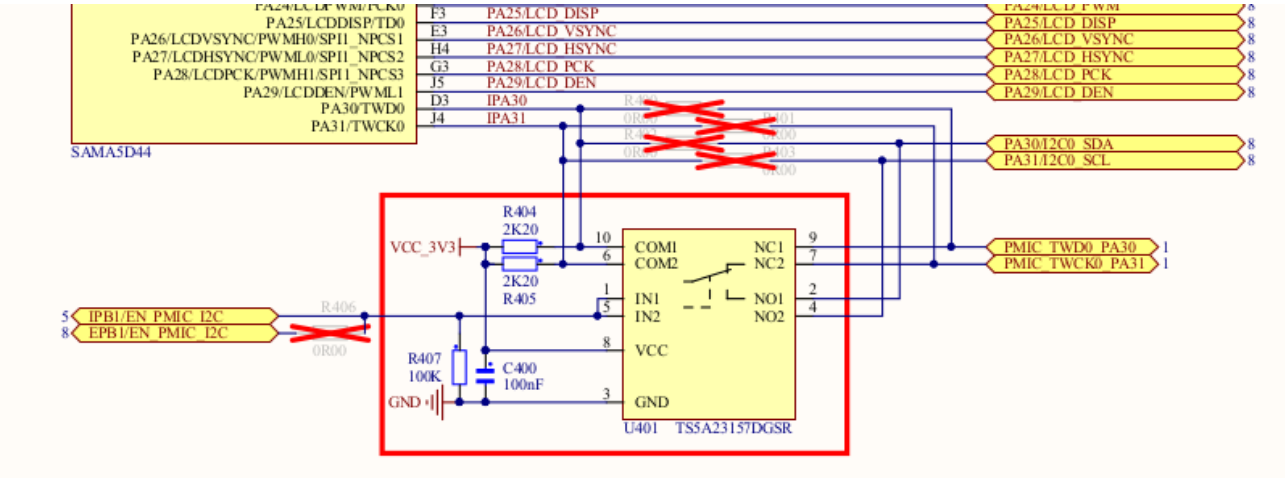

Figure 9: PMIC I2C0 Switch

The following signals are available on the edge connector to control the PMIC:

Pin	Voltage min./max.
24	PMIC_RESET#
22	PMIC_WAKE#
20	PMIC_SHDN
18	PMIC_WKUP

Table 7: PMIC Control Pins

2.6.7.1 Power Supply

For operating MA5D4 an appropriate voltage has to be supplied to the following pins:

Pin	Voltage min./max.	Pin Type
15	GND	Ground
13	GND	Ground
11	GND	Ground
9	GND	Ground
7	5V±10%	Supply
5	5V±10%	Supply
3	5V±10%	Supply
1	5V±10%	Supply

Table 8: Power Supply Pins

2.6.7.2 Back Up Voltage

The 2V supply onboard the MA5D4 is generated by a linear regulator and will be fed by either the 5V supply or the Vbat input. The 2V supply is fed into the CPU as V_{DDBU}.

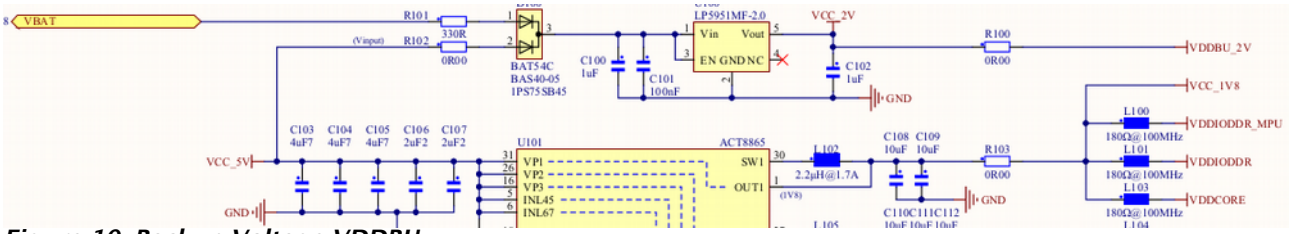

Figure 10: Backup Voltage VDDBU

To generate the 2V Vbat voltage the follwing pins can be supplied:

Pin	Voltage min./max.	Pin Type
17	2,5V ...5,5V	Vbat
7	5V±10%	Supply
5	5V±10%	Supply
3	5V±10%	Supply
1	5V±10%	Supply

Table 9: Backup Supply

2.6.7.3 Monitor Voltages

To check the MA5D4 system health the following voltages are supplied on the edge connector:

Pin	Voltage	Signal Name
21	NRST_2V	Voltage for Reset Pull-Up
19	NRST_3V3	Voltage for Reset Pull-Up
16	0,6V	Vout7
14	0,6V	Vout6
12	3,3V	VDDANA
10	2,5V	Fuse2V5
8	3,3V	VCC3V3
6	1,2V	1V2
4	1,8V	VCC1V8
2	2V	VDDBU_2V

Table 10: Reference Voltages

2.6.8 Clock

The SAMA5D4 clock generator is feeded by a 12MHz and 32.768 kHz quartz crystal.

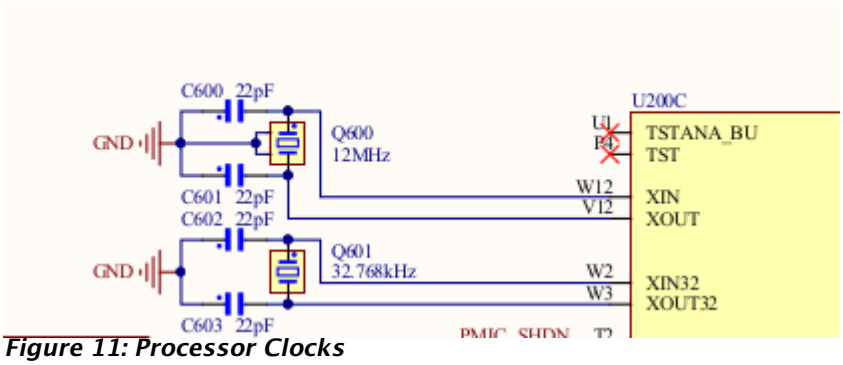

Figure 11: Processor Clocks

2.6.9 Pin Out

3rd use case	2nd use case	1st use case	Ball	Port	Pin Bottom	Pin Top	Port	Ball	1st use case	2nd use case	3rd use case
	JTAG_TMS/SWDIO	LCD_Data0	A7	PA0	229	230	PA1	F6	LCD_Data1		
	FEC1_TXCK	LCD_Data2	E6	PA2	227	228	PA3	C6	LCD_Data3		FEC1_RXCK
	FEC1_TXEN	LCD_Data4	D6	PA4	225	226	PA5	B6	LCD_Data5		FEC1_TXER
FEC1_CRS		LCD_Data6	A6	PA6	223	224	PA7	E5	LCD_Data7		
				GND	221	222	GND				
	JTAG_TCK/SWCLK	LCD_Data8	A5	PA8	219	220	PA9	F4	LCD_Data9		FEC1_COL
	FEC1_RXDV	LCD_Data10	F5	PA10	217	218	PA11	D5	LCD_Data11	FEC1_RXER	
	FEC1_RX0	LCD_Data12	G5	PA12	215	216	PA13	C5	LCD_Data13	FEC1_RX1	
	FEC1_TX0	LCD_Data14	E4	PA14	213	214	PA15	B5	LCD_Data15	FEC1_TX1	
				GND	211	212	GND				
	NTRST	LCD_Data16	H6	PA16	209	210	PA17	D4	LCD_Data17		
FEC1_RX2		LCD_Data18	G4	PA18	207	208	PA19	C4	LCD_Data19		FEC1_RX3
FEC1_TX2		LCD_Data20	A3	PA20	205	206	PA21	B4	LCD_Data21		FEC1_TX3
	FEC1_MDC	LCD_Data22	B3	PA22	203	204	PA23	A4	LCD_Data23	FEC1_MDIO	
				GND	201	202	GND				
prog. CLK0		LCD_PWM	H5	PA24	199	200	PA25	F3	LCD_DISP		
		LCD_VSYNC	E3	PA26	197	198	PA27	H4	LCD_HSYNC		
		LCD_PCK	G3	PA28	195	196	PA29	J5	LCD_DEN		
ISI_SDA	AUDIO_SDA	HDMI_I²C_SDA	D3	PA30	193	194	PA31	J4	HDMI_I²C_SCL	AUDIO_SCL	ISI_SCL
				GND	191	192	GND				
		FEC0_TXCK	C3	PB0	189	190	PB1	A2	iPMIC_I2C/eDNU	FEC0_RXCK	
		FEC0_TXEN	B2	PB2	187	188	PB3	C2	ISI_VSYNC	FEC0_TXER	
	FEC0_CRS	ISI_HSYNC	J3	PB4	185	186	PB5	H2	ISI_PWD	FEC0_COL	
		FEC0_RXDV	G2	PB6	183	184	PB7	H3	FEC0_RXER		
		FEC0_RX0	F2	PB8	181	182	PB9	J2	FEC0_RX1		
prog. CLK2	FEC0_RX2	AUDIO_MCLK	F1	PB10	179	180	PB11	K4	ISI_RST	FEC0_RX3	
		FEC0_TX0	D2	PB12	177	178	PB13	K3	FEC0_TX1		
PWM	FEC0_TX2		A1	PB14	175	176	PB15	E2	FEC0_TX3	HDMI_RST	PWM
		FEC0_MDC	B1	PB16	173	174	PB17	K5	FEC0_MDIO		
				GND	171	172	GND				
EBI_D8	iCAN_MISO/eDNU	SPI1_MISO	K2	PB18	169	170	PB19	C1	SPI1_MOSI	iCAN_MOSI/eDNU	EBI_D9
EBI_D10	iCAN_SCLK/eDNU	SPI1_SPCK	D1	PB20	167	168	PB21	L3	SPI1_NPCS0	iCAN_RSTn/eCAN_DEN	EBI_D11
EBI_D12	iCAN1_CS/eCAN1_RX	SPI1_NPCS1	G1	PB22	165	166	PB23	H1	SPI1_NPCS2	iCAN2_CS/eCAN1_TX	EBI_D13
EBI_D14		JTAG_TDI/DRxD	E1	PB24	163	164	PB25	J1	JTAG_TDO/DTxD		EBI_D15
		AUDIO_BCLK	M5	PB26	161	162	PB27	L2	AUDIO_BCLK	HDMI_TK0	

3rd use case	2nd use case	1st use case	Ball	Port	Pin Bottom	Pin Top	Port	Ball	1st use case	2nd use case	3rd use case
	HDMI_TD0	AUDIO_DACDAT	K1	PB28	159	160	PB29	M3	AUDIO_ADCDAT		
		AUDIO_LRCLK	M4	PB30	157	158	PB31	L1	AUDIO_LRCLK	HDMI_TF0	
				GND	155	156	GND				
	HDMI_MCK		M1	PD8	153	154	PD9	M2			
		CTS0	N2	PD10	151	152	PD11	N3	RTS0	SPI2_MISO	
		RXD0	N1	PD12	149	150	PD13	P3	TXD0	SPI2_MOSI	
		CTS1	P2	PD14	147	148	PD15	N4	RTS1	SPI2_SPCK	
		RXD1	R2	PD16	145	146	PD17	R3	TXD1	SPI2_NPCS0	
				GND	143	144	GND				
PIOBU0	Secured IO0		U3	-	141	142	-	T3		Secured IO1	PIOBU1
PIOBU2	Secured IO2		T4	-	139	140	-	U4		Secured IO3	PIOBU3
PIOBU4	Secured IO4		P6	-	137	138	-	T5		Secured IO5	PIOBU5
PIOBU6	Secured IO6		R4	-	135	136	-	U5		Secured IO7	PIOBU7
PIOBU8		RFU	R5		133	134	-	U6	RFU		PIOBU9
PIOBU10		RFU	R6	-	131	132	-	T6	RFU		PIOBU11
PIOBU12		RFU	R7	-	129	130	-	U7	RFU		PIOBU13
PIOBU14		RFU	P7	-	127	128	-	T7	RFU		PIOBU15
				GND	125	126	GND				
		SENSE0	T9	PD18	123	124	PD19	P11	SENSE1		
		SENSE2	T10	PD20	121	122	PD21	P10	SENSE3		
		SENSE4	U11	PD22	119	120	PD23	R10	SENSE5		
		SENSE6	U10	PD24	117	118	PD25	R11	SENSE7		
		SENSE8	U13	PD26	115	116	PD27	T14	SENSE9		
			R1	PD28	113	114	PD29	P1			
			N5	PD30	111	112	PD31	P5	SPI0_NPCS2	prog. CLK1	
				GND	109	110	GND				
	ISI_D8	SPI0_MISO	V4	PC0	107	108	PC1	P8	SPI0_MOSI	ISI_D9	
	ISI_D10	SPI0_SPCK	V5	PC2	105	106	PC3	R8	SPI0_NPCS0		
SD/MMC0_CK	ISI_MCK	SPI0_NPCS1	W5	PC4	103	104	PC5	T8	EBI_D0	SD/MMC0_CDA	
	SD/MMC0_DA0	EBI_D1	W6	PC6	101	102	PC7	R19	EBI_D2	SD/MMC0_DA1	
	SD/MMC0_DA2	EBI_D3	N15	PC8	99	100	PC9	U8	EBI_D4	SD/MMC0_DA3	
	SD/MMC0_DA4	EBI_D5	V6	PC10	97	98	PC11	V7	EBI_D6	SD/MMC0_DA5	
	SD/MMC0_DA6	EBI_D7	W7	PC12	95	96	PC13	V8	EBI_RD/NANDOE	SD/MMC0_DA7	
		EBI_WE/NANDWE	U9	PC14	93	94	PC15	W8	NCS3		
		NANDRDY	V9	PC16	91	92	PC17	W9	EBI_A21/NANDALE		
		EBI_A22/NANDCLE	V10	PC18	89	90	GND				
				GND	87	88	PC19	U14	ISI_D0		

3rd use case	2nd use case	1st use case	Ball	Port	Pin Bottom	Pin Top	Port	Ball	1st use case	2nd use case	3rd use case
		ISI_D1	V11	PC20	85	86	PC21	U15	ISI_D2		
		ISI_D3	T15	PC22	83	84	PC23	U16	ISI_D4		
		ISI_D5	T16	PC24	81	82	PC25	V17	ISI_D6		
		ISI_D7	R16	PC26	79	80	GNDUTMI				
				GND	77	78	/	W11	opt. VBG		
				AGND	75	76	/	V14	HHSDMA/DHSDM		
		ADC_0	U12	PC27	73	74	/	W14	HHSDPA/DHSDP		
		ADC_1	T11	PC28	71	72	GNDUTMI				
		ADC_2	R13	PC29	69	70	/	V15	HHSDMB		
		ADC_3	T12	PC30	67	68	/	W15	HHSDPB		
		ADC_4	T13	PC31	65	66	GNDUTMI				
		ADCVREF	R12	/	63	64	/	V16	HHSDMC		
				AGND	61	62	/	W16	HHSDPC		
				GND	59	60	GNDUTMI				
	EBI_A0/NBS0	PMIC_IRQ	W19	PE0	57	58	PE1	U17	FEC0_IRQ	EBI_A1	
	EBI_A2	SD/MMC0_CD	T17	PE2	55	56	PE3	P16	HDMI_IRQ	EBI_A3	
	EBI_A4	AUDIO_IRQ	U18	PE4	53	54	PE5	R17	SD/MMC1_CD	EBI_A5	
	EBI_A6	iCAN1_INT/eCAN2RX	V19	PE6	51	52	PE7	U19	iCAN2_INT/eCAN2TX	EBI_A7	
	EBI_A8		T19	PE8	49	50	PE9	T18		EBI_A9	
	EBI_A10	USB_AEN	N14	PE10	47	48	PE11	R18	USB_BEN	EBI_A11	
	EBI_A12	USB_CEN	P17	PE12	45	46	PE13	P18	USB_OCUR	EBI_A13	
	EBI_A14		N17	PE14	43	44	PE15	N18	iEMMC_RST/eDNU	EBI_A15	
				GND	41	42	GND				
	EBI_A16	i.e. Debug RS-232	M15	PE16	39	40	PE17	N19	i.e. Debug RS-232	EBI_A17	
	EBI_A18	SD/MMC1_CK	P19	PE18	37	38	PE19	N16	SD/MMC1_CDA	EBI_A19	
	EBI_A20	SD/MMC1_DA0	M14	PE20	35	36	PE21	M18	SD/MMC1_DA1	EBI_A23	
	EBI_A24	SD/MMC1_DA2	M19	PE22	33	34	PE23	L18	SD/MMC1_DA3	EBI_A25	
	EBI_NCS0#		L19	PE24	31	32	PE25	M17		EBI_NCS1#	
	EBI_NCS2#		L15	PE26	29	30	PE27	M16		EBI_WR1/BS1#	
	EBI_WAIT#		L17	PE28	27	28	PE29	V1	SOFT_MODEM_P		
		SOFT_MODEM_N	U2	PE30	25	26	PE31	L4	ADTRG	USB_VBUS	
		JTAG_SEL	V2	/	23	24	/	T1	RESET#		
		NRST_2V		/	21	22	/	V3	WAKE#		
		MRST_3V3		/	19	20	/	T2	SHDN		

3rd use case	2nd use case	1st use case	Ball	Port	Pin Bottom	Pin Top	Port	Ball	1st use case	2nd use case	3rd use case
		Vbat		/	17	18	/		WKUP		
		GND		/	15	16	/		VOUT7	VOUT7	
		GND		/	13	14	/		VOUT6	VOUT6	
		GND		/	11	12	/		VOUT5	VDDANA	
		GND		/	9	10	/		VOUT4	FUSE_2V5	
		Vin		/	7	8	/		VOUT3	VCC_3V3	
		Vin		/	5	6	/		VOUT2	1V2_HDMI	
		Vin		/	3	4	/		VOUT1	VCC_1V8	
		Vin		/	1	2	/		VDDBU_2V	VCC_2V	

Table 11: Pin Out

2.7 Interfaces

2.7.1 JTAG

The device features a number of complementary debug and test capabilities.

A common JTAG/ICE (In-Circuit Emulator) port is used for standard debugging functions, such as downloading code and single-stepping through programs.

A 2-pin debug port Serial Wire Debug (SWD). SWD replaces the 5-pin JTAG port and provides an easy and risk free alternative to JTAG as the two signals SWDIO and SWCLK are overlaid on the TMS and TCK pins, allowing for bi-modal devices that provide the other JTAG signals. These extra JTAG pins can be switched to other uses when in SWD mode.

The Debug Unit provides a two-pin UART that can be used to upload an application into internal SRAM. It manages the interrupt handling of the internal COMMTX and COMMRX signals that trace the activity of the Debug Communication Channel.

A set of dedicated debug and test input/output pins gives direct access to these capabilities from a PC-based test environment.

Characteristics_

- Cortex-A5 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
  - Serial Wire Debug
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

The JTAG interface is available with the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
JTAG_TMS/SWDIO	A7	PA0	229				
JTAG_TCK/SWCLK	A5	PA8	219				
NTRST	H6	PA16	209				
JTAG_TDI/DrxD	E1	PB24	163	164	PB25	J1	JTAG_TDO/DtxD
JTAG_SEL	V2	n.a.	23				

Table 12: JTAG Signals

For production test purposes the JTAG interface can be switched into Boundary Scan mode. Boundary Scan is enabled when JTAGSEL is high.

It is not possible to switch directly between JTAG and ICE operations. A chip reset must be performed after JTAGSEL is changed.

A Boundary-scan Descriptor Language (BSDL) file can be obtained from the Atmel website to set up a test.

Please contact ARIES Embedded to get a netlist for MA5D4.

2.7.2 External Bus Interface

MA5D4 supports a 16-bit wide External Bus Interface supporting:

- Static Memories
- NAND Flash with Multi-bit ECC

The EBI I/Os accept three drive level (LOW, MEDIUM, HIGH) allowing to avoid overshoots and give the best performances according to the bus load and external memories voltage. The slew rates are determined by programming SFR_EBICFG bit in the SFR registers.

At reset the selected drive is low. The user must make sure to program the correct drive according to the device load.

The External Bus Interface is available with the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
EBI_D8	K2	PB18	169	170	PB19	C1	EBI_D9
EBI_D10	D1	PB20	167	168	PB21	L3	EBI_D11
EBI_D12	G1	PB22	165	166	PB23	H1	EBI_D13
EBI_D14	E1	PB24	163	164	PB25	J1	EBI_D15
				104	PC5	T8	EBI_D0
EBI_D1	W6	PC6	101	102	PC7	R19	EBI_D2
EBI_D3	N15	PC8	99	100	PC9	U8	EBI_D4
EBI_D5	V6	PC10	97	98	PC11	V7	EBI_D6
EBI_D7	W7	PC12	95	96	PC13	V8	EBI_RD/NANDOE
EBI_WE/NANDWE	U9	P14	93	94	PC15	W8	NCS3
NANDRDY	V9	PC16	91	92	PC17	W9	EBI_A21/NANDALE
EBI_A22/NANDCLE	V10	PC18	89				
EBI_A0/NBS0	W19	PE0			PE1	U17	EBI_A1
EBI_A2	T17	PE2			PE3	P16	EBI_A3
EBI_A4	U18	PE4			PE5	R17	EBI_A5
EBI_A6	V19	PE6			PE7	U19	EBI_A7
EBI_A8	T19	PE8			PE9	T18	EBI_A9
EBI_A10	N14	PE10			PE11	R18	EBI_A11
EBI_A12	P17	PE12			PE13	P18	EBI_A13
EBI_A14	N17	PE14			PE15	N18	EBI_A15
EBI_A16	M15	PE16			PE17	N19	EBI_A17
EBI_A18	P19	PE18			PE19	N16	EBI_A19
EBI_A20	M14	PE20			PE21	M18	EBI_A23
EBI_A24	M19	PE22			PE23	L18	EBI_A25
EBI_NCS0#	L19	PE24			PE25	M17	EBI_NCS1#
EBI_NCS2#	L15	PE26			PE27	M16	EBI_WR1/BS1#
EBI_WAIT#	L17	PE28					

Table 13: External Bus Interface Signals

Utilization:
On MA5D4 at least the following functional blocks are driven by the External Bus Interface:

- eMMC NAND Flash (chapter 2.6.4 eMMC NAND Flash)
- NAND Flash (chapter 2.6.5 NAND Flash)

2.7.3 UART

The Universal Asynchronous Receiver Transmitter features a two-pin UART that can be used for communication and trace purposes and offers an ideal medium for in-situ programming solutions.
Moreover, the association with a DMA controller permits packet handling for these tasks with processor time reduced to a minimum.

Characteristics:

- Two-pin UART
  - Independent Receiver and Transmitter with a Common Programmable Baud Rate Generator
  - Baud rate can be driven by processor independent source clock
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Interrupt Generation
  - Support for Two DMA Channels with Connection to Receiver and Transmitter
  - Register Write Protection

The UART interfaces are available on the following pins:

Interface	Signal	Port	Pin
UART0	URXD0	PE29	28
UART0	UTXD0	PE30	25
UART1	URXD1	PC25	82
UART1	UTXD1	PC26	79

Table 14: UART Signals

2.7.4 USART

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.
The USART features three test modes: Remote loopback, Local loopback and Automatic echo.
The USART supports specific operating modes providing interfaces on RS485, and SPI buses, with ISO7816 T = 0 or T = 1 smart card slots and infrared transceivers. The hardware handshaking

feature enables an out-of-band flow control by automatic management of the pins RTS and CTS.

The USART supports the connection to the DMA Controller, which enables data transfers to the transmitter and from the receiver. The DMAC provides chained buffer management without any intervention of the processor.

Characteristics:

- Programmable Baud Rate Generator
- 5- to 9-bit Full-duplex Synchronous or Asynchronous Serial Communications
  1, 1.5 or 2 Stop Bits in Asynchronous Mode or 1 or 2 Stop Bits in Synchronous Mode
  Parity Generation and Error Detection
  Framing Error Detection, Overrun Error Detection
  Digital Filter on Receive Line
  MSB- or LSB-first
  Optional Break Generation and Detection
  By 8 or by 16 Over-sampling Receiver Frequency
  Optional Hardware Handshaking RTS-CTS
  Receiver Time-out and Transmitter Timeguard
  Optional Multidrop Mode with Address Generation and Detection
- RS485 with Driver Control Signal
- ISO7816, T = 0 or T = 1 Protocols for Interfacing with Smart Cards
  - NACK Handling, Error Counter with Repetition and Iteration Limit
- IrDA Modulation and Demodulation
  - Communication at up to 115.2 Kbps
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to f peripheral clock /6
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- Supports Connection of:
  - Two DMA Controller Channels (DMAC)
- Offers Buffer Transfer without Processor Intervention
- Register Write Protection

The USART interfaces are available on the following pins:

Interface	Signal	Port	Pin
USART0	CTS0	PD10	151
USART0	RTS0	PD11	152
USART0	RXD0	PD12	149
USART0	SCK0	PD28	113
USART0	TXD0	PD13	150
USART1	CTS1	PD14	147
USART1	RTS1	PD15	148
USART1	RXD1	PD16	146

Interface	Signal	Port	Pin
USART1	SCK1	PD29	114
USART1	TXD1	PD17	146
USART2	CTS2	PB3	188
USART2	RTS2	PB11	180
USART2	RXD2	PB4	185
USART2	SCK2	PB1	190
USART2	TXD2	PB5	186
USART3	CTS3	PE5	54
USART3	RTS3	PE24	31
USART3	RXD3	PE16	39
USART3	SCK3	PE15	44
USART3	TXD3	PE17	40
USART4	CTS4	PE0	57
USART4	RTS4	PE28	27
USART4	RXD4	PE26	29
USART4	SCK4	PE25	32
USART4	TXD4	PE27	30

Table 15: USART Signals

2.7.5 Ethernet 0

The SAMA5D4 Ethernet MAC (GMAC) module implements a 10/100 Mbps Ethernet MAC compatible with the IEEE 802.3 standard. The GMAC can operate in either half or full duplex mode at all supported speeds.

Characteristics:

- Compatible with IEEE Standard 802.3
- 10/100 Mbps operation
- Full and half duplex operation at all supported speeds of operation
- MII/RMII interface to the physical layer
- Direct memory access (DMA) interface to external memory
- Programmable burst length and endianism for DMA
- Interrupt generation to signal receive and transmit completion, or errors
- Receive and transmit IP, TCP and UDP checksum offload. Both IPv4 and IPv6 packet types supported
- Address checking logic for four specific 48-bit addresses, four type IDs, promiscuous mode, hash matching of unicast and multicast destination addresses and Wake-on-LAN
- Support for jumbo frames up to 10240 bytes
- Full duplex flow control with recognition of incoming pause frames and hardware

generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Support for 802.1Qbb priority-based flow control
- Recognition of IEEE 1588 PTP frames
- IEEE 1588 time stamp unit (TSU)
- Support for 802.1AS timing and synchronization

The Ethernet 1 interface consists of the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
		GND	191	192	GND		
FEC0_TXCK	C3	PB0	189	190	PB1	A2	FEC0_RXCK
FEC0_TXEN	B2	PB2	187	188	PB3	C2	FEC0_TXER
FEC0_CRS	J3	PB4	185	186	PB5	H2	FEC0_COL
FEC0_RXDV	G2	PB6	183	184	PB7	H3	FEC0_RXER
FEC0_RX0	F2	PB8	181	182	PB9	J2	FEC0_RX1
FEC0_RX2	F1	PB10	179	180	PB11	K4	FEC0_RX3
FEC0_TX0	D2	PB12	177	178	PB13	K3	FEC0_TX1
FEC0_TX2	A1	PB14	175	176	PB15	E2	FEC0_TX3
FEC0_MDC	B1	PB16	173	174	PB17	K5	FEC0_MDIO
		GND	171	172	GND		

Table 16: Ethernet0 Signals

2.7.6 Ethernet 1

Optionally the second Ethernet 2 is available on MA5D4. Please note that the Ethernet 2 pins are shared with the LCD-signals.
The Ethernet 2 interface consists of the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
FEC1_TXCK	E6	PA2	227	228	PA3	C6	FEC1_RXCK
FEC1_TXEN	D6	PA4	225	226	PA5	B6	FEC1_TXER
FEC1_CRS	A6	PA6	223				
				220	PA9	F4	FEC1_COL
FEC1_RXDV	F5	PA10	217	218	PA11	D5	FEC1_RXER
FEC1_RX0	G5	PA12	215	216	PA13	C5	FEC1_RX1
FEC1_TX0	E4	PA14	213	214	PA15	B5	FEC1_TX1
FEC1_RX2	G4	PA18	207	208	PA19	C4	FEC1_RX3
FEC1_TX2	A3	PA20	205	206	PA21	B4	FEC1_TX3
FEC1_MDC	B3	PA22	203	204	PA23	A4	FEC1_MDIO

Table 17: Ethernet1 Signals

2.7.7 SPI

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave mode. It also enables communication between processors if an external processor is connected to the system.

Characteristics:

- Master or Slave Serial Peripheral Bus Interface
  - 8-bit to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delay between consecutive transfers and delay before SPI clock per chip select
  - Programmable delay between chip selects
  - Selectable mode fault detection
- Master Mode can drive SPCK up to Peripheral Clock
- Master Mode Bit Rate can be Independent of the Processor/Peripheral Clock
- Slave mode operates on SPCK, asynchronously with core and bus clock
- Four chip selects with external decoder support allow communication with up to 15 peripherals
- Communication with Serial External Devices Supported
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD controllers, CAN controllers and sensors
  - External coprocessors
- Connection to DMA Channel Capabilities, Optimizing Data Transfers
  - One channel for the receiver
  - One channel for the transmitter
- Register Write Protection

The SPI interfaces are available on the following signals:

SPI0

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
				112	PD31	P5	SPI0_NPCS2
SPI0_MISO	V4	PC0	107	108	PC1	P8	SPI0_MOSI
SPI0_SPCK	V5	PC2	105	106	PC3	R8	SPI0_NPCS0
SPI0_NPCS1	W5	PC4	103				

Table 18: SPI0 Signals

SPI1

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
SPI1_MISO	K2	PB18	169	170	PB19	C1	SPI1_MOSI
SPI1_SPCK	D1	PB20	167	168	PB21	L3	SPI1_NPCS0
SPI1_NPCS1	G1	PB22	165	166	PB23	H1	SPI1_NPCS2

Table 19: SPI1 Signals

SPI2

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
					PD11	N3	SPI2_MISO
					PD13	P3	SPI2_MOSI
					PD15	N4	SPI2_SPCK
					PD17	R3	SPI2_NPCS0

Table 20: SPI2 Signals

Utilization:

On MA5D4 at least the following functional blocks are connected to the SPI Interfaces:

- SPI0: SPI Boot Flash (chapter 2.6.3 SPI Boot Flash)
- SPI1: CAN (chapter 2.6.6 CAN)

2.7.8 Two Wire Interface

The Atmel Two-wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format. It can be used with any Atmel Two-wire Interface bus Serial EEPROM and I2C compatible device such as a Real Time Clock (RTC), Dot Matrix/Graphic LCD Controllers and temperature sensor. The TWI is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported.

Arbitration of the bus is performed internally and puts the TWI in slave mode automatically if the bus arbitration is lost.

A configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

Characteristics:

- Compatible with Atmel Two-wire Interface Serial Memory and I2C Compatible Devices (1)
- One, Two or Three Bytes for Slave Address
- Sequential Read/Write Operations
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbit/s
- General Call Supported in Slave Mode
- Connection to DMA Controller (DMA) Channel Capabilities Optimizes Data Transfers
- Register Write Protection

Signal Description:

- TWD: Two-wire Serial Data
- TWCK: Two-wire Serial Clock

The Two Wire interfaces are available on the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
TWD0	D3	PA30	193	194	PA31	J4	TWCK0
				160	PB29	M3	TWD2
TWCK2	M4	PB30	157				
				82	PC25	V17	TWD3
TWCK3	R16	PC26	79				
				28	PE29	V1	TWD1
TWCK1	U2	PE30	25				

Table 21: Two Wire Interfaces Signals

Utilization:

On MA5D4 at least the following functional blocks are connected to the Two Wire Interface:

- TWDO PMIC (2.6.7 PMIC)

2.7.9 CAN

For more information on the implementation of the CAN interfaces please refer to chapter '2.6.6 CAN'

The CAN interfaces are available on the following pins:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
eCAN1_RX			165	166			eCAN1_TX
eCAN2RX			51	52			eCAN2TX

Table 22: CAN Interface Signals

2.7.10 LCD

The LCD Controller (LCDC) consists of logic for transferring LCD image data from an external display buffer to an LCD module. The LCD has one display input buffer per overlay that fetches pixels through the dual AHB master interface and a lookup table to allow palletized display configurations. The LCD controller is programmable on a per overlay basis, and supports different LCD resolutions, window sizes, image formats and pixel depths.

The LCD is connected to the ARM Advanced High Performance Bus (AHB) as a master for reading pixel data. It also integrates an APB interface to configure its registers.

The LCD interface consists of the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
LCD_Data0	A7	PA0	229	230	PA1	F6	LCD_Data1
LCD_Data2	E6	PA2	227	228	PA3	C6	LCD_Data3
LCD_Data4	D6	PA4	225	226	PA5	B6	LCD_Data5
LCD_Data6	A6	PA6	223	224	PA7	E5	LCD_Data7
		G N D	221	222	G N D		
LCD_Data8	A5	PA8	219	220	PA9	F4	LCD_Data9
LCD_Data10	F5	PA10	217	218	PA11	D5	LCD_Data11
LCD_Data12	G5	PA12	215	216	PA13	C5	LCD_Data13
LCD_Data14	E4	PA14	213	214	PA15	B5	LCD_Data15
		G N D	211	212	G N D		
LCD_Data16	H6	PA16	209	210	PA17	D4	LCD_Data17
LCD_Data18	G4	PA18	207	208	PA19	C4	LCD_Data19
LCD_Data20	A3	PA20	205	206	PA21	B4	LCD_Data21
LCD_Data22	B3	PA22	203	204	PA23	A4	LCD_Data23
		G N D	201	202	G N D		
LCD_PWM	H5	PA24	199	200	PA25	F3	LCD_DISP
LCD_VSYNC	E3	PA26	197	198	PA27	H4	LCD_HSYNC
LCD_PCK	G3	PA28	195	196	PA29	J5	LCD_DEN

Table 23: LCD Signals

2.7.11 Image Sensor Interface ISI

The Image Sensor Interface (ISI) connects a CMOS-type image sensor to the processor and provides image capture in various formats.The ISI performs data conversion, if necessary, before the storage in memory through DMA.

The ISI supports color CMOS image sensor and grayscale image sensors with a reduced set of functionalities. In grayscale mode, the data stream is stored in memory without any processing and so is not compatible with the LCD controller.

Characteristics:

- ITU-R BT. 601/656 8-bit Mode External Interface Support
- Supports up to 12-bit Grayscale CMOS Sensors
- Support for ITU-R BT.656-4 SAV and EAV Synchronization
- Vertical and Horizontal Resolutions up to 2048 × 2048
- Preview Path

  - Up to 2048 × 2048 in Grayscale Mode
  - Up to 640 × 480 in RGB Mode
- 32 Bytes FIFO on Codec Path
- 32 Bytes FIFO on Preview Path
- Support for Packed Data Formatting for YCbCr 4:2:2 Formats
- Preview Scaler to Generate Smaller Size image
- Programmable Frame Capture Rate
- VGA, QVGA, CIF, QCIF Formats Supported for LCD Preview
- Custom Formats with Horizontal and Vertical Preview Size as Multiples of 16 Also Supported for LCD Preview

The ISI interface consists of the following signals:

Signal	Ball	Port	Pin Bottom	Pin Top	Port	Ball	Signal
ISI_SDA	D3	PA30	193	194	PA31	J4	ISI_SCL
				188	PB3	C2	ISI_VSYNC
ISI_HSYNC	J3	PB4	185	186	PB5	H2	ISI_PWD
				180	PB11	K4	ISI_RST
ISI_D8	V4	PC0	107	108	PC1	P8	ISI_D9
ISI_D10	V5	PC2	105	106	PC3	R8	ISI_D11
ISI_MCK	W5	PC4	103				
				88	PC19	U14	ISI_D0
ISI_D1	V11	PC20	85	86	PC21	U15	ISI_D2
ISI_D3	T15	PC22	83	84	PC23	U16	ISI_D4
ISI_D5	T16	PC24	81	82	PC25	U17	ISI_D6
ISI_D7	R16	PC26	79				

Table 24: ISI Signals