M53 Hardware Manual

Release 1

ARIES Embedded GmbH

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

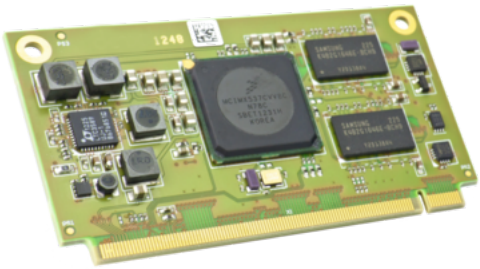
Revision	Date	Revised	Comment
1.0	23.11.2012	aw	Initial creation
1.1	11.07.2016	aw	Transition to pdf documentation Inserted ‘Care and Maintenance’

CHAPTER

TWO

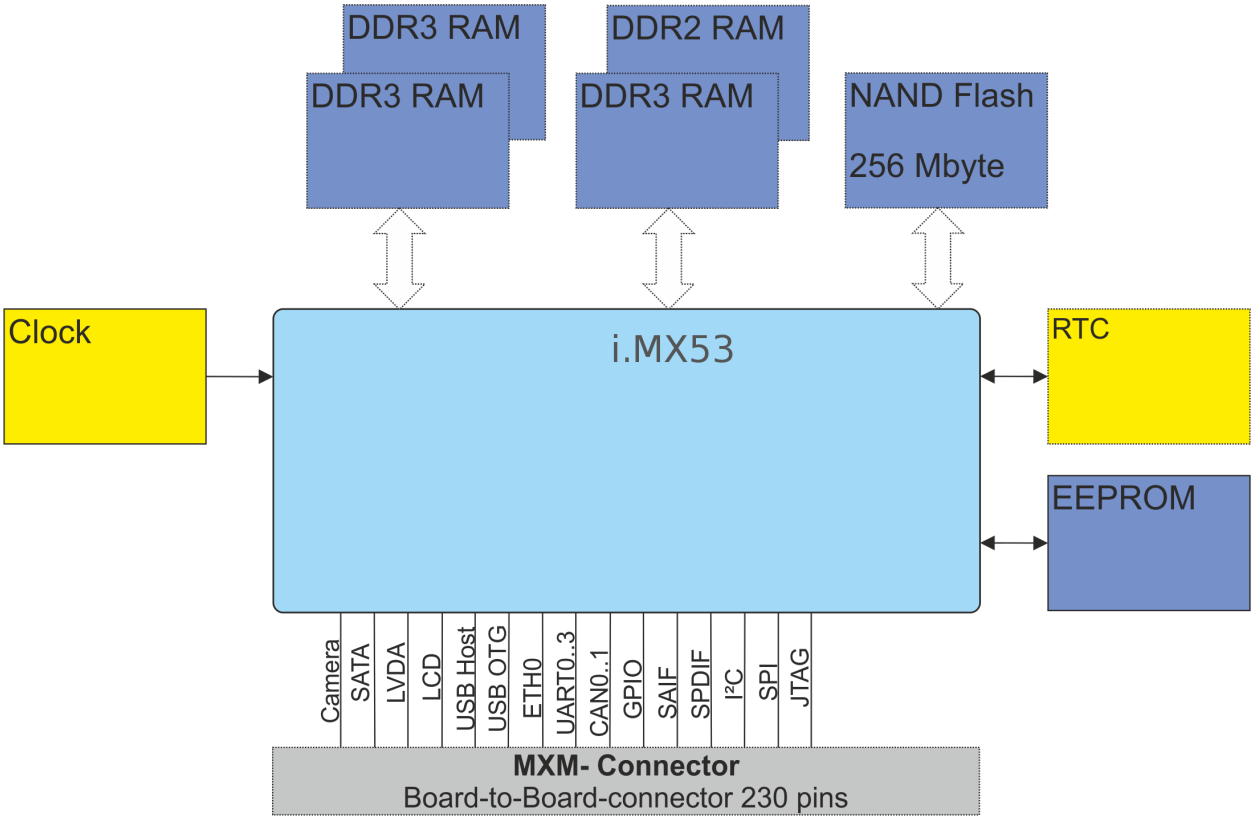
OVERVIEW

Being the second member of the “M” System On Module family the M53 offers the powerful CortexA8 CPU i.MX53 .



The i.MX53 family of processors represents Freescale’s next generation of advanced multimedia and power-efficient implementation of the ARM Cortex™-A8 core with core processing speeds up to 1.2 GHz. It is optimized for both performance and power to meet the demands of high-end, advanced applications. Ideal for a broad range of applications in the consumer, automotive, medical and industrial markets, the i.MX53 includes an integrated display controller, full HD capability, enhanced graphics and connectivity features.

2.1 Block Diagram

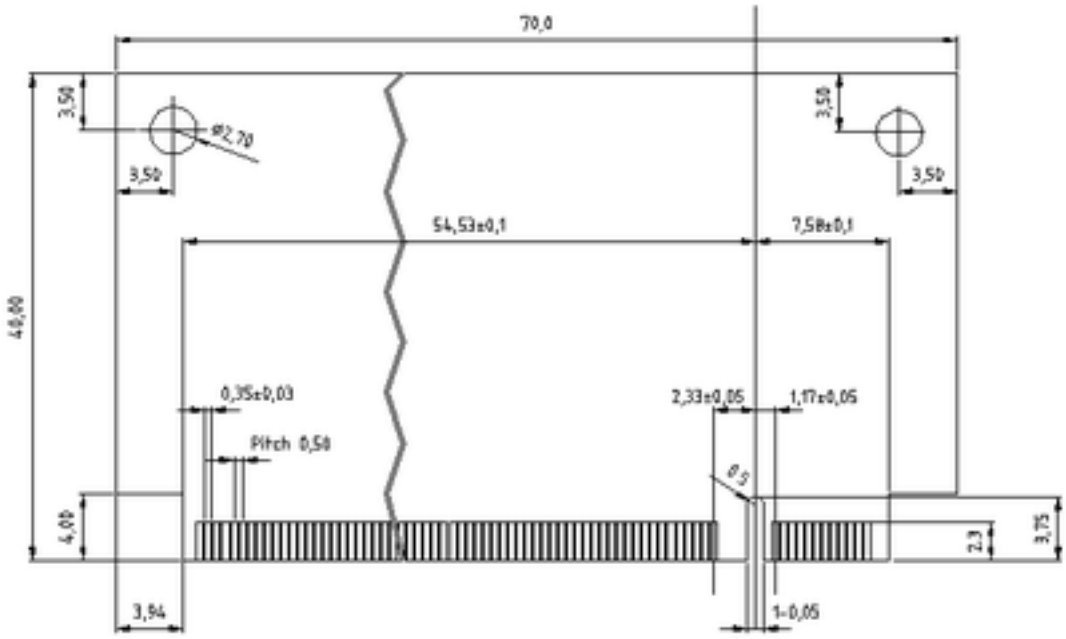


2.2 Feature Set

- **i.MX53 CPU**
  - i.MX535, 1,2GHz speed for temperature range -20°C...+85°C
  - i.MX537, 800MHz speed for temperature range -40°C...+85°C
- 1GByte DDR3 DRAM on the standard versions, ask DENX Computer Systems for the 512MB/2GB options
- 256 MB NAND Flash, extendable up to 16GByte
- **LCD Controller supporting**
  - 1 TFT supporting max. 1920x1080 pixel FullHD resolution with Touchscreen support
  - 2 LVDS Displays
- Camera interface 20 Bit parallel
- 1 x 10/100MBit Ethernet interface, IEEE1588 support
- up to 2 x CAN interfaces
- up to 2 x USB2.0 interfaces, one optionally as OTG/Device
- up to 5 x UART interfaces
- up to 3 x I²C interfaces

- up to 3 x SPI interfaces up
- to 2 x SDIO interfaces
- SATA Audio interface
- TV out
- size 70 x 40mm
- 230 Pins edge connector „MXM“

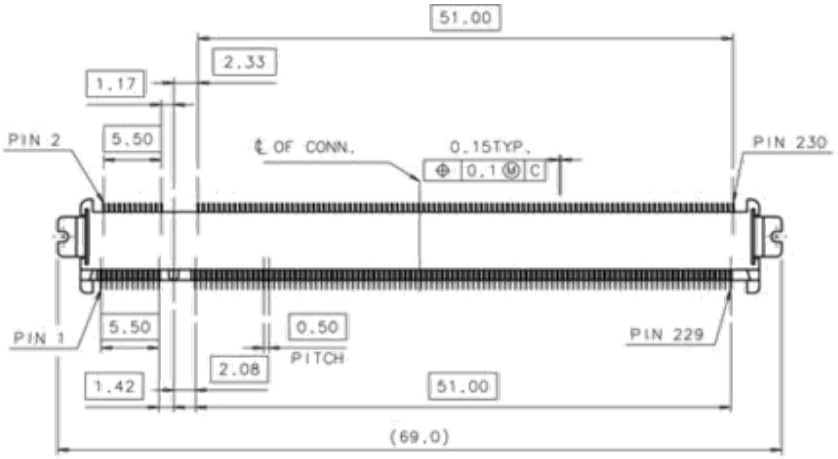
2.3 Dimensions

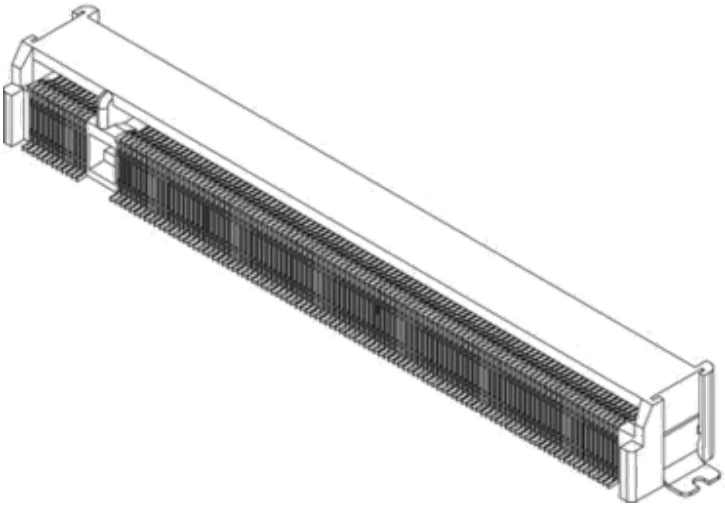


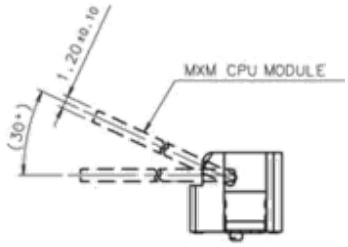
2.4 MXM Connector

M53 supplies its signals on an edge connector which complies to the popular MXM standard which is also used in a large number of “X86” embedded SOMs based on the QSeven Specification. Being a small sized and highly integrated System On Module that can be used in a design application much like an integrated circuit component it uses a 230 pin MXM2 SMT edge connector to connect all power and signal lanes to the carrier board. This connector is available from multiple vendors at different heights (5.5 mm and 7.8 mm).

! The M53 pinout does not comply with the QSeven specification !



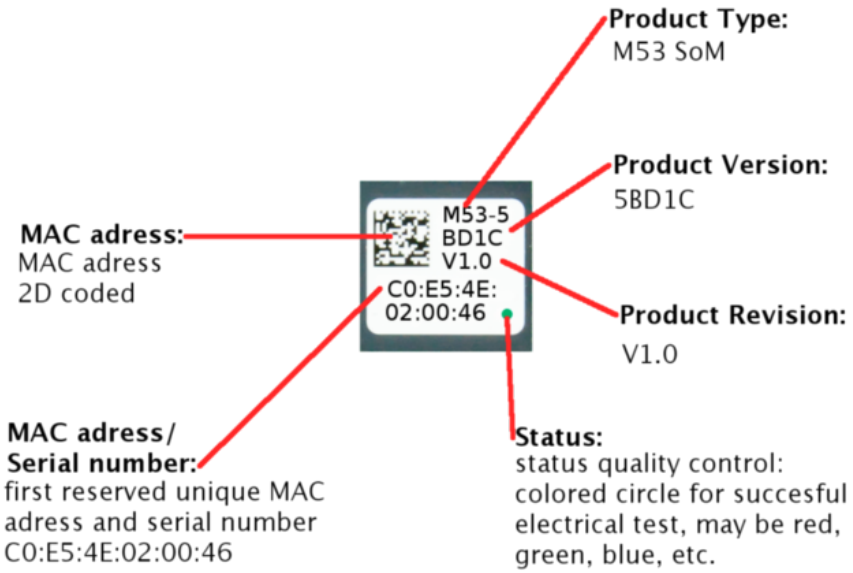




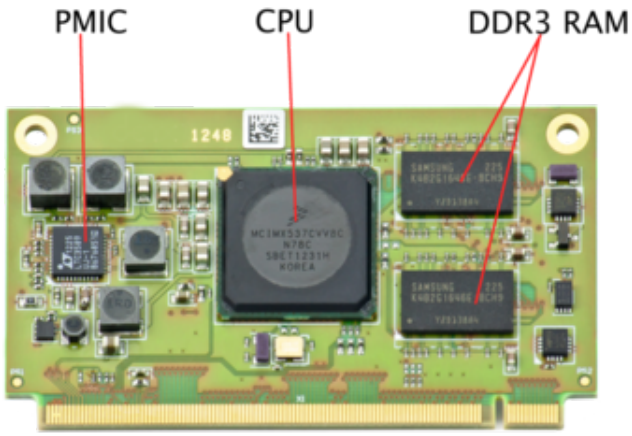
M53 provides

- 230 pins with asymetric segmentation(24 + 206 pins). The contact to contact distance is 0,508mm.
- a PCB thickness of 1,2 $\pm$ 0,1m
- **a standard distance to the baseboard of**
  - 2,7mm. In this case under the M53 module no components shall be populated on the baseboard
  - 5,0mm. In this case under the M53 module components with a maximum height of 2,2mm shall be populated on the baseboard
- a maximum height of components on the top side of 5,5mm.
- Interlocking of the M53 module on the baseboard using 2 x M2,5 screws.

2.5 Part Label



2.6 Part Locations



CHAPTER

THREE

RESOURCES

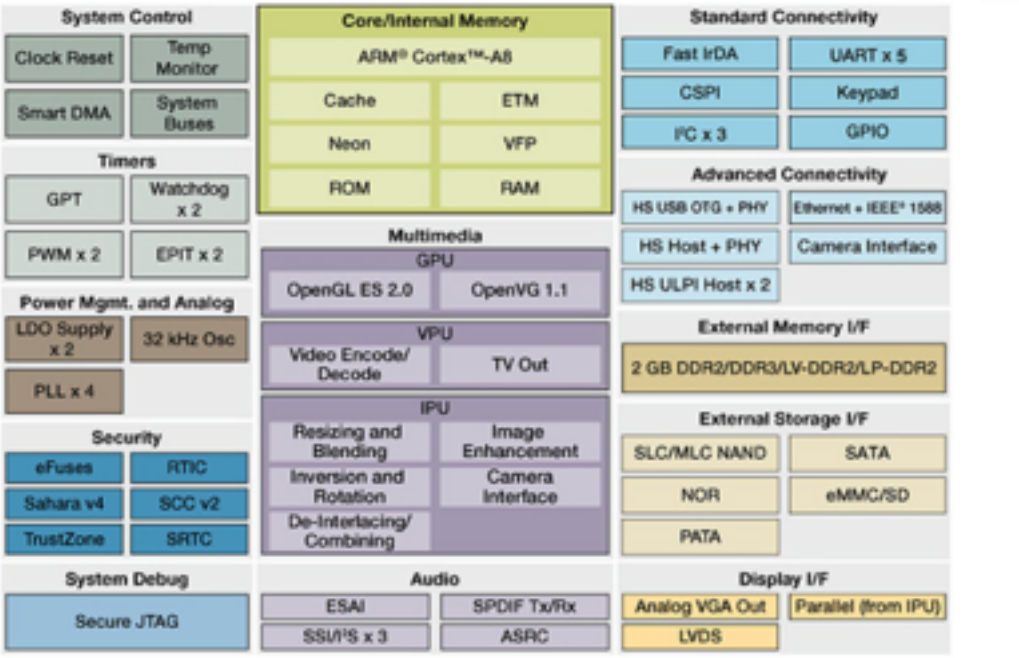
M53 offers multiple interfaces and functions that can used. Not all possibilities can be displayed in this documentation.

For more information on available signals please refer to the Pin Out section and also to the file with possible multiplexing options. Also we recomment to use the I/O-Multiplexing Tool which can be found on the Freescale website.

3.1 Components

3.1.1 CPU

The i.MX53 family of processors represents Freescale's next generation of advanced multimedia and power-efficient implementation of the ARM Cortex™-A8 core. With core processing speeds up to 1 GHz, the i.MX535 is optimized for both performance and power to meet the demands of high-end, advanced applications requiring mobility and a long battery life. 1080p HD video decode and 720p video encode, two dedicated graphics cores, multiple display and connectivity options, and high level of integration make the i.MX535 a choice platform for smart mobile devices.



The i.MX535 features

- 1 GHz ARM Cortex-A8 CPU
- 32 KB instruction and data caches
- Unified 256 KB L2 cache
- NEON SIMD media accelerator
- Vector floating point coprocessor
- Independent OpenGL® ES 2.0 and OpenVG™ 1.1 hardware accelerators
- Multi-format HD 1080p video decoder and HD 720p video encoder hardware engine
- Dual display capable with multiple display options including TFT LCD, LVDS, analog TV-formats (composite, component, RGB) and standard VGA
- Hardware accelerated image post-processing, display quality enhancement, and video and graphics combining
- Two simultaneous camera inputs with hardware pre-processing
- Up to 2 GB LP-DDR2, LV-DDR2, DDR2-800, and DDR3-800 SDRAM, 16/32-bit
- Managed NAND Flash Support with eMMC 4.4/SDIO
- Raw NAND with up to 16-bit ECC
- Multiple independent power domains
- Dynamic voltage and frequency scaling
- High-Speed USB 2.0 OTG with PHY
- High-Speed USB 2.0 Host with PHY
- Two additional High-Speed USB 2.0 controllers (ULPI)
- Integrated LVDS display interface supporting up to 2 channels each with 4 data pairs and 1 clock pair
- Wide array of serial interfaces, including SDIO, SPI, I2C and UART
- I2S and S/PDIF audio interfaces
- 10/100 Ethernet controller
- SATA controller and PHY up to 1.5Gbps
- Advanced security supporting High Assurance Boot, cryptographic cipher engines, random number generator, and tamper detection

More information on the i.MX535 CPU is available under

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=i.MX535&nodeId=018rH3ZrDR988D

3.1.2 RAM

M53 supports four K4B2G1646E-BIH9000 (Samsung) DDR3 SDRAM chips on two banks when equipped in the 1,0GB version and two K4B2G1646E-BIH9000 DDR3 SDRAM chips when equipped in the 512MB version.

The DDR3 SDRAM is connected 32 bit wide to the i.MX53 RAM controller. DRAM_CS0 and DRAM_CS1 signals are used to select them.

The 2Gb DDR3 SDRAM is organized as a 16MBit x 16 x 8 banks device. The synchronous device achieves high speed double- data-rate transfer rates of up to2133 Mb/sec/pin (DDR3-2133) for general applications.

- JEDEC standard VDD = 1.5V $\pm$ 0.075V Power Supply• VDDQ = 1.5V $\pm$ 0.075V device. This synchronous device achieves high speed double-data-rate

- 400 MHz fCK for 800Mb/sec/pin
- 533MHz fCK for 1066Mb/sec/pin
- 667MHz fCK for 1333Mb/sec/pin
- 800MHz fCK for 1600Mb/sec/pin
- 933MHz fCK for 1866Mb/sec/pin
- 1066MHz fCK for 2133Mb/sec/pin
- 8 Banks
- Programmable CAS Latency(posted CAS): 5,6,7,8,9,10,11,13,14
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600), 9(DDR3-1866) and 10(DDR3-2133)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm $\pm$ 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Support Industrial Temp (-40 ... +95°C)
- Asynchronous Reset

More information on the K4B2G1646E-BIH9000 DDR3 SDRAM chips is available under

http://www.samsung.com/global/business/semiconductor/product/consumer-dram/detail?productId=7709&iaId=739

3.1.3 Flash

M53 supports 256MB of NAND Flash which is populated as MT29F2G08ABAEAWP-IT:E (Micron) .

The NAND Flash is connected 8 bit wide to the i.MX53 NAND Flash controller PATA_DATA[0]....PATA_DATA[7]. The NANDF_CS0 signal is used to select it.

The MT29F2G and device contains 2,048 erasable blocks, respectively. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes (x8) . The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area on the x8 device; and on the x16 device, separate 1,024-word and 32-word areas. The 64-byte and 32-word areas are typically used for error management functions.

The contents of each 2,112-byte page can be programmed in 300μs, and an entire 132K- byte/66K-word block can be erased in 2ms. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 100,000 cycles when appropriate error correction code (ECC) and error management are used.

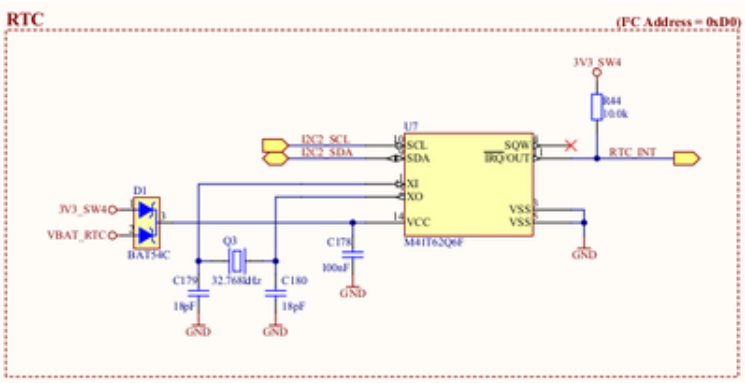
- **Organization**
  - Page size x8: 2,112 bytes (2,048 + 64 bytes)
  - Page size x16: 1,056 words (1,024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)

  - Device size: 2Gb: 2,048 blocks; 4Gb: 4,096 blocks; 8Gb: 8,192 blocks

- **READ performance**
  - Random READ: 25μs
  - Sequential READ: 30ns (3V x8 only)
- **WRITE performance**
  - PROGRAM PAGE: 300μs (TYP)
  - BLOCK ERASE: 2ms (TYP)
- Endurance: 100,000 PROGRAM/ERASE cycles
- First block (block address 00h) guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles)
- VCC: 1.70V–1.95V1 or 2.7V–3.6V
- Automated PROGRAM and ERASE

3.1.4 RTC

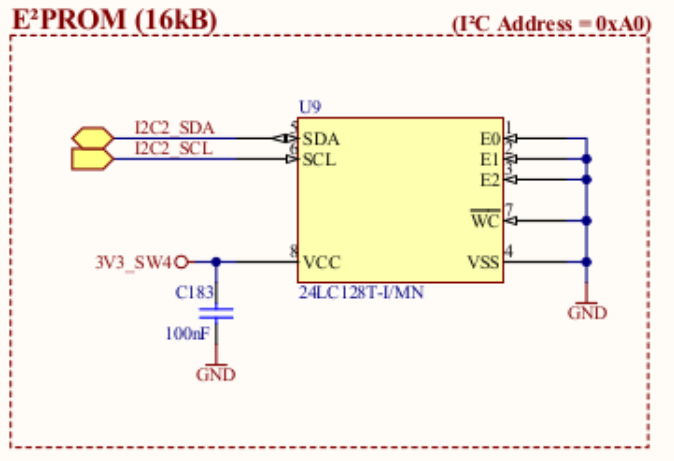
M53 supports a M41T62 RTC which his connected to the I2C2 interface, adress 0xD0.



- RTC-type: M41T62
- 350 nA timekeeping current at 3 V
- Low operating current of 35 μA (at 400 kHz)

3.1.5 EEPROM

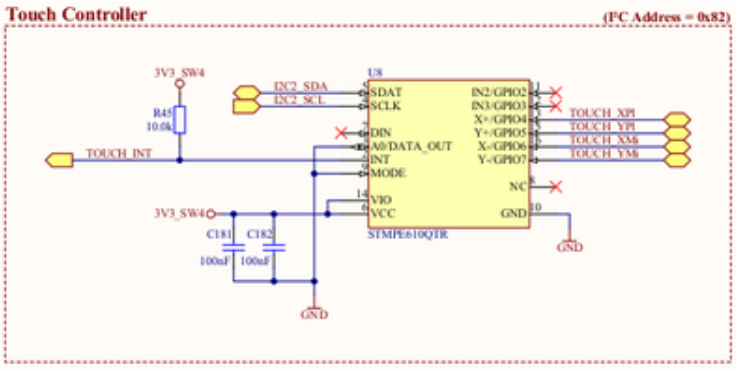
M53 offers a 128kBit EEPROM M28124 on interface I2C2 which could be used to store application or system data.



The EEPROM is connected to the I2C2 interface, adress 0xA0.

3.1.6 Touchscreen

The Touch Screen Controller STMPE610QTR is connected to the I2C2 interface.



3.2 Interfaces

3.2.1 Ethernet

M53 supplies one 10/100 MBit Ethernet interfaces at the following pins:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	1	2	GND	
F10	FEC_TXD0	3	4	FEX_RXD0	C11
D10	FEC_TXD1	5	6	FEX_RXD1	E11
D5	FEC_TXD2	7	8	FEX_RXD2	C4
B4	FEC_TXD3	9	10	FEX_RXD3	C5
C10	FEC_TX_EN	11	12	FEC_RX_DV	D11
B3	FEC_TX_ER	13	14	FEC_RX_ER	F12
D12	FEC_MDIO	15	16	FEC_COL	D6
E10	FEC_MDC	17	18	FEC_CRS	F6
	GND	19	20	GND	
E12	FEC_TX_CLK	21	22	FEC_RX_CLK	E7
	GND	23	24	GND	

The Fast Ethernet controller (FEC) is designed to support both 10- and 100-Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard physical interfaces (MAC-PHY) for connection to an external Ethernet transceiver.

The FEC incorporates the following features:

- **Support for three different Ethernet physical interfaces:**
  - 10-Mbps and 100-Mbps IEEE Std. 802.3 MII
  - 10-Mbps and 100-Mbps RMII
  - 10-Mbps 7-wire interface (industry standard)
- IEEE 802.3 full-duplex flow control
- Support for full-duplex operation (200Mbps throughput) with a minimum system clock rate of 50 MHz
- Support for half-duplex operation (100Mbps throughput) with a minimum system clock rate of 25 MHz

3.2.2 JTAG

M53 provides a JTAG interface:

	GND	201	202	GND	
E9	JTAG_TRST(2)	203	204	JTAG_nSRST	A21
A8	JTAG_TMS(2)	205	206		
B8	JTAG_TDI(2)	207	208		
A7	JTAG_TDO	209	210		
D9	JTAG_TCK (1)	211	212		
C9	JTAG_MODE(1)	213	214		

1. = Pins are connected via pull down resistor 10kΩ to GND
2. = Pins are connected via pull up resistor 10kΩ to 2,8V

3.2.3 Serial Interfaces

UART

On M53 the UART block provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. The UART module supports NRZ encoding format and IrDA-compatible infrared slow data rate (SIR) format.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 4.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 7 or 8 data bits
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Edge-selectable RTS and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- DCE/DTE capability
- RTS, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE), RI (DTE only), DCD (DTE only), DTR (DCE only) and DSR (DTE only) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate.

The following pins are available on M53 for UART:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
J2	UART1_RXD	163	164	UART1_RTS	K1
J3	UART1_TXD	165	166	UART1_CTS	K2
K4	UART2_RXD	167	168	UART2_RTS	K3
J1	UART2_TXD	169	170	UART2_CTS	K5
L2	UART3_RXD	171	172	UART3_RTS	L4
L5	UART3_TXD	173	174	UART3_CTS	L3

CAN

The Flexible Controller Area Network (FLEXCAN) block on M53 is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. It includes two embedded memories, one for storing Message Buffers and another one for storing Rx Individual Mask Registers. Support for 64 Message Buffers is provided.

The CAN protocol was designed primarily to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN block is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. Sixty-four Message Buffers are supported. The Message Buffers are stored in an embedded RAM dedicated to the FLEXCAN. The CAN Protocol Interface (CPI) sub-block manages the serial communication on the CAN bus, requesting RAM access for receiving and transmitting message frames, validating received messages and performing error handling. The Message Buffer Management (MBM) sub-block handles Message Buffer selection for reception and transmission, taking care of arbitration and ID matching algorithms. The Bus Interface Unit (BIU) sub-block controls the access to and from the internal interface bus, in order to establish connection to the ARM and to other blocks. Clocks, address and data buses, interrupt outputs and test signals are accessed through the Bus Interface Unit.

The FLEXCAN includes these distinctive features:

- **Full Implementation of the CAN protocol specification**
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mb/sec
  - Content-related addressing
- Flexible Message Buffers of zero to eight bytes data length
- Each Message Buffer configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Includes 1056 bytes (64 Mbytes) of RAM used for Message Buffer storage
- Includes 256 bytes (64 Mbytes) of RAM used for individual Rx Mask Registers
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous CAN version
- Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
- Unused message buffer and Rx Mask Register space can be used as general purpose RAM space
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Configurable Glitch filter width to filter the noise on CAN bus when waking up

The FlexCAN interfaces are available on the following pins of M53:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
B5	CAN1_RXD	159	160	CAN2_RXD	E6
A4	CAN1_TXD	161	162	CAN2_TXD	E5

USB

M53 supplies

- one USB Host interface (Host1)
- one USB Host/OTG interface

The i.MX53 USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification, and the OTG supplement. It consists of four independent USB controller cores: one OTG controller core, and three Host-only controller cores. Each controller core can support ULPI, Serial, UTMI, IC-USB or HSIC interface according to its feature.

All four controller cores are single-port cores. The OTG core is used as both a downstream and upstream port.

The USB includes the following features:

- **High-speed/full-speed/low-speed host only core (Host1)**
  - HS/FS/LS UTMI compliant interface
- **High-speed/full-speed/low-speed host only core (Host2)**
  - HS/FS/LS ULPI compliant interface
  - Software configurable for full speed/low speed interface for Serial transceiver
  - Full Speed Inter-Chip USB compliant interface (IC-USB)
- **High-speed/full-speed/low-speed Host-only core (Host3)**
  - HS/FS/LS ULPI compliant interface
  - Software configurable for full-speed/low-speed interface for Serial transceiver
- **High-speed/full-speed/low-speed OTG core**
  - HS/FS/LS UTMI compliant interface
  - High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
  - High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
  - Hardware support for OTG signaling, session request protocol, and host negotiation protocol
  - Up to 8 bidirectional endpoints
- Low-power mode with local and remote wake-up capability
- Serial PHY interfaces configurable for bidirectional/unidirectional and differential/single ended
- Embedded DMA controller

The following USB pins are available on M53:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
B19	USB_OTG_D+	181	182	GPIO2_31	Y4
A19	USB_OTG_D-	183	184	USB_HOST_D+	A17
E15	USB_OTG_VBUS	185	186	USB_HOST_D-	B17
C16	USB_OTG_ID	187	188	USB_HOST_VBUS	D15
D8	USB_OTG_PWRON	189	190	USB_HOST_PWRON	C7
D7	USB_OTG_OC	191	192	USB_HOST_OC	A6

SPI

The Configurable Serial Peripheral Interface (CSPI) block is a full-duplex, synchronous, four-wire serial communication block. The CSPI block contains an 8 x 32 receive buffer (RXFIFO) and an 8 x 32 transmit buffer (TXFIFO). With data FIFOs, the CSPI allows rapid data communication with fewer software interrupts.

The Key features of the CSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 8 -entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to one-quarter of the reference clock frequency.

CSPI has two operating modes, master mode and slave mode.

- Master Mode: When the CSPI is configured as a master, it uses a serial link to transfer data between the CSPI and an external slave device. One of the Chip Select (SS) signals and the clock signal (SCLK) are used to transfer data between two devices. If the external device is a transmit-only device, the CSPI master's output port can be ignored and used for other purposes. In order to use the internal TXFIFO and RXFIFO, two auxiliary output signals, Chip Select (SS) and SPI_RDY, are used for data transfer rate control. Software can also configure the sample period control register to a fixed data transfer rate.
- Slave Mode: When the CSPI is configured as a slave, software can configure the CSPI Control register to match the external SPI master's timing. In this configuration, Chip Select (SS) becomes an input signal, and is used to control data transfers through the Shift register, as well as to load/store the data FIFO.

The following SPI pins are available on M53:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
V8	eCSPI2_MISO	149	150	eCSPI2_SS0	AB4
Y7	eCSPI2_MOSI	151	152	eCSPI2_SS1	AA6
W8	eCSPI2_SCLK	153	154	eCSPI2_SS2	Y2
		155	156	eCSPI2_SS3	W3

I2C

The I2C interface on M53 provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard Philips I2C bus protocol.

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a

short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development. The I2C interface operates up to 400 kbps, but it depends on the pin loading and timing characteristics.

The I2C has the following key features:

- Compatibility with I2C bus standard
- Multiple-master operation
- Software-programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

The I2C primarily operates in two different functional modes:

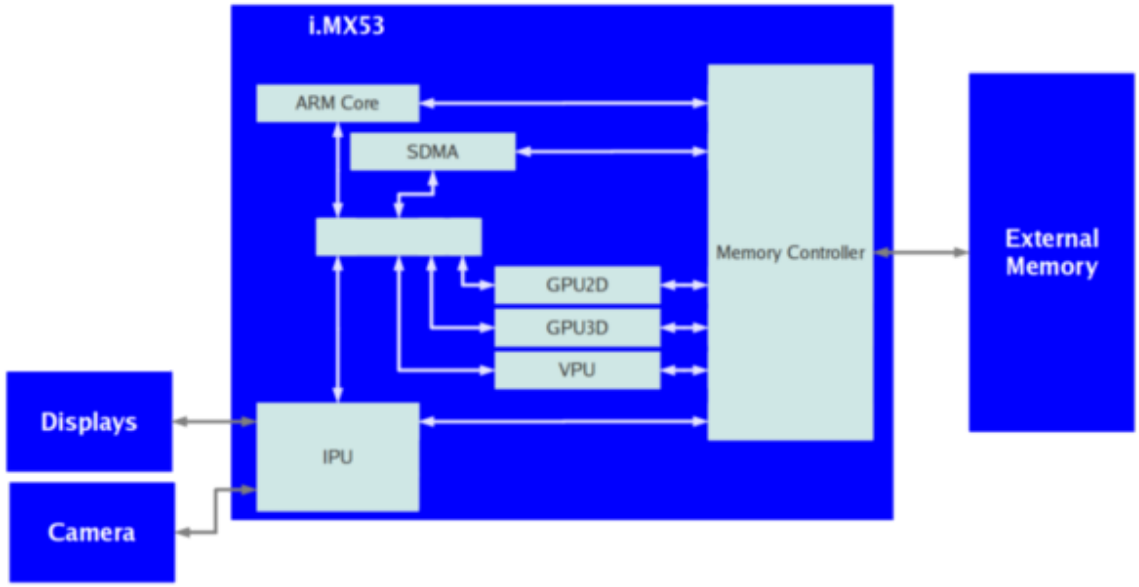
- Standard Mode: In Standard mode, I2C supports the data transfer rates up to 100 Kbits/s.
- Fast Mode: In Fast Mode, data transfer rates up to 400 Kbits/s can be achieved. As per block operation, there is no special configuration required for Fast and Standard mode. It is the data transfer rate which distinguishes Standard and Fast mode.

The following I2C pins are externally available:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
Y3	I²C1_SCL	145	146	I²C3_SCL	A5
U6	I²C1_SDA	147	148	I²C3_SDA	B6

3.2.4 Multimedia Interfaces

The video-graphics sub-system includes the following blocks:



- Video Processing Unit (VPU): a multi-standard video/image codec
- Two Graphics Processing Units (GPUs): one for accelerating 3D graphics (OpenGL/ES), and one for accelerating vector graphics (OpenVG and 2D graphics BitBLT)
- Image Processing Unit (IPU): providing connectivity to cameras and displays, related processing, synchronization and control
- **Display interface bridges: providing optional translation from the digital display interface supported by the IPU to other**
  - TV Encoder (TVE) bridge: composite, S-video, component and VGA interfaces
  - LVDS bridge: up to two LVDS interfaces

Displays

- Two parallel - driven directly by the IPU
- One analog (TV-out or VGA) - driven by the TVE
- Two LVDS channels, driven by the LVDS bridge

IPU has 2 display ports, so only up to two external ports can be active at any given time. (Additional asynchronous data flows can be sent though the parallel ports.)

- IPU has 2 camera ports, used to connect to relevant external devices.
- The IPU, VPU and the GPUs have a master AXI port, providing access to system memory.
- **The blocks are controlled by the ARM Cortex A8TM Platform (ARM) or the Smart Direct Memory Access (SDMA) as fo**
  - The LVDS bridge is controlled by signals connected to top-level registers
  - All other blocks have host interfaces. The VPU and TVE blocks use slave IP ports and the GPU and IPU blocks use slave AHB ports.

- The slave AHB port of the GPUs also allows a direct access of the host to the GPUs internal memory, for the transfer of graphics commands, for example.
- The slave AHB port of the IPU also provides a direct access of the host to an external display controller, connected to the parallel display port.
- There is an interface between the IPU and the GPUs, allowing direct synchronization between them, to transfer graphics data from the GPUs to the IPU (through system memory) while avoiding tearing.

  M53 offers display capabilities as follows:

1. Parallel interface

The parallel display interface offers a 24 Bit TTL LCD interface on the following pins:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	53	54	GND	
W10	DISP1_DAT0	55	56	DISP1_DAT16	AA4
AA8	DISP1_DAT1	57	58	DISP1_DAT17	AA3
AC5	DISP1_DAT2	59	60	DISP1_DAT18	V6
Y9	DISP1_DAT3	61	62	DISP1_DAT19	Y5
V9	DISP1_DAT4	63	64	DISP1_DAT20	W5
AB6	DISP1_DAT5	65	66	DISP1_DAT21	W4
W9	DISP1_DAT6	67	68	DISP1_DAT22	V5
AA7	DISP1_DAT7	69	70	DISP1_DAT23	V4
	GND	71	72	GND	
AC4	DISP1_DAT8	73	74	DI1_PIN1	AA9
Y8	DISP1_DAT9	75	76	DI1_PIN2	AC6
AB5	DISP1_DAT10	77	78	DI1_PIN3	V10
AC3	DISP1_DAT11	79	80	DI1_PIN12	W6
V7	DISP1_DAT12	81	82	DI1_PIN15	AB7
AB3	DISP1_DAT13	83	84	DI1_D0_CS	AC7
W7	DISP1_DAT14	85	86	DI1_D1_CS	Y10
Y6	DISP1_DAT15	87	88	DI1_DISP_CLK	AA5
	GND	89	90	GND	

2. LVDS0 and LVDS1

Two LVDS channels, driven by the LVDS bridge, are available on the following pins of M53:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	23	24	GND	
Y17	LVDS0_TX0_N	25	26	LVDS0_TX1_N	AB17
AA17	LVDS0_TX0_P	27	28	LVDS0_TX1_P	AC17
	GND	29	30	GND	
Y16	LVDS0_TX2_N	31	32	LVDS0_TX3_N	AB15
AA16	LVDS0_TX2_P	33	34	LVDS0_TX3_P	AC15
	GND 35	36	GND		
AB16	LVDS0_CLK_N	37	38	LVDS1_CLK_N	AA13
AC16	LVDS0_CLK_P	39	40	LVDS1_CLK_P	Y13
	GND	41	42	GND	
AC14	LVDS1_TX0_N	43	44	LVDS1_TX1_N	AC13
AB14	LVDS1_TX0_P	45	46	LVDS1_TX1_P	AB13
	GND	47	48	GND	
AC12	LVDS1_TX2_N	49	50	LVDS1_TX3_N	AA12
AB12	LVDS1_TX2_P	51	52	LVDS1_TX3_P	Y12
	GND	53	54	GND	

3. TV-Out or VGA

M53 offers one analog TV-out or VGA Port:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	193	194	GND	
AC21	TVE_RED	195	196	TVE_HSYNC	V1
AB20	TVE_GREEN	197	198	TVE_VSYNC	V2
AB19	TVE_BLUE	199	200	PWM1	G6
	GND	201	202	GND	

Camera Port

The i.MX53 CPU provides two camera ports - controlled by a CSI sub-block - providing a connection to image sensors and related devices. The role of these ports is to receive input from image sensors (or TV decoders) and to provide support for time-sensitive control signals to the camera. Non-time-sensitive controls - such as configuration, reset - are performed by the ARM Core through an I2C interface or General Purpose I/O Module (GPIO) signal. Each of the camera ports includes the following features:

- Direct connectivity to most relevant image sensors and to TV decoders.
- Parallel interface - up to 20-bit data bus
- Frame size: up to 8192 x 4096 pixels (including blanking intervals)
- Data formats supported include Raw (Bayer), RGB, YUV 4:4:4, YUV 4:2:2 and grayscale, up to 16 bits per value (component).
- **Synchronization - video mode**
  - The sensor is the master of the pixel clock (PIXCLK) and synchronization signals
  - **Synchronization signals are received using either of the following methods:**
    - Dedicated control signals -VSYNC, HSYNC - with programmable pulse width and polarity
    - Controls embedded in the data stream, following loosely the BT.656 protocol, with flexibility in code values and location.
- **Synchronization - still image capture**
  - The image capture is triggered by the ARM Core or by an external signal (for example, a mechanical shutter)
  - Synchronized strobes are generated for up to 6 outputs - the sensor and camera peripherals (flash, mechanical shutter...)
- **Additional features**
  - Frame rate reduction, by periodic skipping of frames
  - Window-of-interest selection
  - Pre-flash - for red-eye reduction and for measurements (such as focus) in low-light conditions

Several sensors can be connected to each of the CSIs. Simultaneous functionality (sending data) is supported as follows:

- Two sensors can send data independently, each through a different port.
- Only one of the streams can be transferred to the VDIC or IC for on-the-fly processing, while the other one is sent directly to system memory.

The input rate supported by the camera port is as follows:

- Peak: up to 180 MHz (values/sec)
- **Average (assuming 35% blanking overhead), for YUV 4:2:2**
  - Pixel in one cycle (BT.1120): up to 135 MP/sec, e.g. 9M pixels @ 15 fps
  - Pixel on two cycles (BT.656): up to 67 MP/sec, e.g. 4.5M pixels @ 15 fps.
  - On-the-fly processing may be restricted to a lower input rate.

M53 offers on camera port on the following pins:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	95	96	GND	
R1	CSI0_DAT4	97	98	CSI0_DAT12	T3
R2	CSI0_DAT6	101	102	CSI0_DAT14	U1
R3	CSI0_DAT7	103	104	CSI0_DAT15	U2
T1	CSI0_DAT8	105	106	CSI0_DAT16	T4
R4	CSI0_DAT9	107	108	CSI0_DAT17	T5
R5	CSI0_DAT10	109	110	CSI0_DAT18	U3
T2	CSI0_DAT11	111	112	CSI0_DAT19	U4
P4	CSI0_VSYNC	113	114	CSI0_PIXCLK	P1
P2	CSI0_HSYNC	115	116	CSI0_DAT_EN	P3
	GND	117	118	GND	

Audio

M53 supplies an Audio interface on the following pins:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	117	118	GND	
D13	AUD4_RXD	119	120	AUD4_TXFS	C14
D14	AUD4_TXD	121	122	AUD4_RXFS	E14
E13	AUD4_TXC	123	124	SSI_EXT1_CLK	C8
C6	SPDIF_RX	125	126	SPDIF_TX	A3
	GND	127	128	GND	

The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, Sony/Phillips Digital Interface (SPDIF) transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. It is a superset of the 56300 Family ESSI peripheral and of the 56000 Family SAI peripheral. The ESAI is named synchronous because all serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is similar in that it is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available.

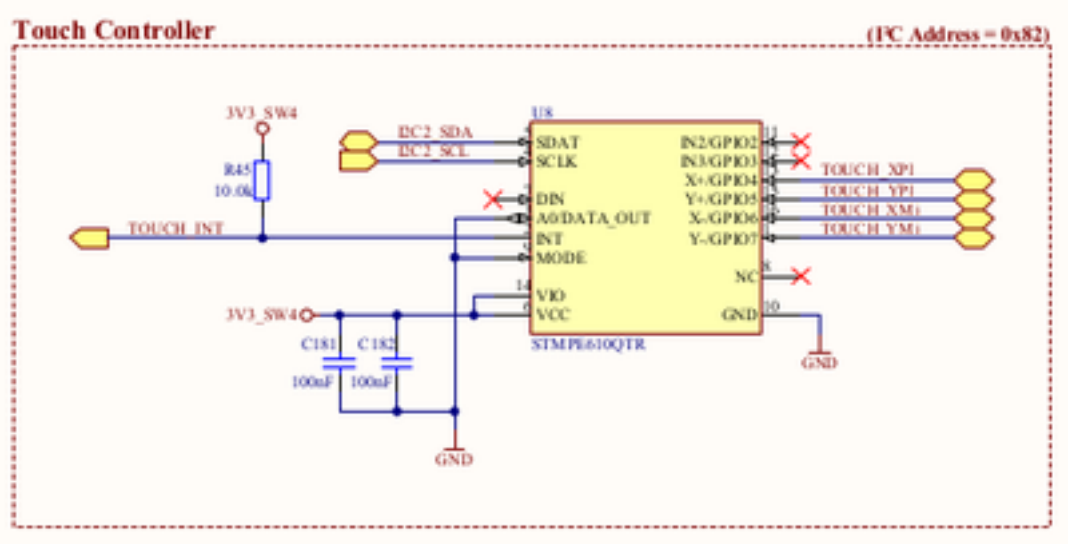
Feature set:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Up to six transmitters and four receivers with SDO2/SDI3, SDO3/SDI2, SDO4/SDI1 and SDO5/SDI0 pins shared by transmitters 2 to 5 and receivers 0 to 3. SDO0 and SDO1 pins are used by transmitters 0 and 1 only.
- Programmable data interface modes such as I2S, LSB aligned, MSB aligned
- Programmable word length (8, 12, 16, 20 or 24bits)

- Flexible selection between system clock or external oscillator as input clock source, programmable internal clock divider and frame sync generation AC97 support
- Time Slot Mask Registers for reduced ARM platform overhead (for both Transmit and Receive)
- 128-word Transmit FIFO shared by six transmitters
- 128-word Receive FIFO shared by four receivers

Touchscreen

M53 features a STMPE610 touch screen controller which is connected to interface I2C2.



The touchscreen controller is available on the following pins:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	89	90	GND	
	Touch X+	91	92	Touch Y+	
	Touch X-	93	94	Touch Y-	
	GND	95	96	GND	

A 4-wire touchscreen controller is built into the STMPE610. The touchscreen controller is enhanced with a movement tracking algorithm to avoid excessive data, 128 x 32 bit buffer and a programmable active window feature. More information on the STMPE610 is available under http://www.st.com/st-web-ui/static/active/en/resource/technical/document/datasheet/CD00226473.pdf

3.2.5 Storage Interfaces

SATA

M53 offers an integrated Serial Advanced Technology Attachment (SATA) Controller that is compatible with the Advanced Host Controller Interface (AHCI) specification. The SATA Controller block (SATA) along with integrated physical link hardware (SATA PHY) provide one SATA port for the attachment of external SATA compliant storage devices. The SATA interface is available on the following pins:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	127	128	GND	
B12	SATA_RXP	129	130	SATA_TXP	A10
A12	SATA_RXM	131	132	SATA_TXM	B10
	GND	133	134	GND	

The SATA block provides the following features:

- Compliant with Serial ATA Specification 2.6, and AHCI Revision 1.3 specifications (except FIS-based switching) at 1.5 Gb/s port speed
- Rx Data Buffer for recovered clock systems
- Data alignment circuitry
- OOB signaling detection and generation
- Asynchronous Signal Recovery, including retry polling
- Digitally supports device hot-plugging
- 8b/10b encoding/decoding
- Supports power management features including automatic Partial to Slumber transition
- Supports BIST loopback data checking on a per FIS basis
- Supports one SATA device (Port 0)
- AMBA AHB interface (one master and one slave)
- Internal DMA engine for reading command lists and transferring data
- Supports hardware-assisted Native Command Queuing for up to 32 entries
- Supports Port Multiplier with command-based switching
- Activity LED support
- Supports disabling Rx and Tx Data clocks during power down modes
- Supports eSATA (when external analog logic also supports eSATA)

ESDHC

The Enhanced Secured Digital Host Controller Version 2 provides the interface between the host system and the SD/SDIO/ MMC cards. The ESDHC acts as a bridge, passing host bus transactions to the SD/SDIO/MMC cards by sending commands and performing data accesses to/from the cards. It handles the SD/SDIO/MMC protocols at the transmission level.

The following pins represent the ESDHC interface:

i.MX53 Ball	Function	Pin	Pin	Function	i.MX53 Ball
	GND	133	134	GND	
A20	ESDHC1_DAT0	135	136	ESDHC1_CLK	E16
C17	ESDHC1_DAT1	137	138	ESDHC1_CMD	F18
F17	ESDHC1_DAT2	139	140	ESDHC1_CD#	B7
F16	ESDHC1_DAT3	141	142	ESDHC1_WP	E8
	GND	143	144	GND	

The features of the ESDHC include the following:

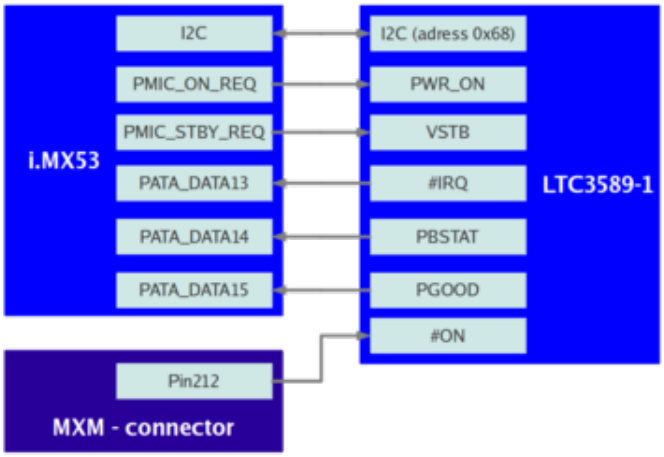
- Conforms to the SD Host Controller Standard Specification version 2.0 including Test Event register support

- Compatible with the MMC System Specification version 4.2/4.3
- Compatible with the SD Memory Card Specification version 2.0 and supports the High Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 2.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 52 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes devices
- Up to 200 Mbps of data transfer for SD/SDIO cards using 4 parallel data lines
- Up to 416 Mbps of data transfer for MMC cards using 8 parallel data lines in SDR (Single Data Rate) mode
- Supports Single Block, Multi Block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort
- Supports pause during the data transfer at block gap
- Supports SDIO Read Wait and Suspend Resume operations
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period
- Embodies a fully configurable 128x32-bit FIFO for read/write data
- Supports internal and external DMA capabilities
- Supports Advanced DMA to perform linked memory access

The ESDHC can select the following modes for data transfer:

- SD 1-bit
- SD 4-bit
- MMC 1-bit
- MMC 4-bit
- MMC 8-bit
- Identification Mode (up to 400 kHz)
- MMC full speed mode (up to 20 MHz)
- MMC high speed mode (up to 52 MHz)
- SD/SDIO full speed mode (up to 25 MHz)
- SD/SDIO high speed mode (up to 50 MHz)

3.3 Power Management



All necessary voltages for operating M53 are build on the SoM using a LTC3589-1. The LTC3589-1 can be configured using the I2C2 interface. I²C adress is 0x68.

Power can be supplied as follows:

Supply Voltage	Supply Pins
2,7V...5,5V	223, 224, 225, 226, 227, 228
GND GND GND GND GND	1, 2, 19, 20, 23, 24, 29, 30, 35, 36, 41, 42, 47, 48, 53, 54, 71, 72, 89, 90, 95, 96, 117, 118, 127, 128, 133, 134, 143, 144, 157, 158, 158, 179, 180, 201, 202, 229, 230

3.3.1 Pushbutton Interface

For switching M53 on and off the Pushbutton Interface could be implemented. It is available on the following pin

Pin	Function	i.MX53 Ball
212	Power Switch	

3.4 Reset

A reset is applied to the M53 module by driving the reset input on pin 206 low. The reset line is implemented as open drain, pin 221 is directly connected to the i.MX53 CPU.

M53 Functional Block	Pin
Reset	206