
M100PFEVP Hardware Manual

Release 1

ARIES Embedded GmbH

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ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

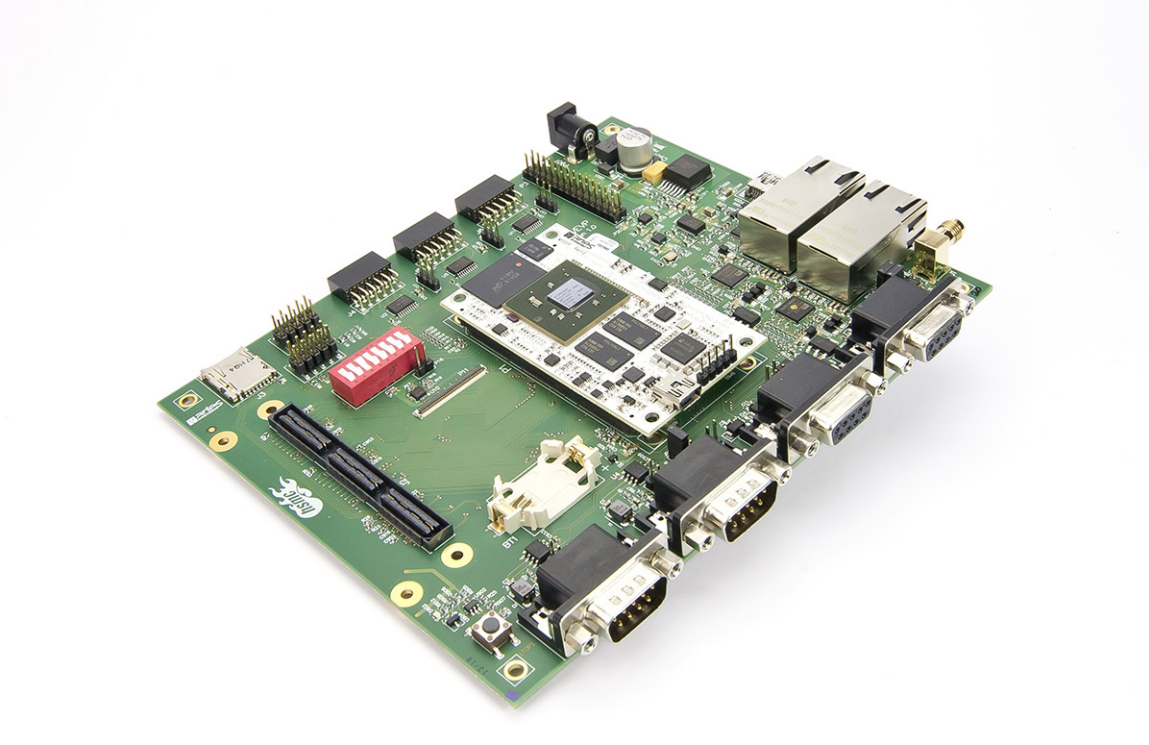
1.6 Change Log

Revision	Date	Revised	Comment
1.0	05.09.2019	aw	Initial creation

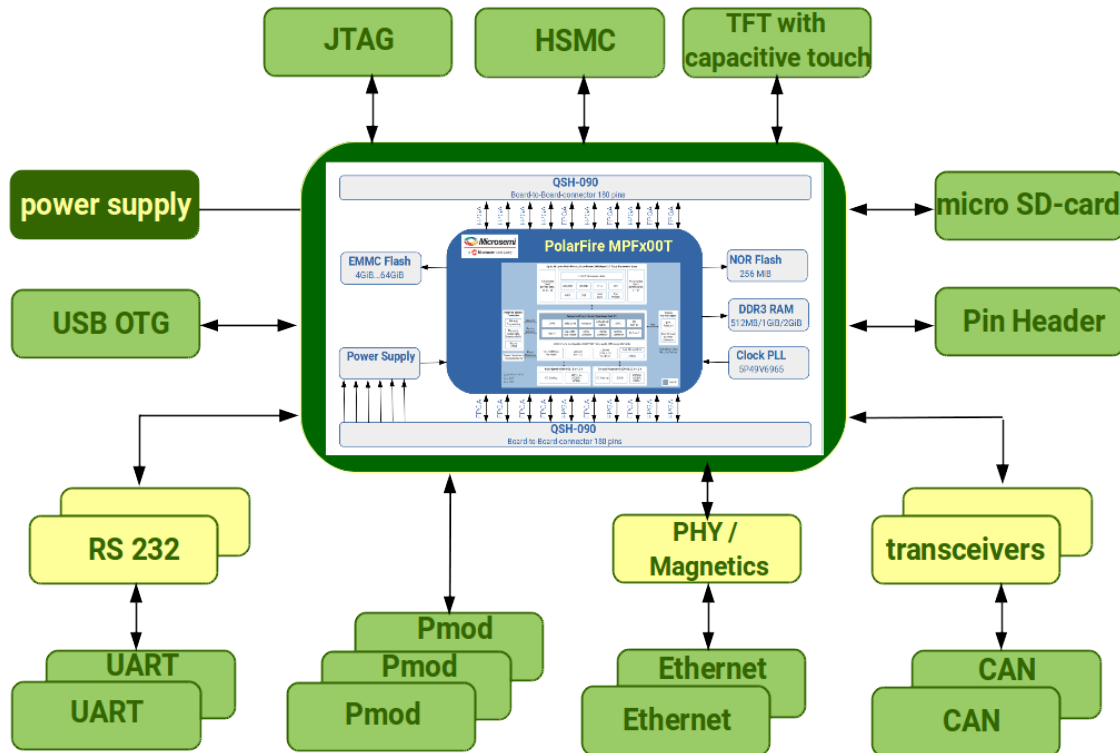
OVERVIEW

M100PFEVP represents the flexible Evaluation Platform for working with the M100PF SoM for PolarFire FPGAs.

The system helps developers to have a smooth start with the M100PF SoMs, it can be used for designing IP, developing software as well as implementing prototypes.



2.1 Block Diagram

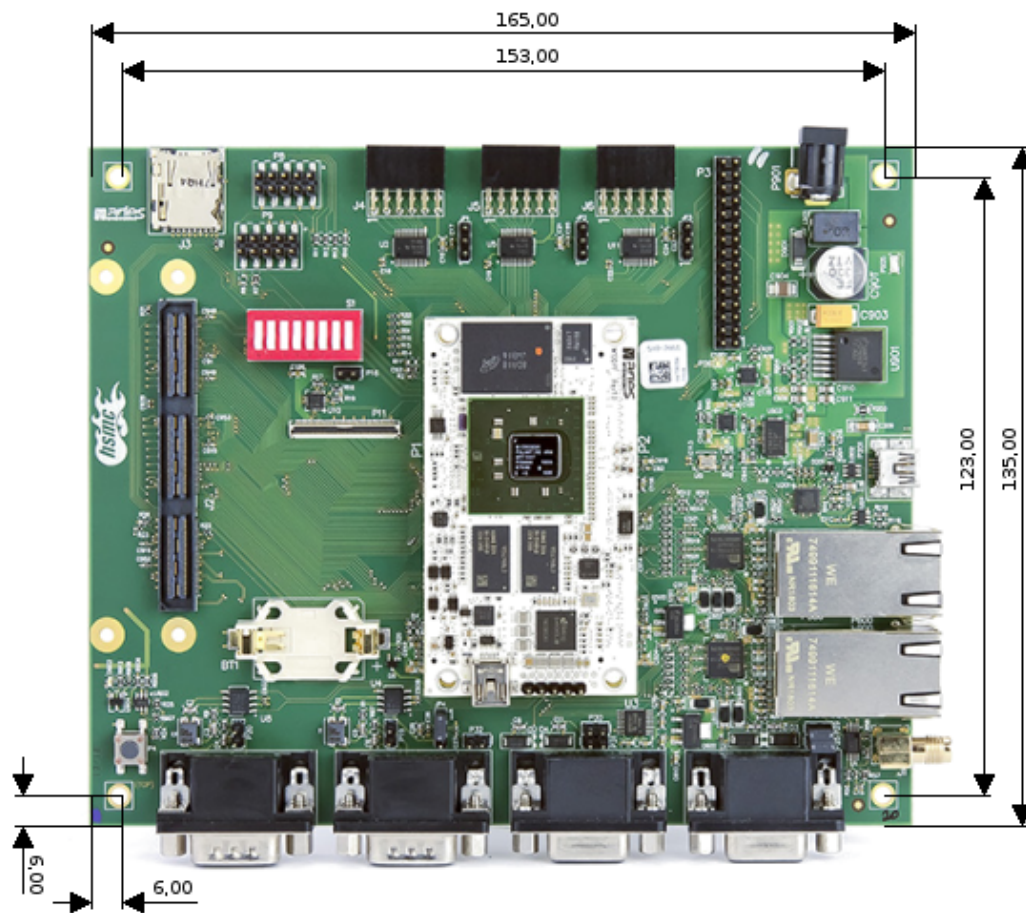


2.2 Feature Set

For supporting development projects and fast prototyping in the best possible way M100PFEVP supplies:

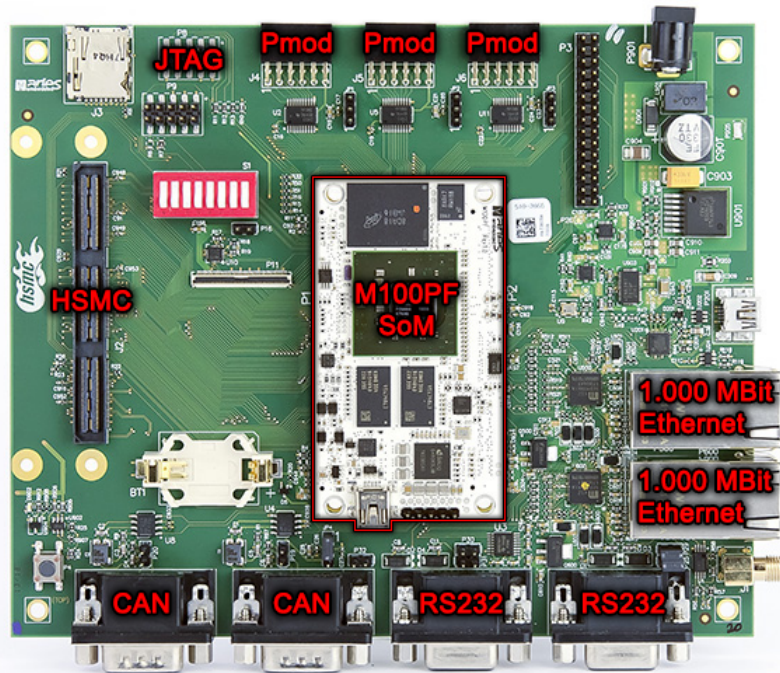
- 2x Gigabit Ethernet on a RJ45 connector
- USB on a mini-USB connector
- 2x UART on a DUSB-9 connector each
- 2x CAN on a DUSB-9 connector each
- TFT with Touch
- HSMC extension connector
- 3x PMOD extension connectors
- microSD-card slot
- JTAG pin header
- flexible supply voltage 7V to 36V DC

2.3 Dimensions



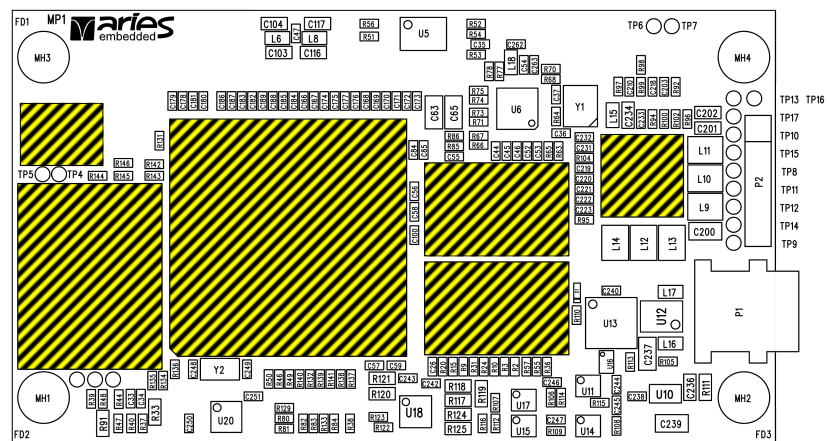
2.4 Parts Location

The available functional blocks can be found on the baseboard as follows:



2.5 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on M100PF it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



RESOURCES

3.1 Ethernet

M100PFEVP offers two Ethernet Ports in RGMII mode to be controlled by the PolarFire FPGA. These ports can be accessed via the RJ45 connectors P500 and P600 supported by Microchip KSZ903 Ethernet physical-layer transceivers.

3.2 UART

Two UARTs are available on a RS232 signal level.

The interface jumpers can be set vertical or horizontal so that the interface complies with straight- or cross-type RS232 cables. The following table shows the signal for horizontal jumper setting, in case of vertical jumper settings RX and TX signals are swapped accordingly.

3.2.1 UART 1 (P21)

Pin	Function	Connector	FPGA Pin
2	UART0_TX	P2-132	K8
3	UART0_RX	P2-138	J8
5	GND		

3.2.2 UART 2 (P22)

Pin	Function	Connector	FPGA Pin
2	UART1_TX	P1-75	K6
3	UART1_RX	P1-77	J7
5	GND		

3.3 USB-OTG

M100PFEVP supports an USB-OTG port. The Microchip USB3320 USB-OTG Phy drives the physical connection. The respective connector on M100PFEVP can be found at position P201.

Note: USB-OTG is not supported by the current version of the M100PF SoM.

3.4 CAN

Two CAN ports are available on M100PFEVP. The signals on the DSUB connector can optionally be terminated by 120 Ohms. This is done by setting the jumpers at position P19 and P20.

Function	Connector	FPGA Pin
CAN0_TX	P2-129	F17
CAN0_RX	P2-137	G17
CAN1_TX	P2-135	F16
CAN1_RX	P2-130	F15

3.4.1 CAN1 (P23)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.4.2 CAN2 (P24)

Pin	Function
2	CAN-L
3	GND
7	CAN-H

3.5 JTAG (P8)

P8 provides the JTAG signals of the FPGA to the outer world. The JTAG connector complies with the standard pinout, the FlashPro5 can be directly connected. The following signals are available:

Function	Connector	FPGA Pin	Pin	Pin	FPGA Pin	Connector	Function
TCK	P1-6	F8	1	2	–	–	GND
TDO	P1-4	F6	3	4	–	–	3.3V
TMS	P1-10	F7	5	6	–	–	–
–	–	–	7	8	–	–	–
TDI	P1-8	G8	9	10	–	–	GND

3.6 Pmod Module Connectors

Three 2x6 angled pin headers are available on the M100PFEVP board which fit the requirements for Pmod modules. To support a wider range of possible modules, each connector has its own level shifter. A corresponding jumper allows the selection between 3.3V or 5V module voltage.

3.6.1 Pmod J4:

Function	Connector	FPGA Pin	Pin	Pin	FPGA Pin	Connector	Function
GPIO_R1	P1-120	R1	1	7	T1	P1-118	GPIO_T1
GPIO_N1	P1-133	N1	2	8	P1	P1-131	GPIO_P1
GPIO_R3	P1-115	R3	3	9	T5	P1-113	GPIO_T5
GPIO_E11	P2-70	E11	4	10	F11	P2-71	GPIO_F11
GND	–	–	5	11	–	–	GND
3.3V	–	–	6	12	–	–	3.3V

3.6.2 Pmod J5:

Function	Connector	FPGA Pin	Pin	Pin	FPGA Pin	Connector	Function
GPIO_M8	P2-136	M8	1	7	N6	P2-127	GPIO_N6
GPIO_T6	P1-162	T6	2	8	N7	P2-121	GPIO_N7
GPIO_B17	P1-17	B17	3	9	M9	P2-128	GPIO_M9
GPIO_A13	P1-15	A13	4	10	N5	P2-123	GPIO_N5
GND	–	–	5	11	–	–	GND
3.3V	–	–	6	12	–	–	3.3V

3.6.3 Pmod J6:

Function	Connector	FPGA Pin	Pin	Pin	FPGA Pin	Connector	Function
GPIO_K4	P2-93	K4	1	7	L3	P2-125	GPIO_L3
GPIO_L7	P2-80	L7	2	8	M4	P2-122	GPIO_M4
GPIO_M7	P2-90	M7	3	9	M5	P2-133	GPIO_M5
GPIO_K5	P2-97	K5	4	10	F10	P2-155	GPIO_F10
GND	–	–	5	11	–	–	GND
3.3V	–	–	6	12	–	–	3.3V

3.7 HSMC Connector (J2)

M100PFEVP hosts a High Speed Mezzanine Card (HSMC) connector. Its pinout is shown in the following table.

Function	Connector	FPGA pin	Pin	Pin	FPGA pin	Connector	Function
–	–	–	1	2	–	–	–
–	–	–	3	4	–	–	–
GND	–	–	5	6	–	–	GND
–	–	–	7	8	–	–	–
–	–	–	9	10	–	–	–
GND	–	–	11	12	–	–	GND
GXB_TX_L5_P	P2-40	H22	13	14	F22	P2-34	GXB_RX_L5_P
GXB_TX_L5_N	P2-42	H21	15	16	F21	P2-36	GXB_RX_L5_N
GND	–	–	17	18	–	–	GND
GXB_TX_L4_P	P2-28	D22	19	20	C20	P2-22	GXB_RX_L4_P
GXB_TX_L4_N	P2-30	D21	21	22	C19	P2-24	GXB_RX_L4_N
GND	–	–	23	24	–	–	GND
GXB_TX_L3_P	P2-16	B22	25	26	A20	P2-10	GXB_RX_L3_P

Continued on next page

Table 3.1 – continued from previous page

Function	Connector	FPGA pin	Pin	Pin	FPGA pin	Connector	Function
GXB_TX_L3_N	P2-18	B21	27	28	A19	P2-12	GXB_RX_L3_N
GND	–	–	29	30	–	–	GND
GXB_TX_L2_P	P2-39	Y22	31	32	W20	P2-33	GXB_RX_L2_P
GXB_TX_L2_N	P2-41	Y21	33	34	W19	P2-35	GXB_RX_L2_N
GND	–	–	35	36	–	–	GND
GXB_TX_L1_P	P2-27	V22	37	38	T22	P2-21	GXB_RX_L1_P
GXB_TX_L1_N	P2-29	V21	39	40	T21	P2-23	GXB_RX_L1_N
GND	–	–	41	42	–	–	GND
GXB_TX_L0_P	P2-15	P22	43	44	M22	P2-9	GXB_RX_L0_P
GXB_TX_L0_N	P2-17	P21	45	46	M21	P2-11	GXB_RX_L0_N
GND	–	–	47	48	–	–	GND
HPS_GPIO51	P2-134	M3	49	50	F13	P2-131	HPS_GPIO52
TCK	P1-6	F8	51	52	F7	P1-10	TMS
GND	–	–	53	54	–	–	GND
HSMC_TDO	–	–	55	56	–	–	HSMC_TDI
CLK25_HSMC	–	–	57	58	–	–	–
GND	–	–	59	60	–	–	GND
IOB4A11	P1-132	–	61	62	–	P1-156	IOB4A0/CLK3p
IOB4A10	P1-134	–	63	64	–	P1-154	IOB4A1/CLK3n
3.3V	–	–	65	66	–	–	VIN
IOB4A28	P1-94	–	67	68	–	P1-152	IOB4A2
IOB4A29	P1-92	–	69	70	–	P1-150	IOB4A3
3.3V	–	–	71	72	–	–	VIN
IOB4A30	P1-90	–	73	74	–	P1-148	IOB4A4
IOB4A31	P1-88	–	75	76	–	P1-146	IOB4A5
3.3V	–	–	77	78	–	–	VIN
IOB4A32	P1-84	–	79	80	–	P1-144	IOB4A6
IOB4A33	P1-82	–	81	82	–	P1-142	IOB4A7
3.3V	–	–	83	84	–	–	VIN
IOB4A40	P1-143	–	85	86	–	P1-136	IOB4A9
IOB4A41	P1-141	–	87	88	–	P1-138	IOB4A8
3.3V	–	–	89	90	–	–	VIN
IOB4A42	P1-137	–	91	92	–	P1-128	IOB4A13
IOB4A43	P1-135	–	93	94	–	P1-130	IOB4A12
3.3V	–	–	95	96	–	–	VIN
IOB4A48	P1-125	–	97	98	–	P1-124	IOB4A15
IOB4A49	P1-123	–	99	100	–	P1-126	IOB4A14
3.3V	–	–	101	102	–	–	VIN
IOB4A50	P1-119	–	103	104	–	P1-116	IOB4A18
IOB4A51	P1-117	–	105	106	–	P1-114	IOB4A19
3.3V	–	–	107	108	–	–	VIN
IOB4A54	P1-111	–	109	110	–	P1-21	IOB8A0
IOB4A55	P1-109	–	111	112	–	P1-19	IOB8A1
3.3V	–	–	113	114	–	–	VIN
CLKEXT_P	P2-160	–	115	116	U19	P2-3	REFCLK0L_P
CLKEXT_N	P2-162	–	117	118	U20	P2-5	REFCLK0L_N
3.3V	–	–	119	120	–	–	VIN
IOB4A56	P1-107	–	121	122	–	P1-108	IOB4A22
IOB4A57	P1-105	–	123	124	–	P1-106	IOB4A23

Continued on next page

Table 3.1 – continued from previous page

Function	Connector	FPGA pin	Pin	Pin	FPGA pin	Connector	Function
3.3V	–	–	125	126	–	–	VIN
IOB4A58	P1-101	–	127	128	–	P1-102	IOB4A24
IOB4A59	P1-99	–	129	130	–	P1-100	IOB4A25
3.3V	–	–	131	132	–	–	VIN
IOB4A62	P1-93	–	133	134	–	P1-98	IOB4A26
IOB4A63	P1-91	–	135	136	–	P1-96	IOB4A27
3.3V	–	–	137	138	–	–	VIN
IOB4A64	P1-89	–	139	140	–	P1-155	IOB4A34
IOB4A65	P1-87	–	141	142	–	P1-153	IOB4A35
3.3V	–	–	143	144	–	–	VIN
IOB4A66	P1-83	–	145	146	–	P1-151	IOB4A36
IOB4A67	P1-81	–	147	148	–	P1-149	IOB4A37
3.3V	–	–	149	150	–	–	VIN
IOB3B24	P1-59	–	151	152	–	P1-147	IOB4A38
IOB3B25	P1-57	–	153	154	–	P1-145	IOB4A39
3.3V	–	–	155	156	–	–	VIN
IOB3B19	P1-71	–	157	158	–	P1-129	IOB4A46
IOB3B18	P1-73	–	159	160	–	P1-127	IOB4A47
3.3V	–	–	161	162	–	–	VIN
IOB3B20	P1-69	–	163	164	–	P1-97	IOB4A60
IOB3B21	P1-67	–	165	166	–	P1-95	IOB4A61
3.3V	–	–	167	168	–	–	VIN
IOB3B22	P1-65	–	169	170	–	P1-24	IOB5B0/CLK4p
IOB3B23	P1-63	–	171	172	–	P1-22	IOB5B1/CLK4n
3.3V	–	–	173	174	–	–	VIN
IOB5B2/CLKOUTp	P1-20	–	175	176	–	P1-16	IOB5B4/CLK5p
IOB5B3/CLKOUTn	P1-18	–	177	178	–	P1-14	IOB5B5/CLK5n
3.3V	–	–	179	180	L8	P2-156	HPS_GPI0
GND	–	–	181	182	–	–	GND
GND	–	–	183	184	–	–	GND
GND	–	–	185	186	–	–	GND
GND	–	–	187	188	–	–	GND
GND	–	–	189	190	–	–	GND
GND	–	–	191	192	–	–	GND

3.8 Samtec Connector

The M100PF SoM connects to the M100PFEVP Baseboard using two Samtec QSH-090-01-F-D-A connectors.

3.8.1 Connector P1

Function	FPGA Pin	Pin	Pin	FPGA Pin	Function
3.3V	–	1	2	G7	GND
3.3V	–	3	4	F6	JTAG_TDO
3.3V	–	5	6	F8	JTAG_TCK
3.3V	–	7	8	G8	JTAG_TDI
3.3V	–	9	10	F7	JTAG_TMS
3.3V	–	11	12	–	2.5V / 3.3V
2.5V / 3.3V (*)	–	13	14	–	HSMC 178 (*)
PMod J5 3	A13	15	16	–	HSMC 176 (*)
PMod J5 4	B17	17	18	–	HSMC 177 (*)
HSMC 112 (*)	–	19	20	–	HSMC 175 (*)
HSMC 110 (*)	–	21	22	–	HSMC 172 (*)
2.5V / 3.3V (*)	–	23	24	–	HSMC 170 (*)
3.3V	–	25	26	–	2.5V / 3.3V (*)
SD_DATA2	C9	27	28	C20	LCD_CLK
SD_DATA3	B10	29	30	A3	LCD_R0
SD_CMD	B9	31	32	D3	LCD_R1
SD_CLK	A2	33	34	E3	LCD_R2
SD_DATA0	C12	35	36	B3	LCD_R3
SD_DATA1	C11	37	38	B2	LCD_R4
SD_DETECT	C10	39	40	E5	LCD_R5
LCD_T_RESET	A12	41	42	F5	LCD_R6
3.3V (*)	–	43	44	–	3.3V (*)
LCD_B4	E8	45	46	C4	LCD_R7
LCD_B5	B5	47	48	D4	LCD_G0
LCD_B6	C5	49	50	E4	LCD_G1
LCD_B7	C6	51	52	F3	LCD_G2
LCD_DIM	C7	53	54	A6	LCD_G3
LCD_DISP	D7	55	56	B4	LCD_G4
HSMC 153 (*)	–	57	58	D6	LCD_G5
HSMC 151 (*)	–	59	60	E6	LCD_G6
3.3V (*)	–	61	62	–	3.3V (*)
HSMC 171 (*)	–	63	64	G2	LCD_G7
HSMC 169 (*)	–	65	66	H2	LCD_B0
HSMC 165 (*)	–	67	68	J2	LCD_B1
HSMC 163 (*)	–	69	70	L2	LCD_B2
HSMC 157 (*)	–	71	72	M2	LCD_B3
HSMC 159 (*)	–	73	74	H1	LCD_HSYNC
UART1_TX	K6	75	76	J1	LCD_VSYNC
UART1_RX	J7	77	78	K1	LCD_DE
3.3V (*)	–	79	80	–	3.3V (*)
HSMC 147 (*)	–	81	82	–	HSMC 81 (*)
HSMC 145 (*)	–	83	84	–	HSMC 79 (*)

Continued on next page

Table 3.2 – continued from previous page

Function	FPGA Pin	Pin	Pin	FPGA Pin	Function
3.3V (*)	–	85	86	–	3.3V (*)
HSMC 141 (*)	–	87	88	–	HSMC 75 (*)
HSMC 139 (*)	–	89	90	–	HSMC 73 (*)
HSMC 135 (*)	–	91	92	–	HSMC 69 (*)
HSMC 133 (*)	–	93	94	–	HSMC 67 (*)
HSMC 166 (*)	–	95	96	–	HSMC 136 (*)
HSMC 164 (*)	–	97	98	–	HSMC 134 (*)
HSMC 129 (*)	–	99	100	–	HSMC 130 (*)
HSMC 127 (*)	–	101	102	–	HSMC 128 (*)
3.3V (*)	–	103	104	–	3.3V (*)
HSMC 123 (*)	–	105	106	–	HSMC 124 (*)
HSMC 121 (*)	–	107	108	–	HSMC 122 (*)
HSMC 111 (*)	–	109	110	R5	ETH1_RXC
HSMC 109 (*)	–	111	112	F1	P3 26
Pmod J4 9	T5	113	114	–	HSMC 106 (*)
Pmod J4 3	R3	115	116	–	HSMC 104 (*)
HSMC 105 (*)	–	117	118	T1	Pmod J4 7
HSMC 103 (*)	–	119	120	R1	Pmod J4 1
3.3V (*)	–	121	122	–	3.3V (*)
HSMC 99 (*)	–	123	124	–	HSMC 98 (*)
HSMC 97 (*)	–	125	126	–	HSMC 100 (*)
HSMC 160 (*)	–	127	128	–	HSMC 92 (*)
HSMC 158 (*)	–	129	130	–	HSMC 94 (*)
Pmod J4 8	P1	131	132	–	HSMC 61 (*)
Pmod J4 2	N1	133	134	–	HSMC 63 (*)
HSMC 93 (*)	–	135	136	–	HSMC 86 (*)
HSMC 91 (*)	–	137	138	–	HSMC 88 (*)
3.3V (*)	–	139	140	–	3.3V (*)
HSMC 87 (*)	–	141	142	–	HSMC 82 (*)
HSMC 85 (*)	–	143	144	–	HSMC 80 (*)
HSMC 154 (*)	–	145	146	–	HSMC 76 (*)
HSMC 152 (*)	–	147	148	–	HSMC 74 (*)
HSMC 148 (*)	–	149	150	–	HSMC 70 (*)
HSMC 146 (*)	–	151	152	–	HSMC 68 (*)
HSMC 142 (*)	–	153	154	–	HSMC 64 (*)
HSMC 140 (*)	–	155	156	–	HSMC 62 (*)
2.5V / 3.3V (*)	–	157	158	–	2.5V / 3.3V (*)
ETH1_GTXCLK	P4	159	160	F2	P3 28
ETH1_MDC	N8	161	162	T6	Pmod J5 2
ETH1_TXD1	P3	163	164	P7	ETH1_MDIO
ETH1_RX_DV	P8	165	166	R4	ETH1_TXD3
P3 10	L1	167	168	R6	ETH1_RXD2
ETH1_RXD0	R8	169	170	P9	ETH1_RXD1
ETH1_TXD2	N4	171	172	T3	ETH1_TX_EN
ETH1_RXD3	P6	173	174	T2	ETH1_TXD0
2.5V / 3.3V (*)	–	175	176	–	2.5V / 3.3V (*)
3.3V	–	177	178	–	3.3V
3.3V	–	179	180	–	3.3V
Ground Plate	–	181	182	–	Ground Plate

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Table 3.2 – continued from previous page

Function	FPGA Pin	Pin	Pin	FPGA Pin	Function
Ground Plate	–	183	184	–	Ground Plate
Ground Plate	–	185	186	–	Ground Plate
Ground Plate	–	187	188	–	Ground Plate
Ground Plate	–	189	190	–	Ground Plate
Ground Plate	–	191	192	–	Ground Plate

Note: Functions marked with (*) are not connected on the M100PF SoM side.

3.8.2 Connector P2

Function	FPGA Pin	Pin	Pin	FPGA Pin	Function
GND	–	1	2	–	GND
HSMC 116	U19	3	4	J19	REFCLK1_P
HSMC 118	U20	5	6	J20	REFCLK1_N
GND	–	7	8	–	GND
HSMC 44	M22	9	10	A20	HSMC 26
HSMC 46	M21	11	12	A19	HSMC 28
GND	–	13	14	–	GND
HSMC 43	P22	15	16	B22	HSMC 25
HSMC 45	P21	17	18	B21	HSMC 27
GND	–	19	20	–	GND
HSMC 38	T22	21	22	C20	HSMC 20
HSMC 40	T21	23	24	C19	HSMC 22
GND	–	25	26	–	GND
HSMC 37	V22	27	28	D22	HSMC 19
HSMC 39	V21	29	30	D21	HSMC 21
GND	–	31	32	–	GND
HSMC 32	W20	33	34	F22	HSMC 14
HSMC 34	W19	35	36	F21	HSMC 16
GND	–	37	38	–	GND
HSMC 31	Y22	39	40	H22	HSMC 13
HSMC 33	Y21	41	42	H21	HSMC 15
GND	–	43	44	–	GND
–	AA20	45	46	L20	–
–	AA19	47	48	L19	–
GND	–	49	50	–	GND
–	AB22	51	52	K22	–
–	AB21	53	54	K21	–
GND	–	55	56	–	GND
–	–	57	58	–	–
–	–	59	60	–	–
3.3V	–	61	62	–	3.3V
–	–	63	64	–	–
–	–	65	66	–	–

Continued on next page

Table 3.3 – continued from previous page

Function	FPGA Pin	Pin	Pin	FPGA Pin	Function
–	–	67	68	–	–
–	–	69	70	E11	Pmod J4 4
Pmod J4 10	F11	71	72	–	–
–	–	73	74	–	–
3.3V	–	75	76	–	3.3V
1.8V (*)	–	77	78	–	2.5V (*)
P3 5	E14	79	80	L7	Pmod J6 2
USB_DIR (*)	–	81	82	–	USB_D6 (*)
USB_CLK (*)	–	83	84	–	USB_D7 (*)
USB_D4 (*)	–	85	86	–	USB_D5 (*)
USB_D1 (*)	–	87	88	–	USB_NXT (*)
P3 3	C14	89	90	M7	Pmod J6 3
P32 Boot Mode	J6	91	92	D14	P3 7
Pmod J6 1	K4	93	94	L6	Pmod J6 10
USB_STP (*)	–	95	96	C15	P3 2
Pmod J6 4	K5	97	98	–	USB_D2 (*)
USB_D3 (*)	–	99	100	–	USB_D0 (*)
1.8V (*)	–	101	102	–	2.5V (*)
3.3V	–	103	104	–	3.3V
ETH0_TXD3	H13	105	106	C16	ETH0_TXD0
ETH0_TXD1	A16	107	108	A15	ETH0_TXD2
ETH0_RXD3	D16	109	110	G15	ETH0_RXD0
ETH0_RXD2	D17	111	112	B15	ETH0_MDC
ETH0_GTXCLK	B14	113	114	C17	ETH0_TX_EN
ETH0_MDIO	A17	115	116	H15	ETH0_RXD1
ETH0_RX_DV	E16	117	118	G14	ETH0_RXC
3.3V	–	119	120	–	3.3V
Pmod J5 8	N7	121	122	M4	Pmod J6 8
Pmod J5 10	N5	123	124	–	LCD_T_INT (*)
Pmod J6 7	L3	125	126	H6	I2C0_SDA
Pmod J5 7	N6	127	128	M9	Pmod J5 9
CAN0_TX	F17	129	130	F15	CAN1_RX
HSMC 50	F13	131	132	K8	UART0_TX
Pmod J6 9	M5	133	134	M3	HSMC 49
CAN1_TX	F16	135	136	M8	Pmod J5 1
CAN0_RX	G17	137	138	J8	UART0_RX
I2C0_SCL	H5	139	140	–	3.3V
3.3V	–	141	142	–	3.3V
P3 23	E13	143	144	J3	P3 9
P3 25	D13	145	146	E10	P3 13
P3 17	F12	147	148	–	ETH1_INT (*)
P3 11	D11	149	150	K3	P3 15
–	–	151	152	G12	P3 27
P3 19	D12	153	154	G13	ETH0_INT
P3 21	F10	155	156	L8	HSMC 180
3.3V	–	157	158	–	3.3V
RST_N	–	159	160	–	OCLK_P
VBAT	–	161	162	–	OCLK_N
3.3V	–	163	164	–	2.5V (*)

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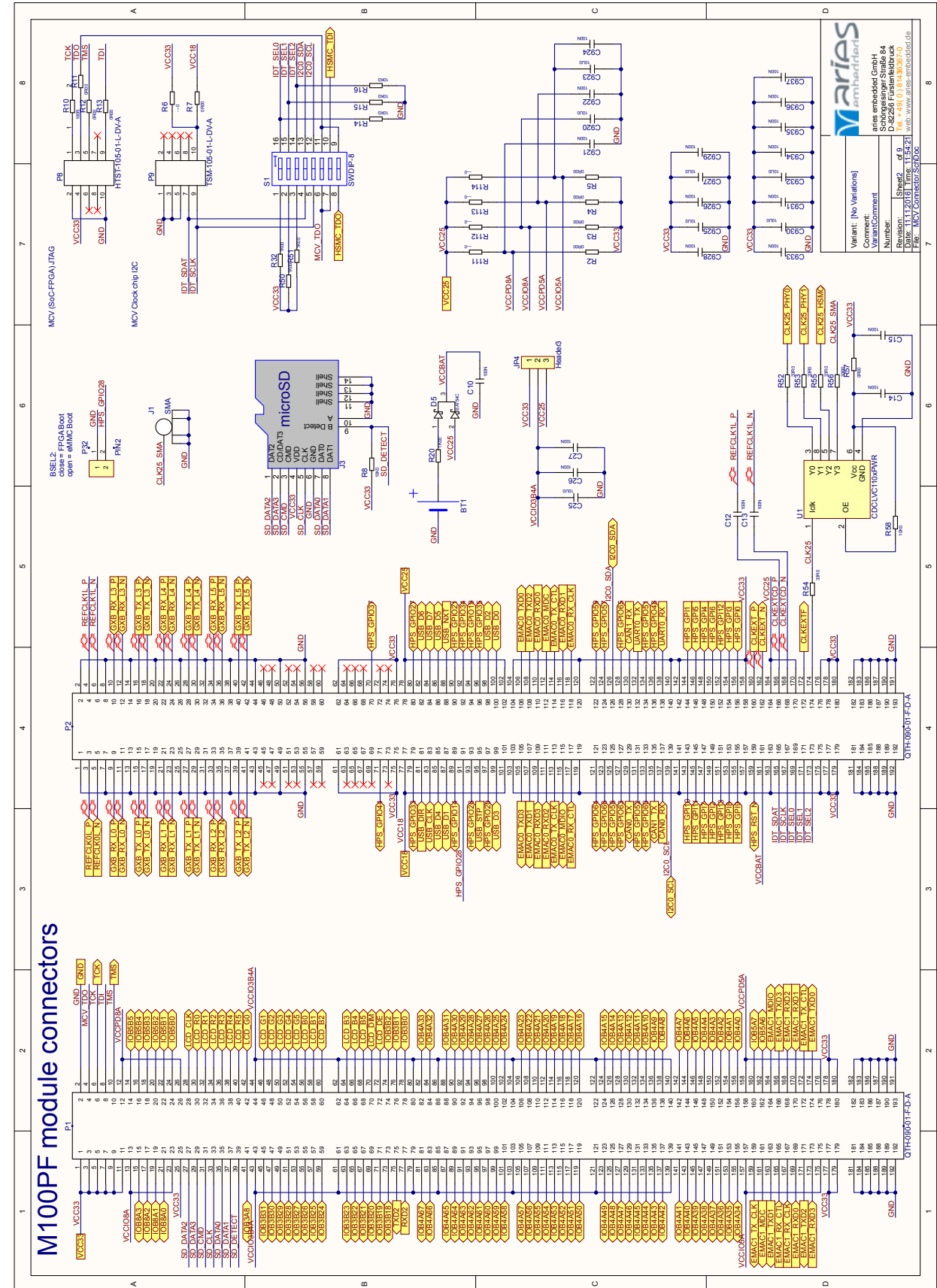
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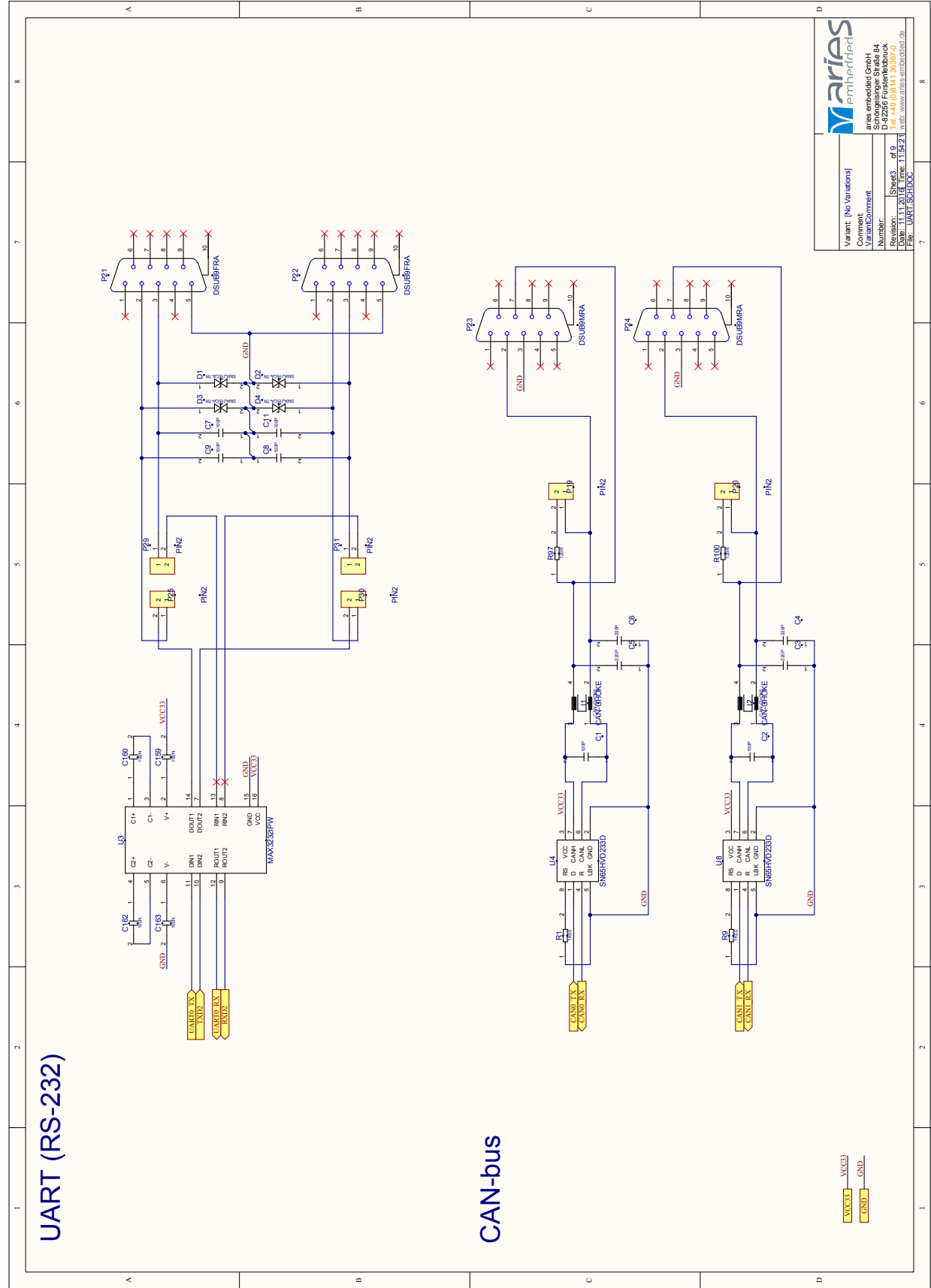
Function	FPGA Pin	Pin	Pin	FPGA Pin	Function
PIC_SDA	–	165	166	–	CLKEXT_P (*)
PIC_SCL	–	167	168	–	CLKEXT_N (*)
IDT_SEL0	–	169	170	–	2.5V (*)
IDT_SEL1	–	171	172	L5	CLKEXTF
IDT_SEL2	–	173	174	–	CLK25_3
3.3V	–	175	176	–	3.3V
3.3V	–	177	178	–	3.3V
3.3V	–	179	180	–	3.3V
Ground Plate	–	181	182	–	Ground Plate
Ground Plate	–	183	184	–	Ground Plate
Ground Plate	–	185	186	–	Ground Plate
Ground Plate	–	187	188	–	Ground Plate
Ground Plate	–	188	190	–	Ground Plate
Ground Plate	–	191	192	–	Ground Plate

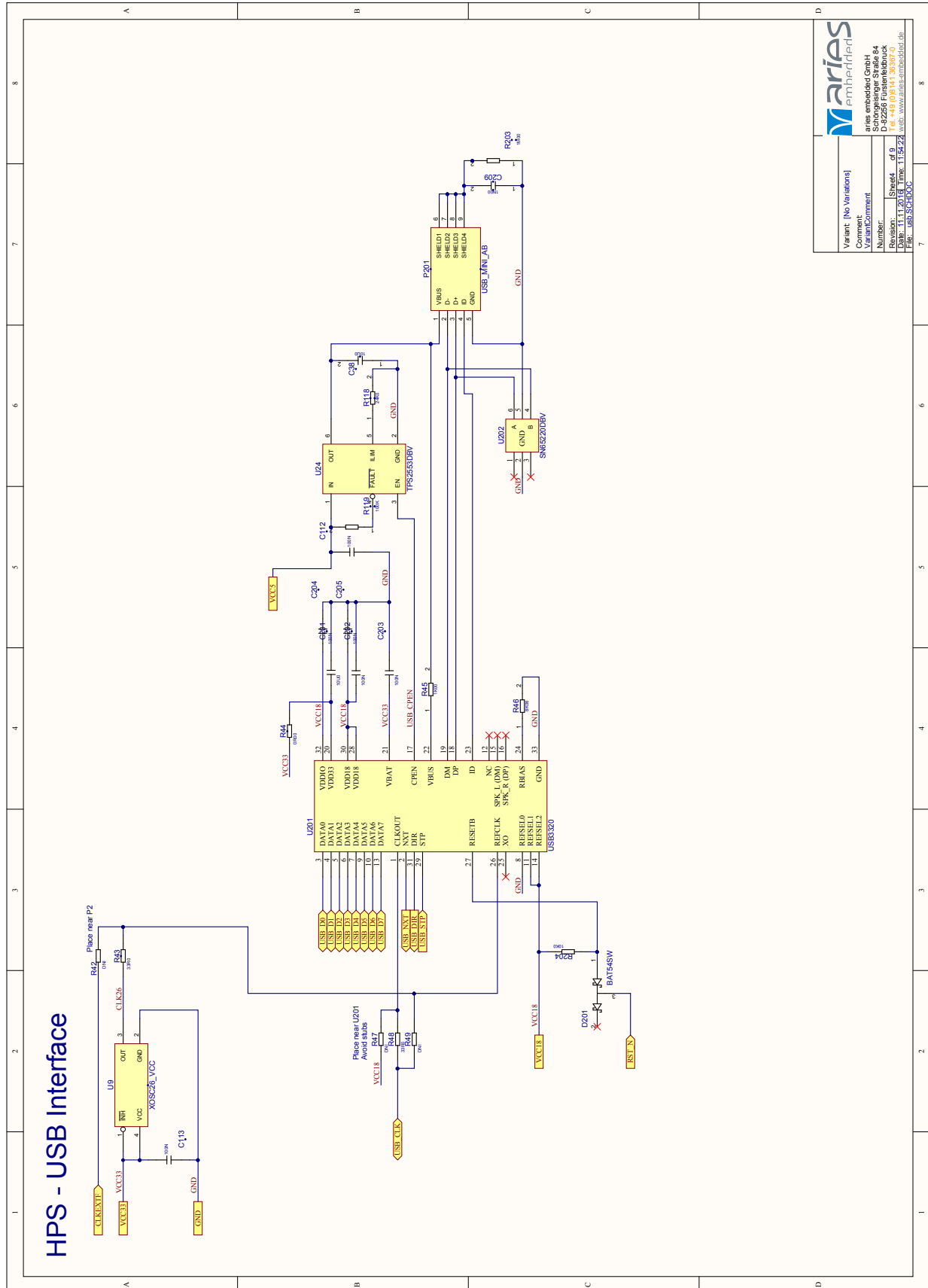
Note: Functions marked with (*) are not connected on the M100PF SoM side.

4.1 Schematics

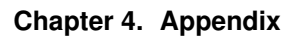
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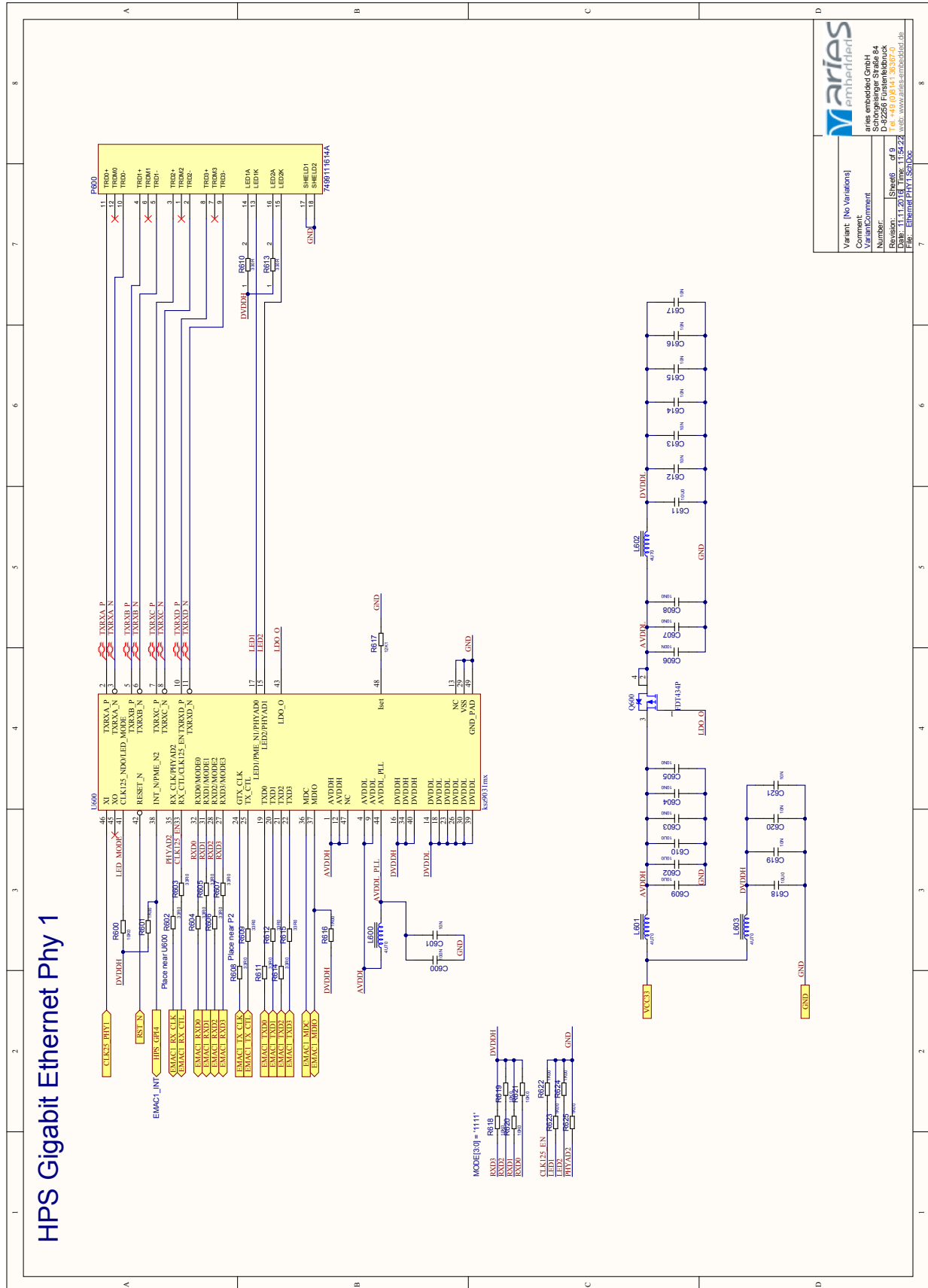




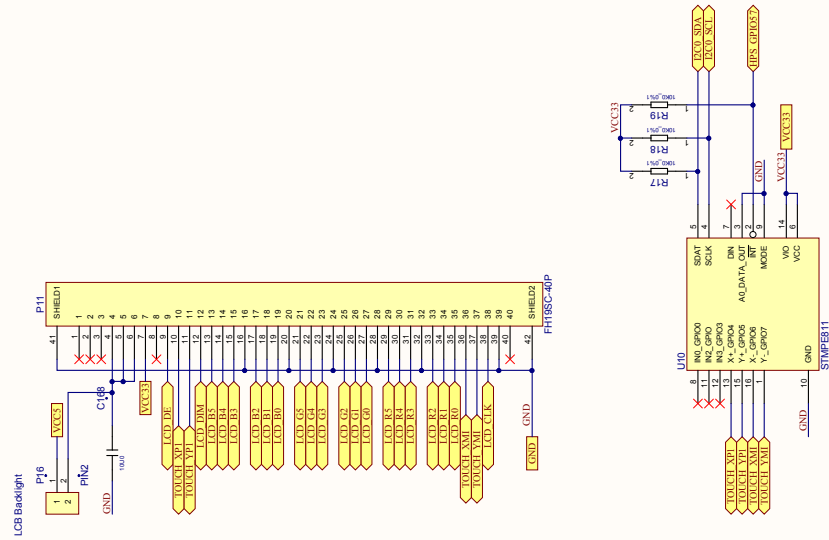
22 Chapter 4. Appendix



HPS Gigabit Ethernet Phy 1

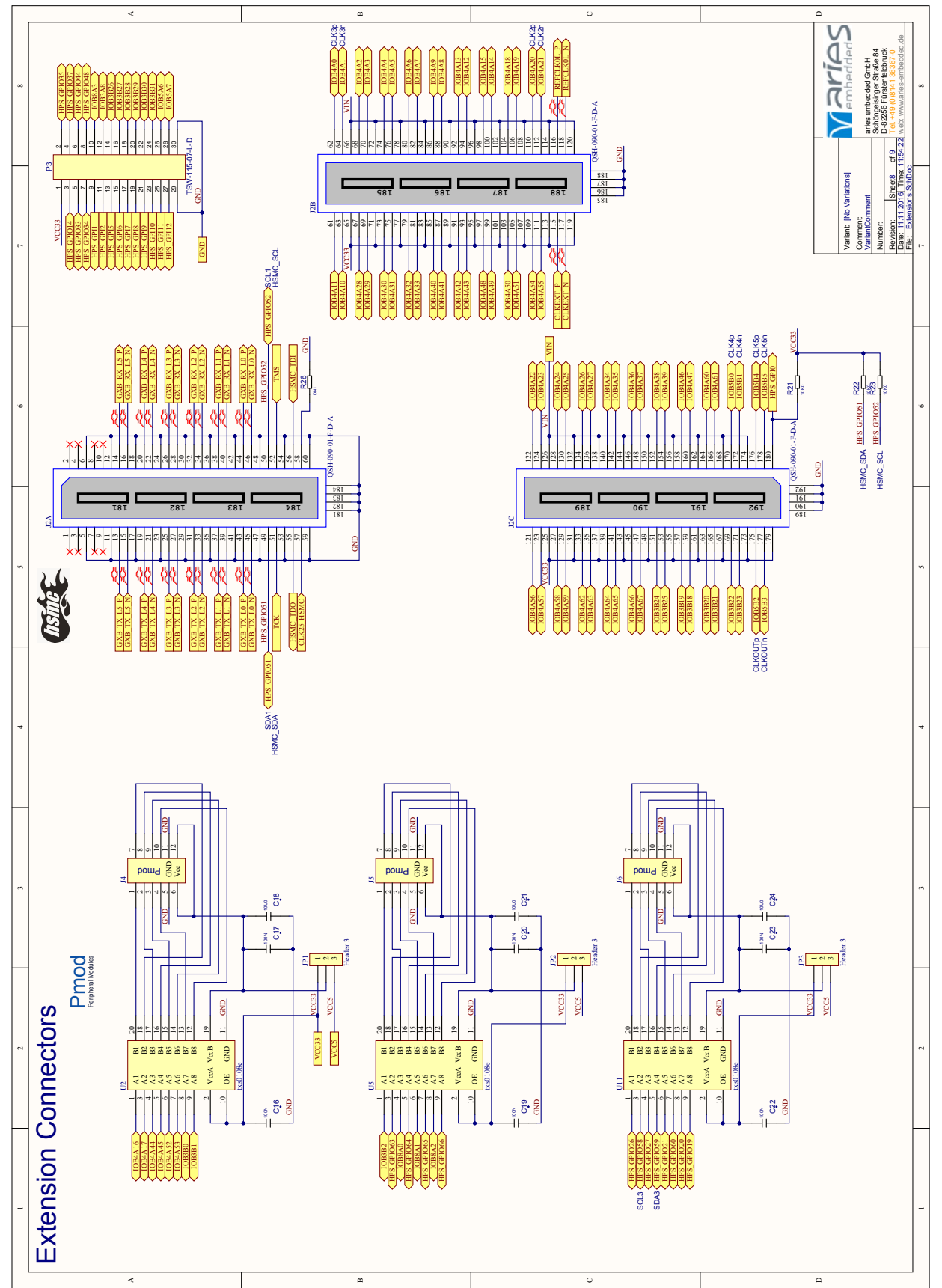


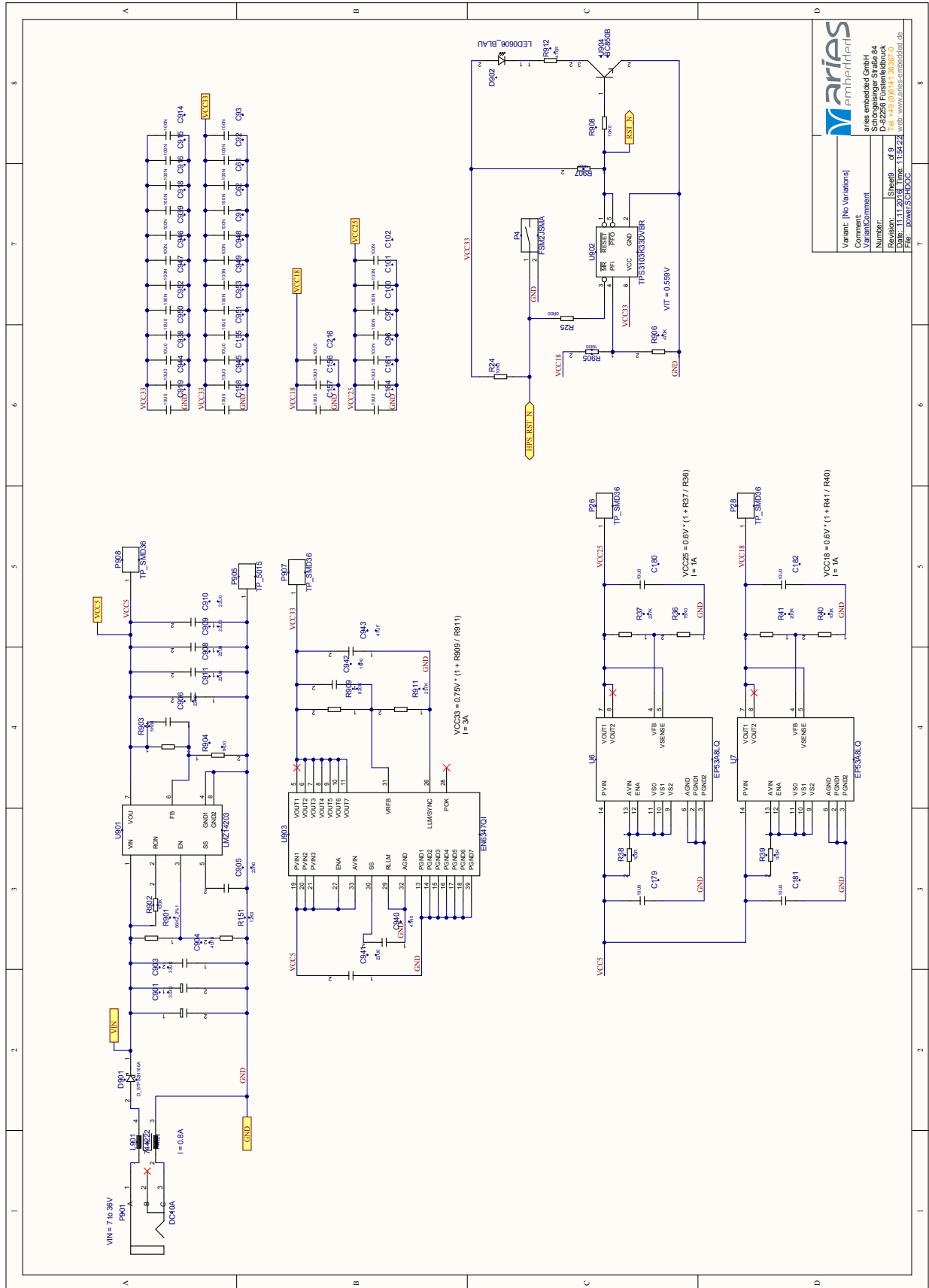
TFT Interface and Touch Controller



	 arios embedded GmbH Sprengelstraße 84 D-32207 Kalken Tel: +49 (0)9141 36307-0 web: www.arios-embedded.de
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Number:	
Revision:	Sheet 7 of 9
Date: 11.11.2018	Time: 11:54:23
File: LCD_SchDoc	

4.1. Schematics





4.2 Layout Diagram

