SLL Multiple Bus Memory Controller (MBMC) IP Installation Guide with Detailed Step-by-Step Instructions

A comprehensive guide with a large number of screen shots
Ideal for users **not** familiar with installing third party IP in Quartus

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1. Introduction

1.1 Intended Audience

This Multiple Bus Memory Controller (MBMC) IP Installation Guide provides detailed step-by-step instructions for obtaining and installing SLL Multiple Bus Memory Controller (MBMC) intellectual property (IP) into your development environment. This visually illustrated guide includes a large number of screen shots – which increases the length of the document, but makes the installation process easier and faster. This guide is ideal for users who are not familiar with Intel's process for installing third party IP in Quartus Prime. It is also suitable for users with little-to-no experience with using Quartus Prime. This guide describes how to:

1. Obtain a License Credential for SLL Multiple Bus Memory Controller IP
2. Install that License Credential into Quartus
3. Install SLL Multiple Bus Memory Controller Qsys Component

1.2 Prerequisites

All of SLL IP has been optimised for use with the Intel Qsys system integration tool. SLL IP is designed to run on the Lite and Standard editions of Quartus Prime on both Windows and Linux. Please ensure that you are running the latest version of Quartus Prime with all service packs installed. Your Quartus Prime development environment will probably need the Nios II development tools (Nios II EDS) installed. SLL IP currently supports: (a) The Mentor Graphics ModelSim*-Intel FPGA Starter Edition; and (b) ModelSim-Intel FPGA Edition software. Please contact us if you require support for other simulators.

SLL Multiple Bus Memory Controller IP currently supports a very broad range of Intel FPGA device families, including Cyclone IV, Cyclone V (SoC), Cyclone 10 LP, Cyclone 10 GX, Arria 10, MAX 10, …

2. Finding the IP license credentials and IP component

2.1 License Credential

Your IP and License bundle should contain one or more files with the following naming convention:

2-*LC-ID*.txt

Each file contains a license credential, and that license credential may contain one or more Quartus License Keys embedded within it.

This guide only describes how to install Fixed Node License Credentials.

This guide does not describe how to install Floating Node License Credentials, you will need to refer to other documentation from Intel for those License Credentials.

2.4 Qsys Component

Your IP and License bundle should contain a folder with the a naming similar to:

YYYYMMDD_sll_mbmc_vX_X_XX_*

In that folder you will find several files with **.v**, **.tcl**, and other extensions:

The **.v** file is the encrypted Verilog file containg the SLL MBMC Intellectual property (IP). It can only be used with Quartus tools. The encrypted Verilog is provided to you under a license from Synaptic Labs.

The **.tcl** file is used by Qsys for configuring the IP.

The **.ocp** file (OpenCore Plus) is present in Trial Versions of SLL's IP. The file is used by the Quartus tools to generate a time limited fully functional IP.

Section 3 below provides guidance on how to install this Qsys component.

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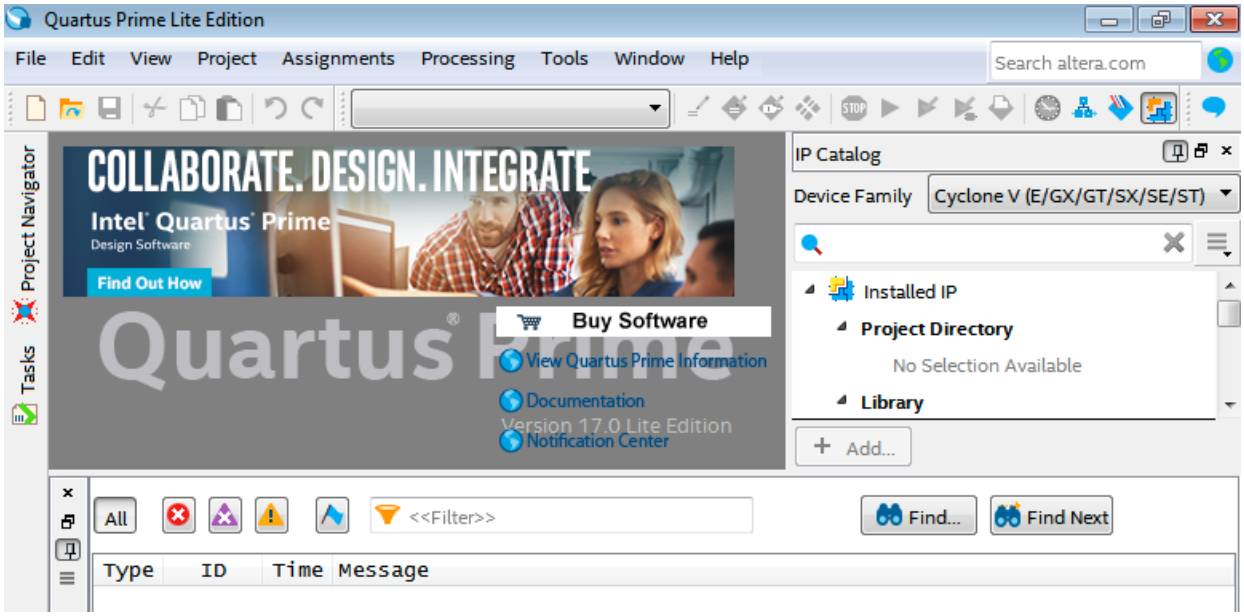
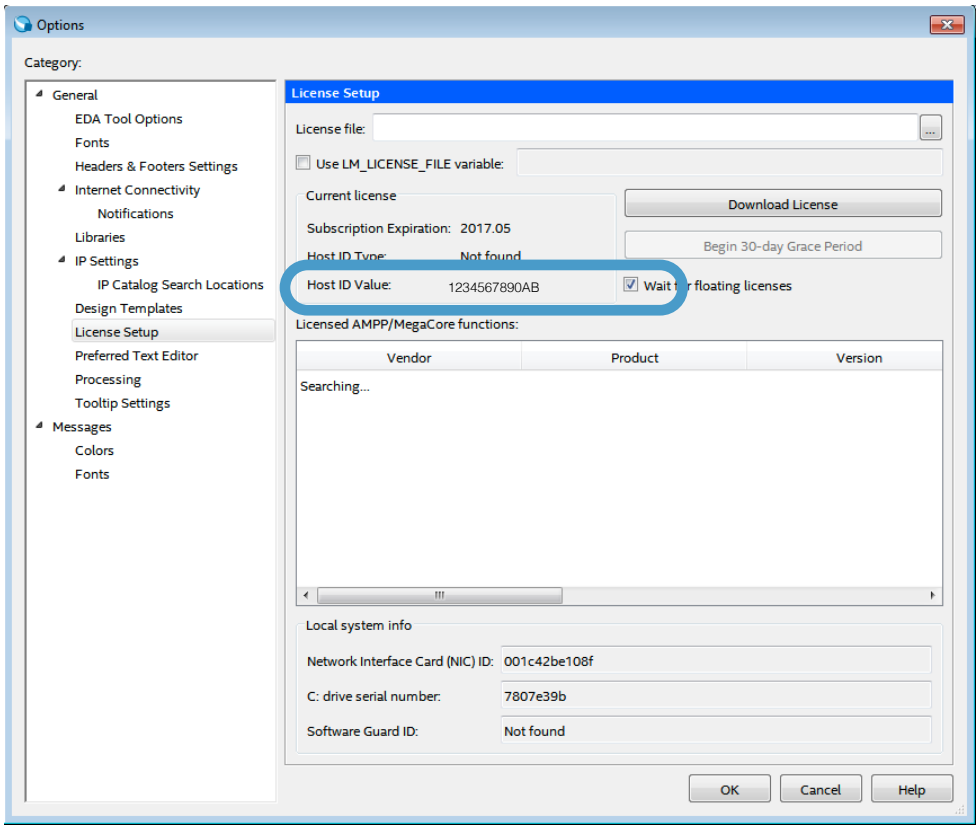
3. Installing the Fixed Node License Credential/s into Quartus

You must install the contents of one of the **2-*LC-ID*.txt** License Credential for SLL Multiple Bus Memory Controller IP into the local **Quartus License File** of Quartus Prime **before** you can successfully compile projects using that IP. Typically each License Credential is mapped to a specific Network Identification Card (NIC) Identifier (ID):

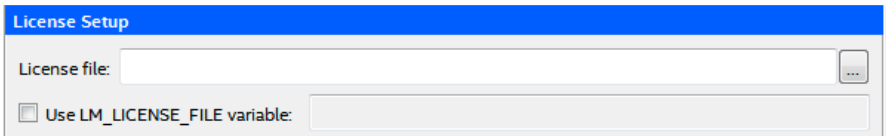
1. Open Quartus Prime



2. In the menu bar of the Quartus Prime window, click on **Tools → License Setup.** A window called "Options" will open:

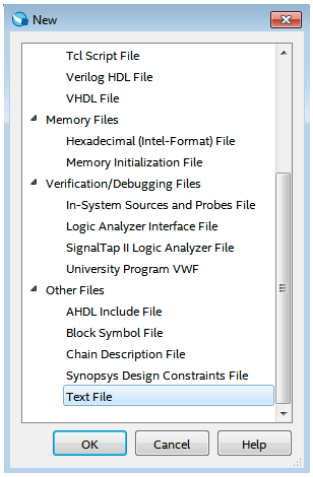


3. If the **License file:** field is empty **and** the **[ ] use LM_LICENSE_FILE variable** is not ticked (see below), then you will need to create a new .dat file to store one or more license credentials.



a. Close the “options” window by clicking the **[Cancel]** button.

b. We will now create a new empty file using Quartus Prime:



   i. Select the Quartus Prime Window.

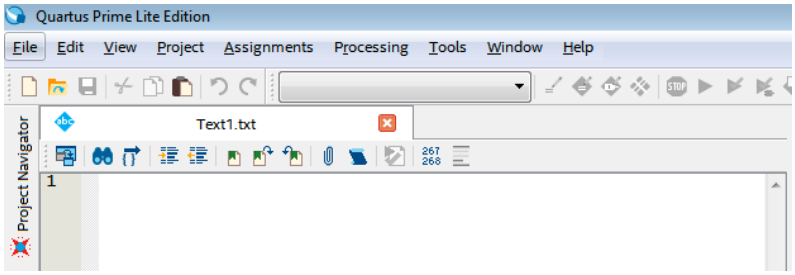
   ii. In the menu bar, click on **File → New…**

   iii. A window will pop up called “New”

   iv. Scroll down to the bottom of the list.

   v. Select “**Text File**”. Click on the **[OK]** button.

   vi. A new text file called “Text1.txt” will be created:



   vii. In the menu bar, click on **File → Save As…**

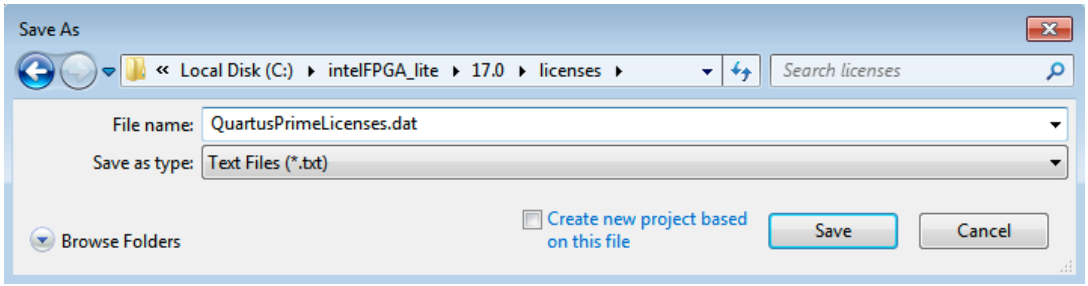
   viii. A Save as window will open.

   ix. Navigate to folder where your Intel FPGA development tools are located: **intelFPGA** or **IntelFPGA_lite**

   x. Navigate to folder corresponding with the **version** of Quartus you are running

   xi. Navigate to the **licenses** folder

   xii. In my Windows System, running Quartus Prime Lite Edition version 17.0:

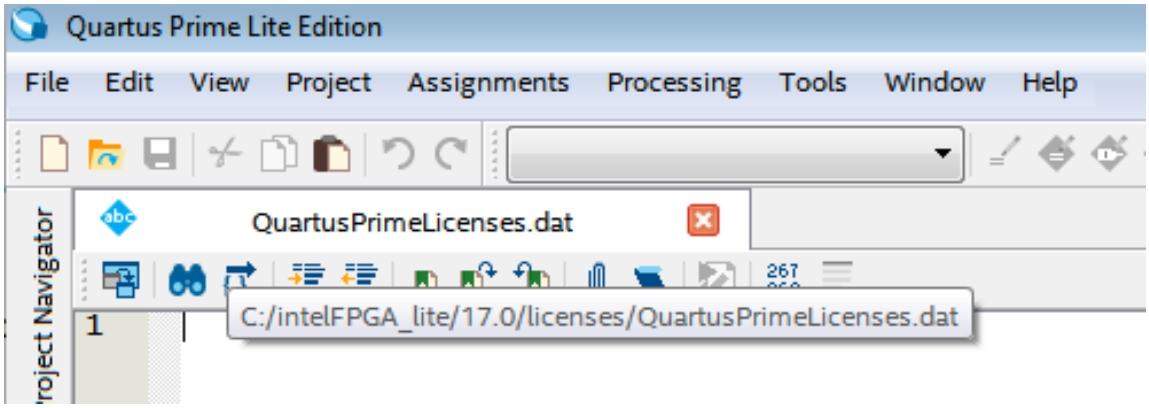


   xiii. Type in the filename: **QuartusPrimeLicenses.dat**

   xiv. Make sure **[ ] Create new project based on this file** is NOT ticked.

   xv. Click the **[Save]** Button.

xvi. Click on **[x]** button on the tab to close the empty **QuartusPrimeLicenses.dat** file

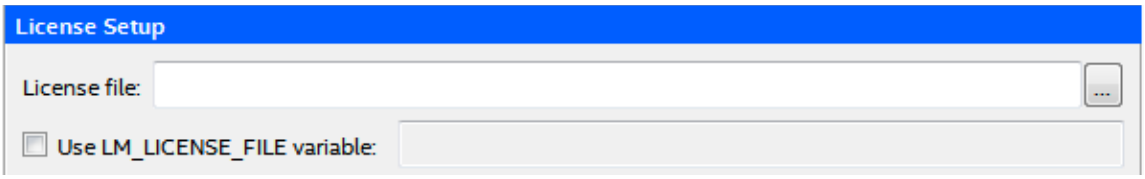


c. We now need to set the **QuartusPrimeLicenses.dat** file as our license file.

i. In the menu bar of the Quartus Prime window, click on **Tools → License Setup**

ii. A window called “Options” will open

iii. Click on the **[…]** button next to the **Licenses file:** field (illustrated below to the right)



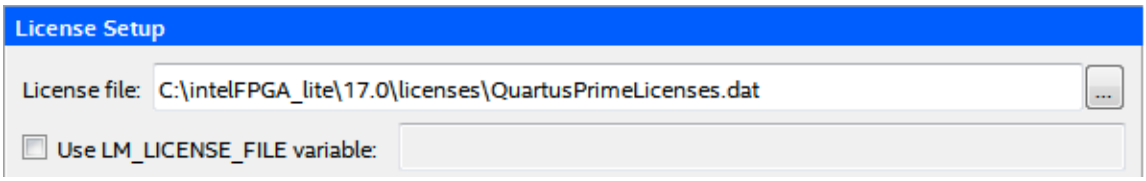
iv. A select file window will open.

v. Navigate to where you saved the **QuartusPrimeLicenses.dat** file**.**

vi. Select the **QuartusPrimeLicenses.dat** file.

vii. Click the **[OPEN]** button

viii. The path of your **QuartusPrimeLicenses.dat** file displayed in the **License file:** field



ix. Ensure that the **[ ] LM_LICENSE_FILE variable:** field is not ticked.

x. Click the **[OK]** button at the bottom right of the “Options” window to **SAVE** the changes.

xi. You are now ready to install the license credentials into the **.dat** file.

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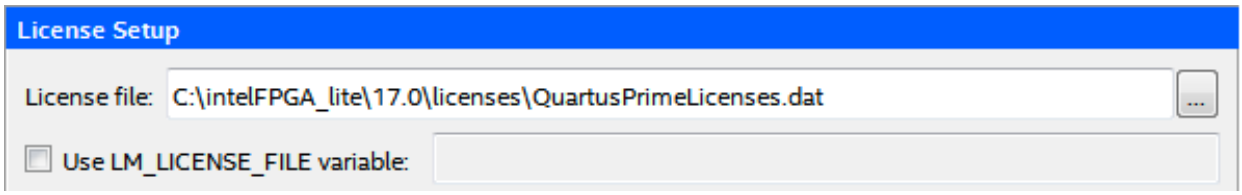
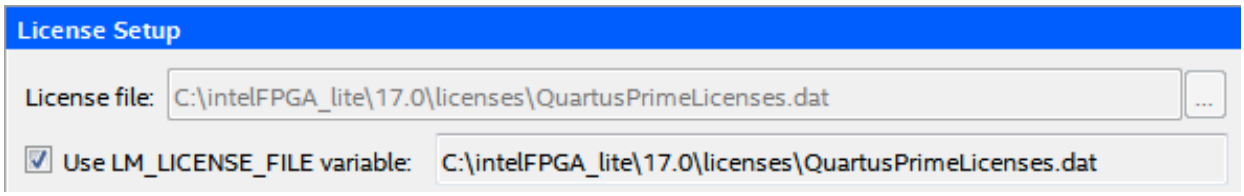
4. We now want to open the license file used by Quartus Prime to install your credentials.

   In my system, the license file appears as below:



   Alternatively, if your system has already been configured to use licenses, your screen might look like:

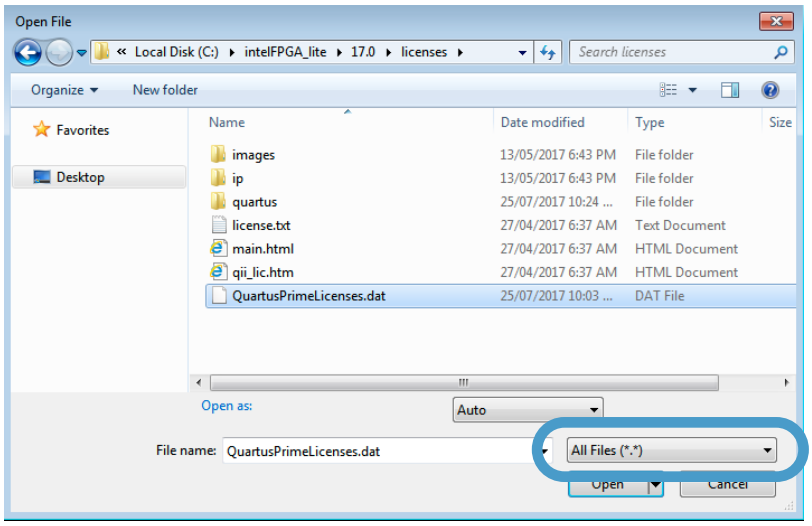


   a. We will now want to open that **.dat** license file for editing using the Quartus Prime Text Editor.

      i. Select the Quartus Prime Window

      ii. In the menu bar, click on **File → Open…**

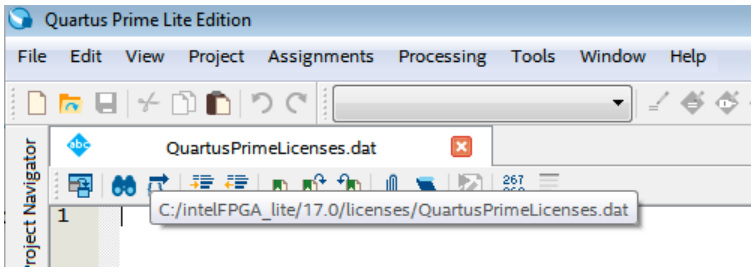
      iii. Ensure that **[All Files (*.*) V]** is selected so that you can see the **.dat** file



      iv. Select the .dat file

      v. Click the **[Open]** button.

      vi. The .dat file is now ready for editing



e. Find the credential you want to install that your received in your email. It will look something like this:

```
# == START OF LICENCE CREDENTIAL WITH EMBEDDED QUARTUS LICENSE KEY ==
#
…
#
# == END OF LICENCE CREDENTIAL WITH EMBEDDED QUARTUS LICENSE KEY ==
```

f. Copy-and-paste the contents of that credential (including the start and end lines) and paste it at the end of the **QuartusPrimeLicenses.dat** file.

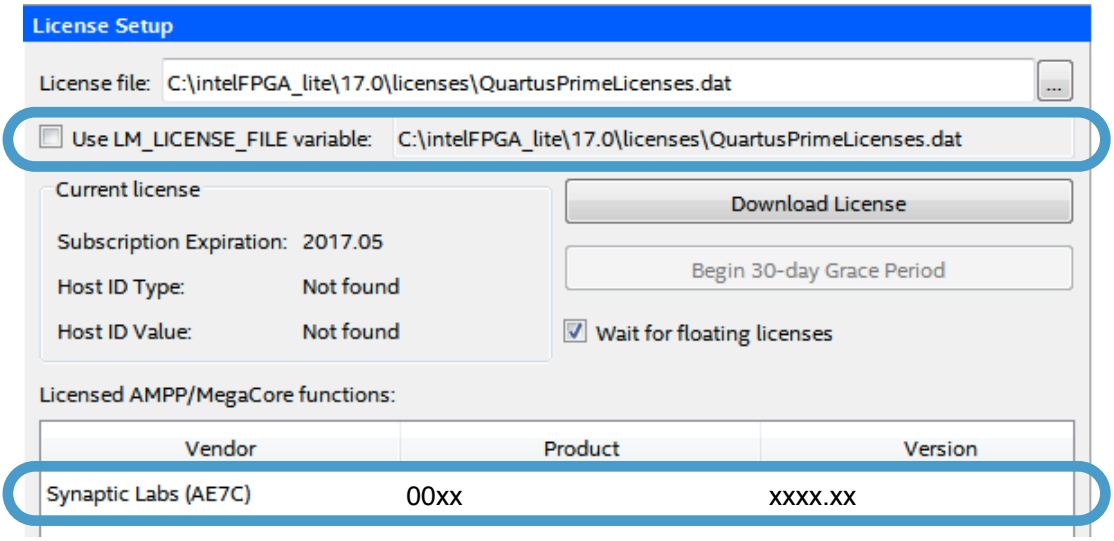
g. Save the **QuartusPrimeLicenses.dat** file.

h. Check that the credential is installed correctly:

   i. In the menu bar of the Quartus Prime window, click on **Tools → License Setup**

   ii. A window called “Options” will open

   iii. You should now be able to see **Synaptic Labs (AE7C)** credential installed in the list of **Licensed AMPP/MegaCore functions.**
   It will look something like what is illustrated below:



4. Installation of SLL MBMC Qsys component

4.1 There are 3 types of way third party Qsys components can be installed

There are 3 types of way third party Qsys components can be installed into the Quartus Prime development environment:

1. Inside each Quartus Project,
   for use just by that Quartus Project
   e.g.
   c:\myQuartusProject\ip\a_qsys_component

2. Inside the IP folder of the Quartus installation,
   for use by all Quartus Projects opened by that version of Quartus
   e.g.
   c:\intelFPGA\xx.x\ip\vendor_name\a_component
   or
   c:\intelFPGA_lite\xx.x\ip\vendor_name\a_qsys_component

3. Inside a user selected shared folder, and
   then configure Quartus Prime and/or Qsys to search for IP in that shared folder
   e.g.
   c:\mySharedIpFolder\vendor\a_qsys_component

SLL strongly recommends installing our IP into each Quartus Project as described in section 4.2 below.

4.2 Installing SLL IP into each Quartus project (Recommended)

SLL strongly recommends installing our IP into each Quartus Project (particularly for organisations concerned about change management):

1. Create a Quartus project
   e.g.
   c:\myQuartusProject

2. Create an **IP** folder in the quartus project
   e.g.
   c:\myQuartusProject\ip

3. Copy the folder containing the version of SLL IP you want into that **IP** folder

4. Restart Quartus Prime.

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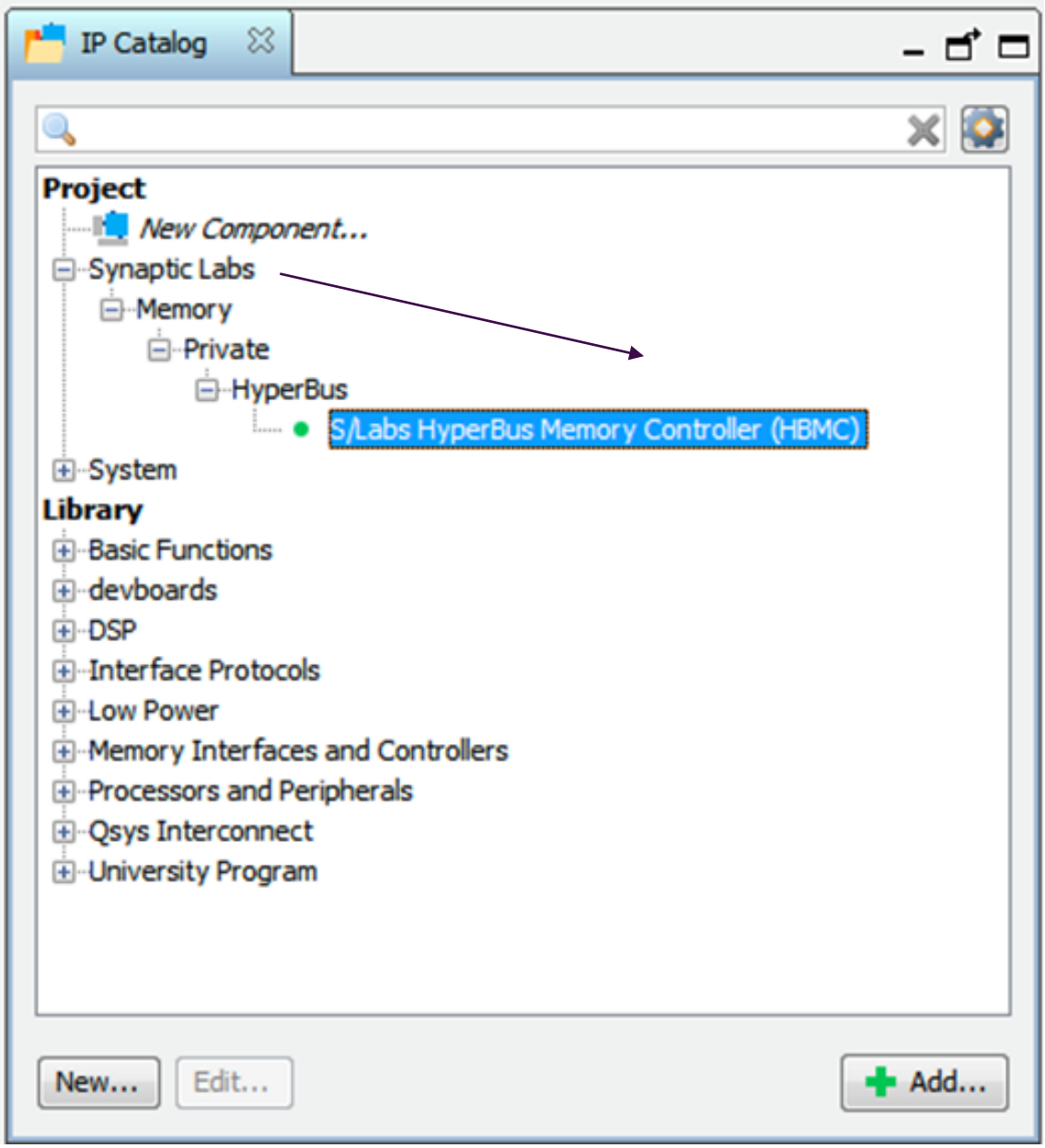
5. SLL IP will now be visible in the **IP Catalog** window under the **Project** folder:



Please note, updating SLL IP in that Quartus Project folder, will only update Synaptic Labs IP for **that specific** Quartus Prime project. This approach makes change control much easier.

A WARNING FOR ADVANCED USERS

When copying SLL Multiple Bus Memory Controller IP directly in the Quartus project folder, ensure that none of the IP search paths in the Quartus or Qsys environment point to a different copy of this IP.

Open Qsys. On the menu bar click **Tools→Options**.
Ensure that the IP search path does not point to a previously installed MBMC IP.

You then need to repeat this process in Quartus. Open Quartus. On the menu bar click **Tools→Options**.
In **Category**, Select **General** / **IP Settings** / **IP Catalog Search Locations**.
Ensure that none of the IP search paths point to a previously installed MBMC IP.

Also ensure SLL IP is not installed in the IP folder located in the Intel FPGA installation directory.
e.g.
\intelFPGA\17.0\ip*

4.3 Installing SLL IP into the IP folder of the Quartus installation

Some organisations prefer to keep the latest version of third party IP's stored in the Quartus installation directory. This is similar to the way that Intel keeps the latest version of Intel's Qsys components that are bundled with Quartus in that installation directory. If you chose to install SLL IP in the Quartus installation directory, we recommend ensuring the latest version of SLL IP is always used in that folder:

1. Locate the IP folder of your Quartus Prime installation.
   e.g.
   - **C:\intelFPGA_lite\xx.x\ip**
   - **C:\intelFPGA\xx.x\ip**
2. Create a sub folder called **SynapticLabs**
   e.g.
   - **C:\intelFPGA_lite\xx.x\ip\SynapticLabs**
3. Copy the folder containing the latest version of SLL IP into that **SynapticLabs** folder
4. Restart Quartus Prime

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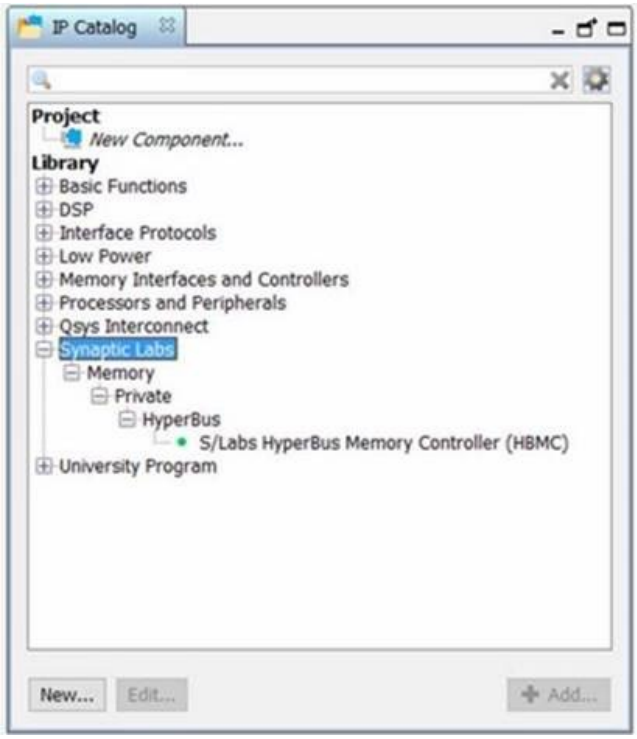
5. SLL IP will now be visible in the **IP Catalog** window under the **Library** folder:



Please note, in this example, updating SLL IP in the **c:\mySharedIpFolder\SynapticLabs** folder, will implicitly update Synaptic Labs IP for **every** Quartus Prime project that runs in any version of Quartus Prime that uses that shared folder.

A WARNING FOR ADVANCED USERS

When copying SLL Multiple Bus Memory Controller IP directly in the Quartus project folder, ensure that none of the IP search paths in the Quartus or Qsys environment point to a different copy of this IP. The easiest way to ensure this is to avoid using the installation processes described in section 3.4 and 3.5 below.

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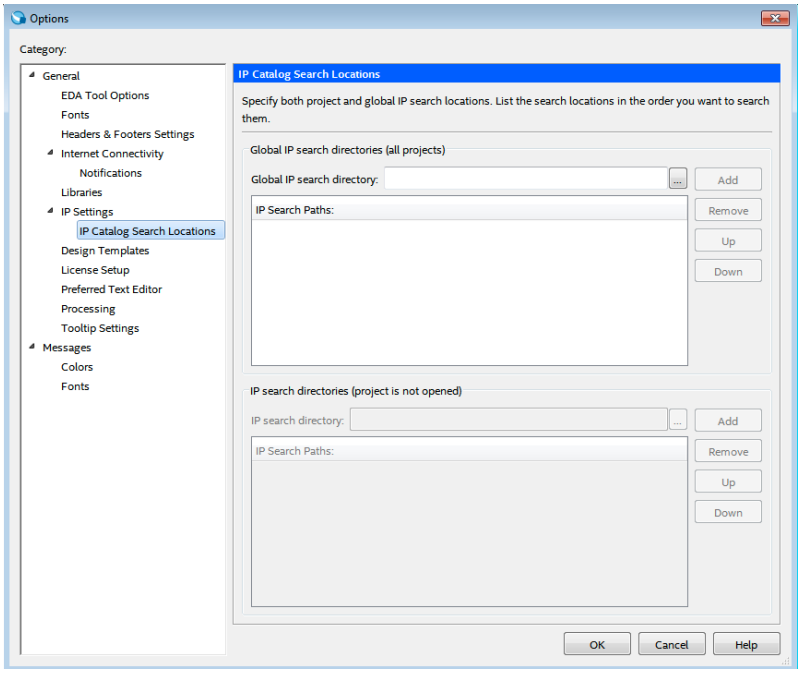
4.4 Installing SLL IP into a shared folder

If you chose to install SLL IP into a shared folder and then reference that folder using one of the Quartus Prime or Qsys IP Catalog Search environment settings, we recommend ensuring the latest version of SLL IP is always used in that folder. Please note, this search based approach is harder to manage. **Please ensure that SLL IP is ONLY located ONCE in the search paths of Quartus and Qsys.**

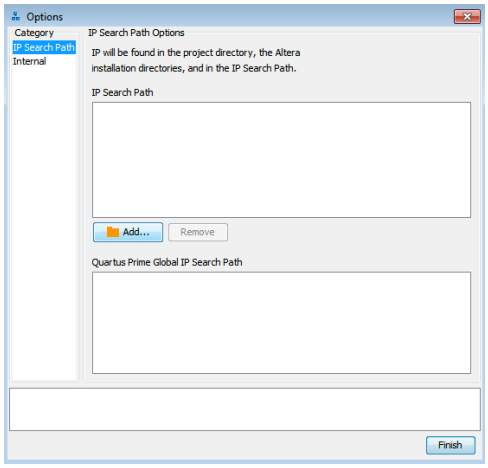
When using this approach, ensure the latest version of SLL IP is used:

1. Create a folder to share third party IP within your system.
   e.g.
   c:\mySharedIpFolder
2. Create a sub folder called **SynapticLabs**
   e.g.
   c:\mySharedIpFolder\SynapticLabs
3. Copy the folder containing the latest version of SLL IP into that **SynapticLabs** folder
4. Optionally install in the search paths of Quartus Prime
   a. Open Quartus
   b. In the menu bar, click on **Tools→Options**
   c. A window called “Options” opens
   d. Select General / IP Settings / IP Catalog Search Locations



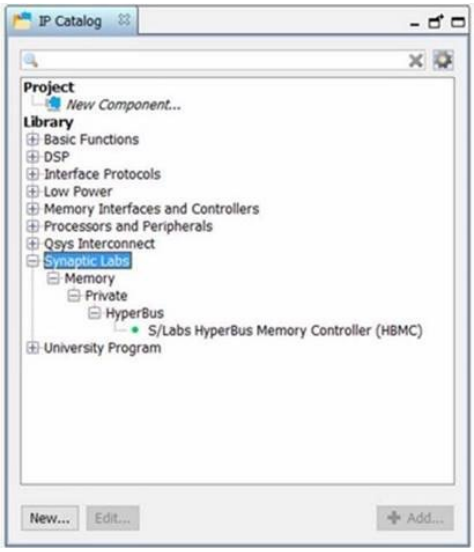
   e. You can now **[Add]** the search folder to either:
      - The “**Global IP Search Directories**” which will then be used by all Quartus Projects; or
      - The “**IP Search directories**” which will be used only for the current Quartus project.

5. Optionally install in the search paths of Qsys
    a. Open a Quartus Project
    b. Open a Qsys Project found within that Quartus Project
    c. In the menu bar of Qsys, click on **Tools→Options…**
    d. A window called “Options” opens



    e. You can now **[Add…]** the search folder to the **IP Search Path** used by this Qsys component.

6. SLL IP will be listed in the **IP Catalog** window under the **Library** folder:



Please note, updating SLL IP in the **c:\mySharedIpFolder\SynapticLabs** folder, will implicitly update any Quartus Project or Qsys Project that references that IP.

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5. Instantiating SLL MBMC IP in the Qsys environment

SLL Hyperbus Memory Controller IP can be found in the
Qsys **IP Catalog** panel under:

Project

+ Synaptic Labs
  + Memory
    +HyperBus
      - SLL Multiple Bus Memory Controller

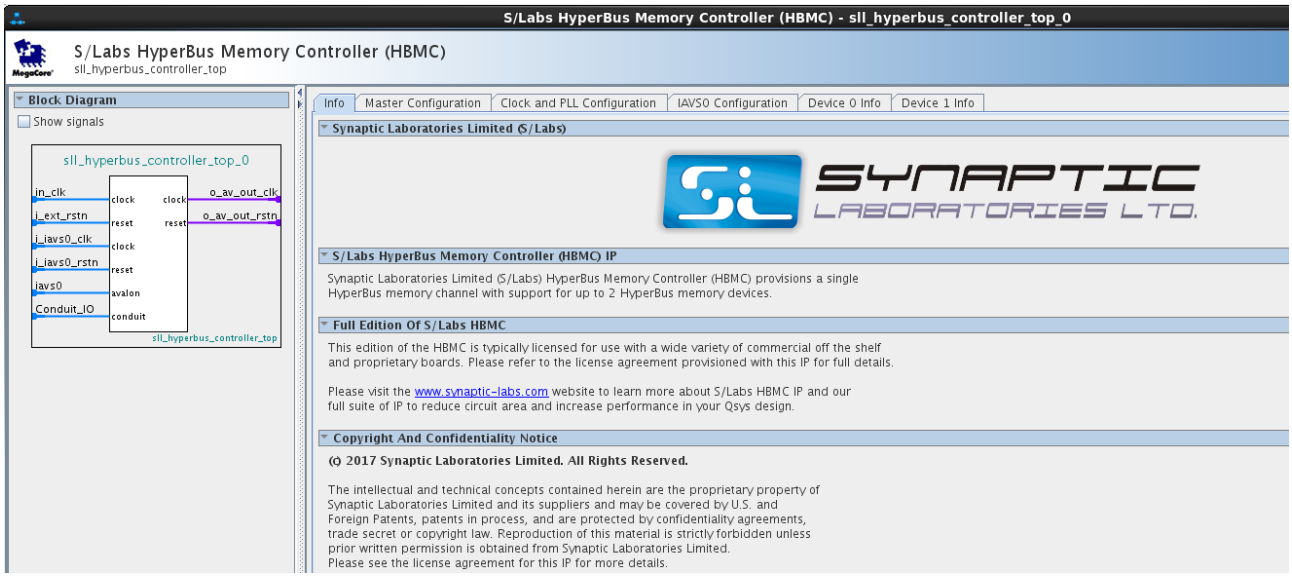
or

SLL Hyperbus Memory Controller IP can be found in the
Qsys **IP Catalog** panel under:

Library

+ Synaptic Labs
  + Memory
    +HyperBus
      - SLL Multiple Bus Memory Controller

Warning:
SLL MBMC IP should only be visible under the **Project** folder or the **Library** folder, not both folders.



Finding SLL Hyper Memory Controller IP in the Qsys IP Catalog

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6. Next steps

We strongly recommend that you proceed to study one of the many excellent tutorials available for SLL Multiple Bus Memory Controller IP available on the Intel Design Cloud. These tutorials offer the best place to start your own project from.

SLL has published at least two detailed tutorials for Basic Edition of our Multiple Bus Memory Controller IP. Each tutorial has 1 or more parts that build on each other. You can find these tutorials on the Intel Design Cloud, and the link above.

★ **SLL Tutorial 1 (T001) for SLL Multiple Bus Memory Controller IP**

- "T001A: Qsys based Nios II reference design with a simple self test of the HyperFlash and HyperRAM device using SLL MBMC IP"

- "T001B: A Qsys based Nios II reference design with a simple Memory Bandwidth Benchmark of the HyperRAM device using SLL MBMC IP"

★ **SLL Tutorial 2 (T002) for SLL Multiple Bus Memory Controller IP**

- "T002A: A Qsys based Nios II reference design using Intel's MSGDMA to benchmark memory copy operations on the HyperRAM device using SLL MBMC IP"

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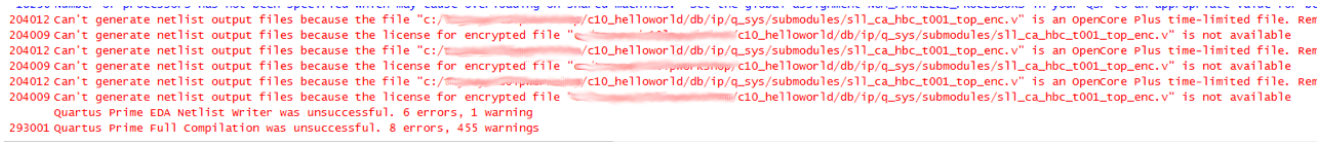
7. Fixing Quartus Prime Error Messages

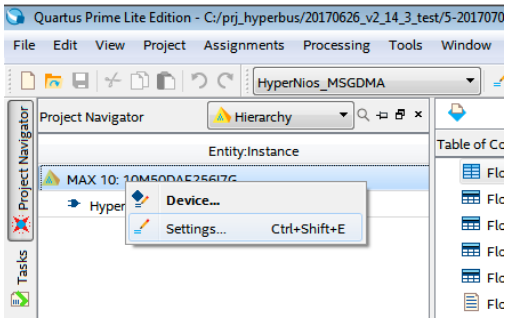
Sometimes Quartus Prime generates errors that are not very easy to understand. This section is dedicated to describing some of the error messages you may see, provide an explanation for those error messages, and offer a solution for fixing that problem in your Quartus setup.

7.1 Netlist Generation Error Messages in Quartus

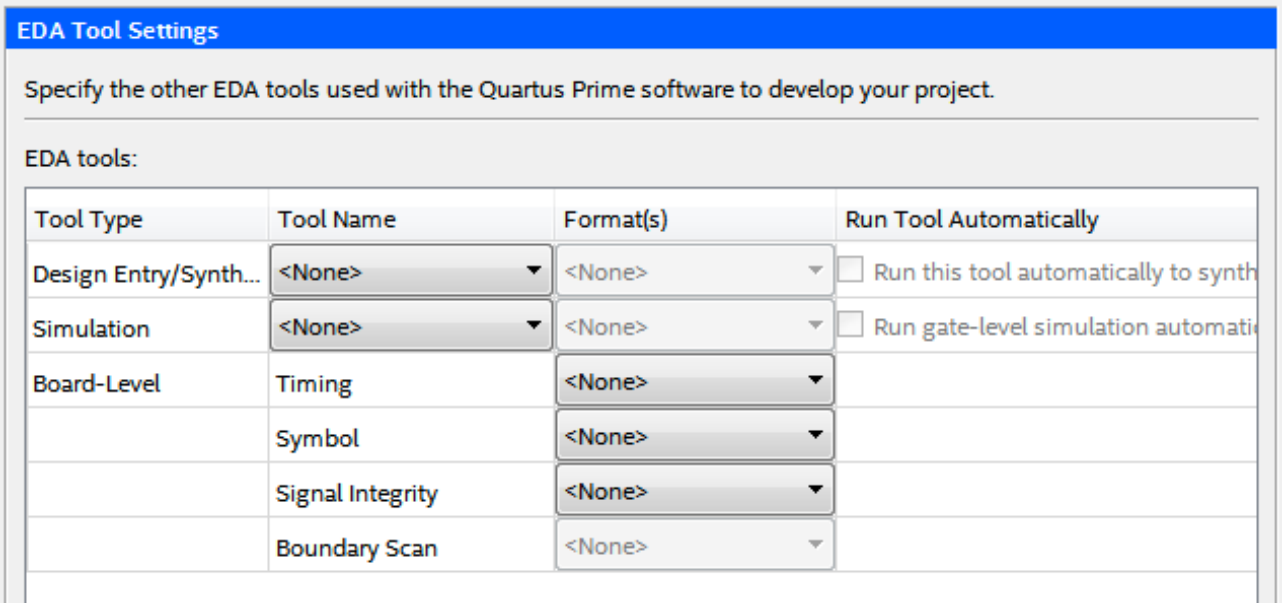
The open core edition of Synaptic Labs' MBMC IP license does not support netlist generation in Quartus Prime. Figure 4 shows a typical error message issued by Quartus Prime during compilation when netlist generation is enabled.



You can disable netlist generation in your Qsys project to stop this error occurring when compiling that Qsys project by executing the following steps.



1. Go to the Quartus Prime window.
2. In the project Navigator tab, **right click** on the FPGA device (MAX 10, Cyclone 10 LP, …)
3. Select "**Settings…**"
4. In the category panel of the settings window, select "**EDA Tool Settings**".
5. On your screen you will probably see that the "**Simulation**" field has been set to **ModelSim-Intel**.
6. Set the value of the "**Simulation**" field to **<None>** .



7. Then click the **[Apply]** button. This will then disable netlist generation during compilation. This will remove the error messages so they do not occur in the reference project(s) you create.

7.2 Quartus Error (10170)

Problem:

Error (10170): Verilog HDL syntax error at sll_ca_hbc_t001_top_enc.v(1) near text: . Check for and fix any syntax errors that appear immediately before or at the specified keyword. The Intel FPGA Knowledge Database contains many articles with specific details on how to resolve this error. Visit the Knowledge Database at https://www.altera.com/support/support-resources/knowledge-base/search.html and search for this specific error message number.

Reason:

You have previously installed an old version of our license and IP.
You have installed a new version of our IP which in this case requires a new license.
In this case, the old version of our IP and the new version of our IP are encrypted using different secret keys.

Solution:

You must delete the **old** credential for this IP out of the .dat file that contains the licenses used by Quartus. See Appendix A below.

Then re-install SLL credential for your computer following each of the steps in section "**3. Installing the .dat License into Quartus**" carefully.