MSMP1 Hardware Manual

Version: **2.2**

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CONTENTS:

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	13.07.2022	dk	Initial creation
2.0	28.04.2023	wa	Updating STMP1 to STM32MP1, ST Microelectronics to STMicroelectronics
2.1	23.05.2023	aw	Correcting typos for table 3.8.10 MSMP1 SiP Pads • SIP Pad Y7 • SIP Pad AA6
2.2	06.03.2024	aw	• USB intefaces exchanged, interfaces are now compliant with OSM standard • Inserted chapter 3 with additional information on the OSM standard • minor changes
3.0	15.01.2025	fn	Contact table 4.2.17.3 • Updating SDIO • Updating individual pins • Deleting unconnected functions in table (MIPI CSI, PCIe, eDP/eDP++, UFS)
3.1	12.02.2025	fn	Adding the interface conversion via OSMEVK_ADAP_MSMP1
3.2	29.04.2025	fn	Changing supply voltage and adding OSM-standard voltage
4.0	22.05.2025	fn	Changing LPDDR3 to DDR3L RAM • Upgrading fotos of MSMP1 (Cover, block diagram, part overview, dimensions, handling recommendations) • Changing signals for table 4.1.2.1 • Changing order codes and feature set • Changing schematics (4.4)

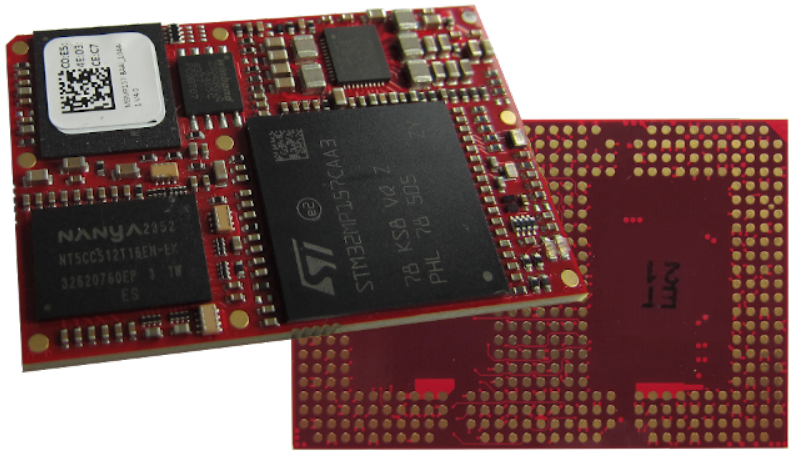
CHAPTER

TWO

OVERVIEW

2.1 MSMP1 Microprocessor SiP

The MSMP1 is the Open Standard Module compliant System-In-Package based on STMicroelectronics STM32MP1 Family architecture offering high-performance single/dual CortexA7 cores in combination with a CortexM4 core. The MSMP1 combines compact design and a wide range of services, bringing low power consumption, thermal efficiency and low-cost to embedded systems.



MSMP1 fits to an OSM size M SoM in a size of only 30x45mm. Due to its 476 contacts the SoM offer the CPU almost transparently so that it can be used almost without functional restrictions due to the pin-multiplexing of the CPU.

2.2 Feature Set

- **STM32MP1 (STMicroelectronics)**
  - Single/Dual Cortex-A7, up to 800MHz
  - Cortex-M4, up to 209MHz
- 512MB – 1GB DDR3L RAM
- 4GB – 64GB eMMC NAND Flash
- 10/100/1000MBit Ethernet
- USB2.0 Host/OTG
- 2x CAN
- UART, I2C, SPI
- ADC, DAC
- Parallel display port
- Camera interface
- compliant to the SGET OSM standard
- size M, 30x45mm
- 476 contacts
- 0°C..+70°C commercial temperature range
- -30°C..+85°C industrial temperature range

2.3 Order Codes

The MSMP1 SoM is available in the following standard configurations:

- **MSMP151-A0C**
  - STM32MP151
  - 512MB DDR3L RAM
  - no eMMC
  - 512MBit SPI NOR
  - 0°C...+70°C
- **MSMP157-BAA**
  - STM32MP157
  - 1GByte DDR3L RAM
  - 4GB eMMC
  - 128MBit SPI NOR
  - 0°C...+70°C

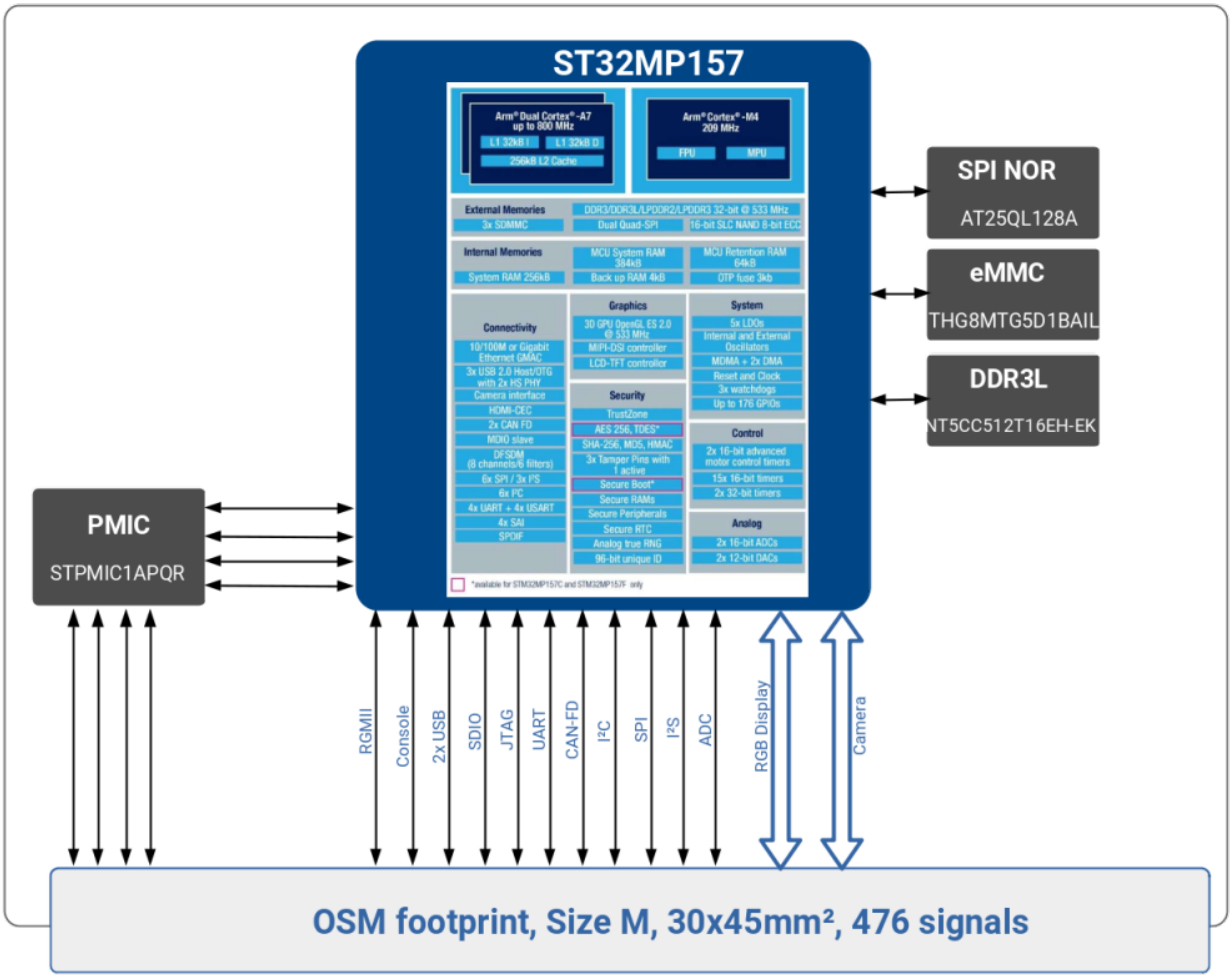
Additionally, depending on the installed PMIC, the MSMP1 is available in variants that support either 1.8V or 3.3V I/O voltage.

PMIC Derivatives

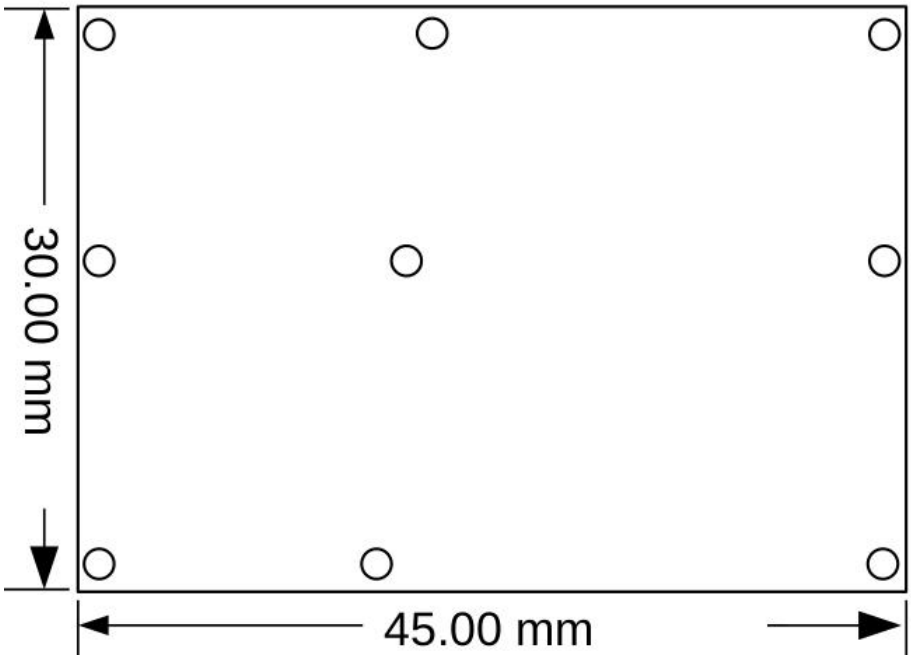
Device	I/O Voltage	Comment
STPMIC1A	3.3V	Standard
STPMIC1B	1.8V	

Please contact ARIES Embedded under sales@aries-embeded.de for more information about the availability of other standard products of MSMP1 or custom configurations.

2.4 Block Diagram

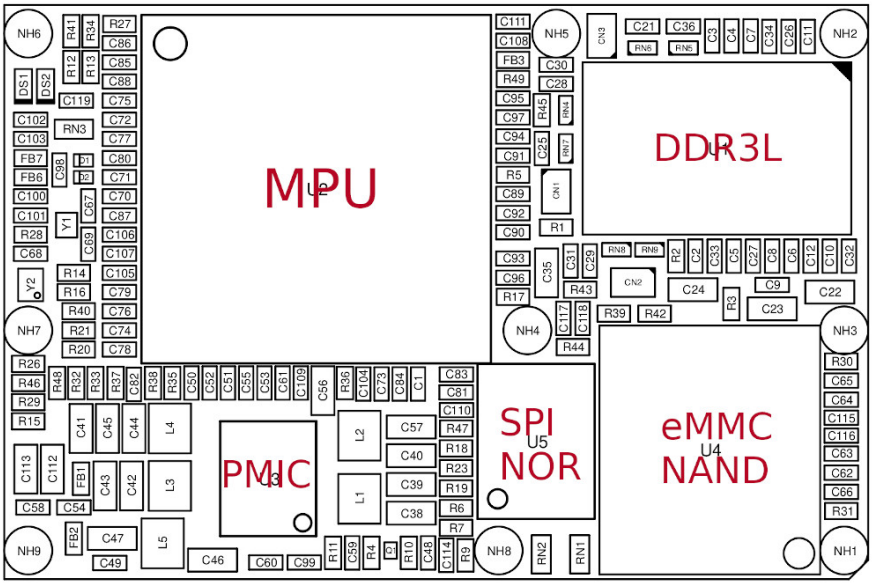


2.5 Dimensions

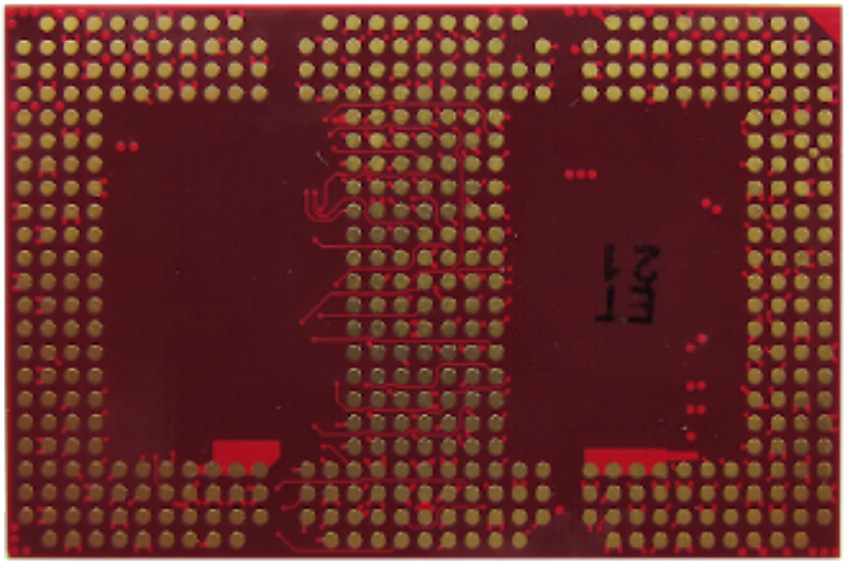


2.6 Part Overview

Assembly Top

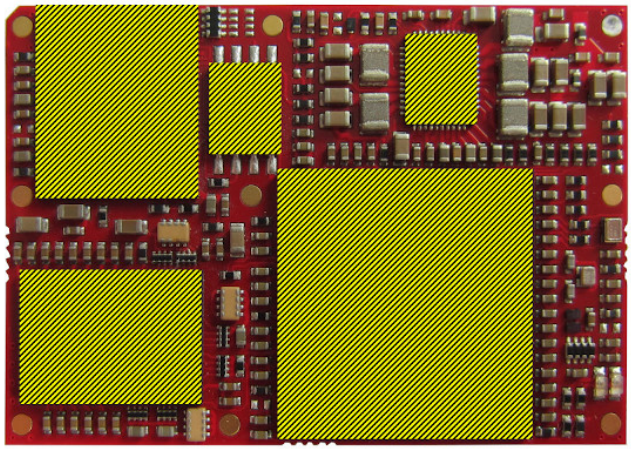


Assembly Bottom



2.7 Handling Recommendations

To avoid mechanical damage to the components populated on MSMP1 it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

OPEN STANDARD MODUL (OSM)

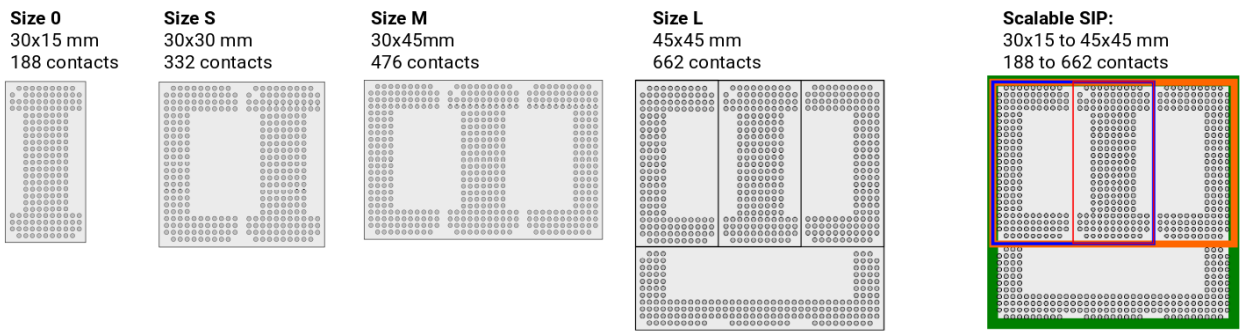
The idea of all Open Standard Modules™ is to create a new, future proof and versatile standard for small-size, low-cost embedded computer modules, combining the following key characteristics:

- Completely machine processible during soldering, assembly and testing
- Pre-tinned LGA package for direct PCB soldering without connector
- Pre-defined soft- and hardware interfaces
- Open-Source in soft- and hardware

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

3.1 Module Sizes and Dimensions

OSM SoMs are highly scalable in size, performance and functionality as they are available in different mechanical sizes and contact count:



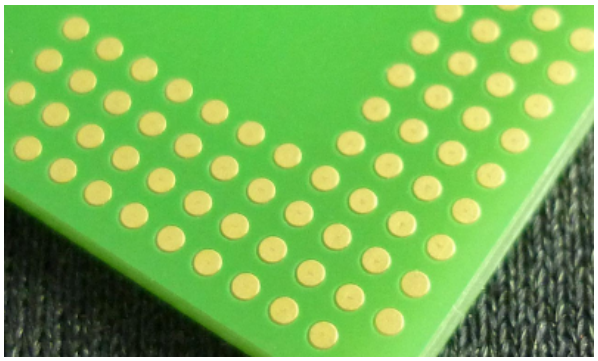
Size	Metrics	Contact Count	Colour Outline
Size-0 – “Zero”	30 mm x 15 mm	188 contacts	red
Size-S – “Small”	30 mm x 30 mm	332 contacts	blue
Size-M – “Medium”	30 mm x 45 mm	476 contacts	orange
Size-L – “Large”	45 mm x 45 mm	662 contacts	green

3.2 Contact Characteristics:

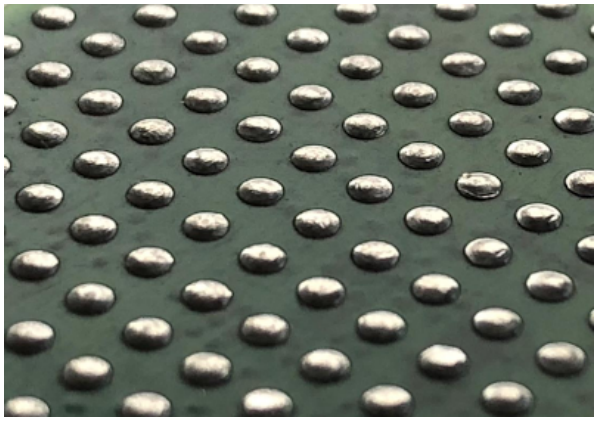
OSM SoMs are available with different contact characteristics:

3.2.1 ENIG-LGA

All OSM-SoMs by ARIES Embedded are using ENIG-LGA contacts on its PCBs:



3.2.2 Fused Tin Grid Array

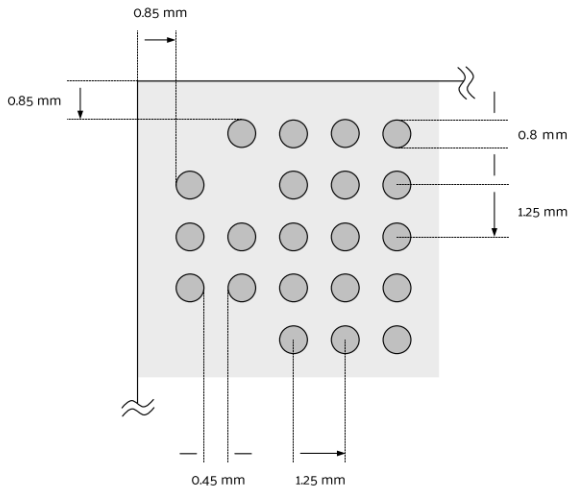


3.2.3 BGA

3.3 Contact Grid

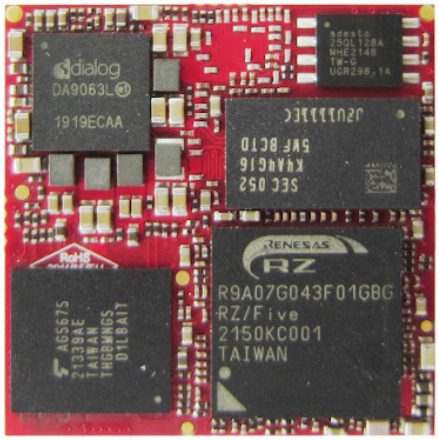
The Contact Grid for the Open Standard Module™ Specification is symmetrically and defines the following dimensions:

- Contact Diameter: 0.8 mm
- Contact Grid: 1.25 mm
- Contact-to-Contact: 0.45 mm
- Contact-to-Edge: 0.85 mm

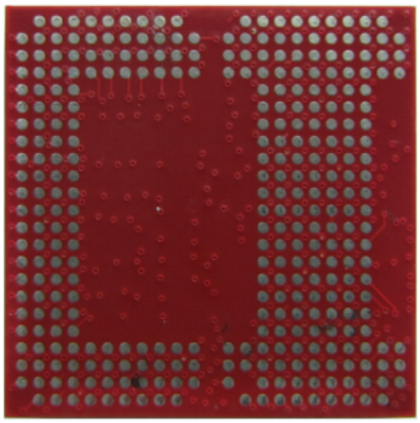


3.4 Recommendations for Processing OSM System on Modules

In the following the MSRZFive-AAA SoM will be used as a reference.



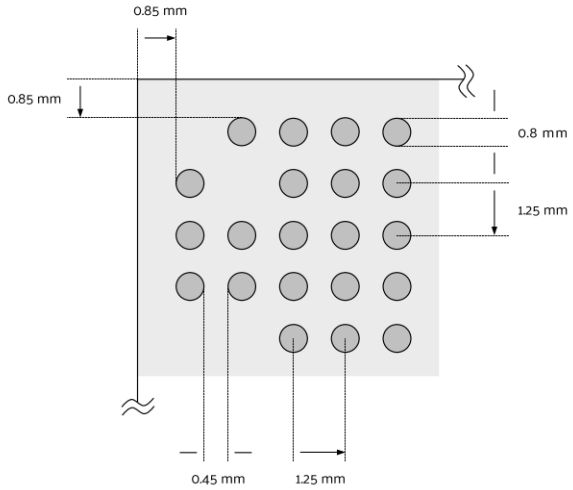
MSRZFive is available as a LGA332 package with round flat pads on the solder side of the SoM:



3.4.1 Design

3.4.1.1 Layout PCB

The connecting pad size of the baseboard layout should be similar to the layout of e.g. the FIVEberry baseboard. The pad size is defined with 0.8mm, the pitch 1.25mm.



3.4.1.2 Stencil

The stencil should have a with of 120µm. The openings in the stencil should be round shape with a diameter of 0.8mm, accordingly.

3.4.2 Process Recommendation

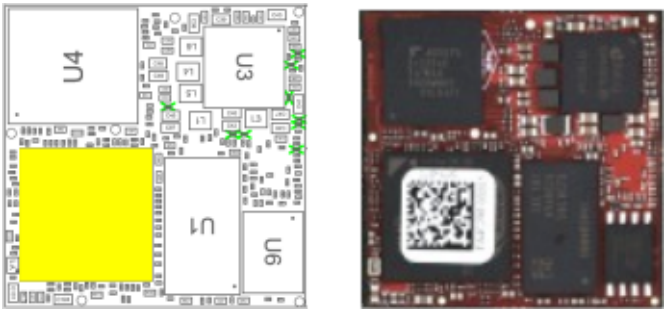
3.4.2.1 Storage

The OSM SoMs are to be handeled as moisture sensitive components. The SoMs shall be stored in suitable vacuum packages with dry packs.

The processing of the SoMs with opened package is limited to 168 hours at a maximum of 30°C and 60% air moisture. In case these values are exceeded and additional drying is necessary, the requirements of J-STD-033 have to b considered.

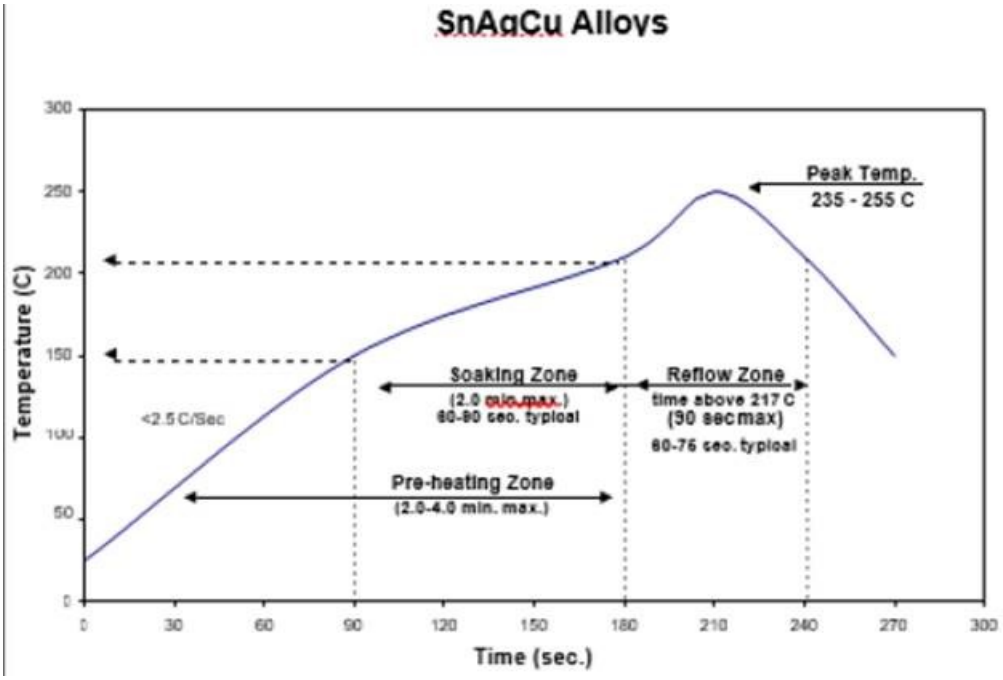
3.4.2.2 Production

For mounting the OSM SoMs the SoMs will be offered to the SMT machine in a tray or a reel. For the pickup of the SoM, using a vacuum nozzle, the SoM should be picked up by using a mechanical point as much as possible in the middle of the SoM, e.g. on U2 (yellow marking).



3.4.2.3 Reflow Soldering

The SoM can be soldered in a reflow soldering process, using a standard RoHS profile. Below picture show the recommendation for the solder paste Kester NP545.



3.5 OSM Design Guide

The primary purpose of OSM Design Guide is to serve as a suggestion for developers of OSM Carrier Boards and for OSM Module customers who wish to have a OSM based system developed. The document should also be valuable to FAEs and Product managers to help them understand the OSM Module infrastructure.

The OSM Design Guide is avaible for download (after registration) under https://sget.org/standards/osm/

CHAPTER

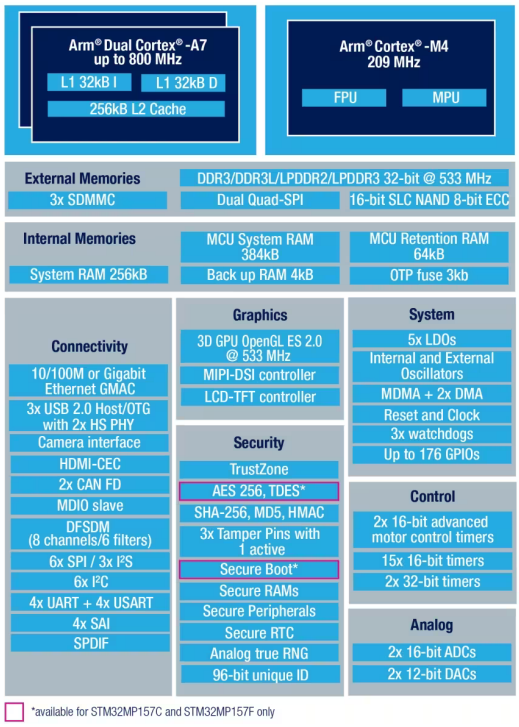
FOUR

RESOURCES

4.1 Components

4.1.1 MPU

STM32MP157 microprocessors are based on the flexible architecture of a Dual Arm® Cortex®-A7 core running up to 800 MHz and Cortex®-M4 at 209 MHz combined with a dedicated 3D graphics processing unit (GPU) and MIPI-DSI display interface and a CAN FD interface. As well as an LCD-TFT display controller, the STM32MP157 line offers 3D GPU, MIPI DSI display interface, CAN FD, 10/100M or Gigabit Ethernet, 3x USB 2.0 Host/OTG and advanced analog.



For more information about the STM32MP157A/D microprocessor please refer to the documentation which is available from STMicroelectronics.

4.1.2 DDR3L RAM

The MSMP1 is equipped with 1 block of NANYA NT5CC512T16EH-EK DDR3L RAM, providing up to 8 Gb of 16-bit memory. The device is designed for the commercial temperature range of 0°C ... +95°C. The memory interface operates at a data rate of up to 1866 Mbps and is clocked at 933 MHz.

4.1.2.1 MPU Signals for DDR3L

MPU Pin	Function	DDR3L Pin		MPU Pin	Function	DDR3L Pin
K19	DDR_A0	N3		E21	DDR_DQ0	E3
M18	DDR_A1	P7		F21	DDR_DQ1	F7
J18	DDR_A2	P3		H21	DDR_DQ2	F2
J19	DDR_A3	N2		E20	DDR_DQ3	F8
T18	DDR_A4	P8		J21	DDR_DQ4	H3
H19	DDR_A5	P2		H20	DDR_DQ5	H8
U19	DDR_A6	R8		H22	DDR_DQ6	G2
F18	DDR_A7	R2		G19	DDR_DQ7	H7
U18	DDR_A8	T8		N22	DDR_DQ8	D7
H18	DDR_A9	R9		R21	DDR_DQ9	C3
N18	DDR_A10	L7		P21	DDR_DQ10	C8
P19	DDR_A11	R7		T20	DDR_DQ11	C2
N19	DDR_A12	N7		V20	DDR_DQ12	A7
G18	DDR_A13	T3		R20	DDR_DQ13	A2
P18	DDR_A14	T7		U21	DDR_DQ14	B8
M19	DDR_A15	M7		V21	DDR_DQ15	A3
K20	DDR_BA0	M2		G22	DDR_DQS0_P	F3
R18	DDR_BA1	N8		G21	DDR_DQS0_N	G3
K18	DDR_BA2	M3		G20	DDR_DQM0	E7
M20	DDR_RASN	J3		T22	DDR_DQS1_P	C7
M22	DDR_CASN	K3		R22	DDR_DQS1_N	B7
N20	DDR_CLK_P	J7		T21	DDR_DQM1	D3
N21	DDR_CLK_N	K7		L21	DDR_ODT	K1
R19	DDR_CKE	K9		–	–	–
L18	DDR_CSN	L2		–	–	–
M21	DDR_WEN	L3		–	–	–
F19	DDR_RSTN	T2		–	–	–

4.1.3 SPI-NOR Flash

MSMP1 features a SPI-NOR device in a range of 128MBit to 512MBit.

Device	Capacity
W25Q128JVEIQ	128MBit
W25Q256JVEIQ	256MBit
W25Q512JVEIQ	512MBit

The SPI-NOR flash device uses the following connections:

MPU Pin	Function	SPI-NOR Pin
W13	CS#	1
AB11	DO	2
AA10	WP#	3
	GND	4
AB10	DI	5
V12	CLK	6
AA11	RES#	7
	VCC	7

4.1.4 eMMC Flash

The MSMP1 supports one eMMC NAND Flash in the range of 4-64 GByte. The eMMC provides a high-speed memory card interface compliant with JEDEC Version 5.0, eliminating the need for users to be concerned about directly controlling Flash Memories.

MPU Pin	Function	eMMC Pin
D11	SDMMC2_CMD	M5
B11	SDMMC2_D7	B6
E13	SDMMC2_D6	B5
E11	SDMMC2_D5	B4
F15	SDMMC2_D4	B3
C13	SDMMC2_D3	B2
A12	SDMMC2_D2	A5
B12	SDMMC2_D1	A4
A13	SDMMC2_D0	A3
E2	–	H5
A10	SDMMC2_CK	M6
R2	NRST	K5

4.1.5 PMIC

The power management on the MSMP1 SoM is provided by a STPMIC1xPQR ST-Microelectronics fully integrated power management IC. The device integrates advanced low power features controlled by a host processor via I^2C and IO interface.

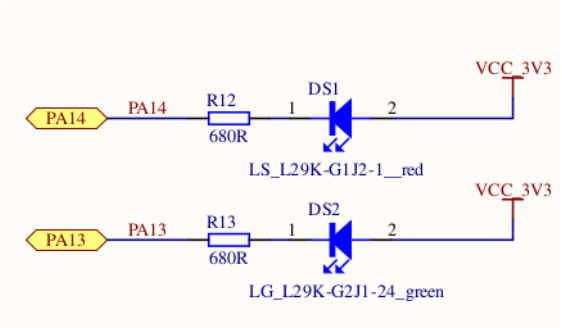
The MSMP1 supports a supply voltage range of 3.7V to 5.5V. This range fully includes the OSM standard supply voltage of 5V (+/-5%).

PMIC connections

MPU Pin	Function	PMIC Pin	SiP Pads
G1	I2C4_SCL/PMIC	4 SCL	–
H4	I2C4_SDA/PMIC	3 SDA	–
T1	PWR_ON	44 PWRCTRL	–
R2	NRST	1 RSTn	–
N2	PMIC/WAKEUP	2 WAKEUP	–
–	PMIC/PONKEYn	17 PONKEYn	AA9
N1	PI8_WKUP	43 INTn	–

4.1.6 User LEDs

The ports PA13 and PA14 are connected to user LEDs as follows:



MPU Pin	Function	SiP Pads	Remarks
R3	PA14	F17	Do not use (3V3, red LED on module)
W3	PA13	E17	Do not use (3V3, green LED on module)

4.2 Interfaces

4.2.1 I2C

When using MSMP1 in conformity to the OSM standard two I2C interfaces are available:

MPU Pin	Function	SiP Pads	Remarks
B9	I2C2_SCL	AA15	2k2 pullup to VCC
E10	I2C2_SDA	AA16	2k2 pullup to VCC
G3	I2C6_SCL	AA20	2k2 pullup to VCC
H3	I2C6_SDA	AA21	2k2 pullup to VCC

4.2.2 I2S

When using MSMP1 in conformity to the OSM standard one I2S interface is available:

MPU Pin	Function	SiP Pads
E1	I2S2_SDI (TIM8_CH4)	V21
E3	I2S2_SDO (TIM8_ETR)	W21
D7	I2S2_MCK (GPIO/UART8_TX_CH4)	V18
D1	I2S2_WS (TIM5_CH4)	W18
E2	I2S2_CK (TIM8_BKIN2)	W20

4.2.3 SPI

When using MSMP1 in conformity to the OSM standard three SPI interface are available:

MPU Pin	Function	SiP Pads
G2	SPI1_SCK	D29
H5	SPI1_MISO	C29
K5	SPI1_MOSI	D30
F4	SPI1_NSS	C30
C5	SPI3_SCK	U16
A8	SPI3_MISO	U15
AA8	SPI3_MOSI	V15
V6	SPI3_NSS	Y15
E4	SPI4_SCK	Y21
C12	SPI4_MISO	Y22
B4	SPI4_MOSI	Y23
D5	SPI4_NSS	AA23

4.2.4 JTAG

MPU Pin	Function	SiP Pads
D17	JTAG_TCK	N17
E17	JTAG_TMS	N19
D16	JTAG_TDI	P17
E16	JTAG_TDO	R17
E15	JTAG_NTRST	R19

4.2.5 UART

4.2.5.1 UART

MPU Pin	Function	SiP Pads
AA11	UART7_RX (SPI5_NSS)	A14
AA10	UART7_TX (SPI5_SCK)	B13
AB10	UART7_RTS (SPI5_MISO)	C13
AB11	UART7_CTS (SPI5_MOSI)	C14

4.2.5.2 UART-Console

MPU Pin	Function	SiP Pads
V13	UART4_RX	D22
U11	UART4_TX	D23

4.2.5.3 USART

MPU Pin	Function	SiP Pads
F9	USART2_RX (GPIO)	D14
D9	USART2_TX (GPIO)	D13
C9	USART2_RTS (FMC_NOE)	D15
C4	USART2_CTS (TIM1_BKIN)	D16
F10	USART2_CK (GPIO)	B21

4.2.6 TIMER/PWM

MPU Pin	Function	SiP Pads
B13	PA8 (TIM1_CH1)	E18
A11	PA9 (TIM1_CH2)	F18
A4	PE13 (TIM1_CH3)	G18
Y16	PA11 (TIM1_CH4)	H18
B1	PH10 (TIM5_CH1)	J18
B3	PH11 (TIM5_CH2)	K18

4.2.7 Ethernet

MPU Pin	Function	SiP Pads
U8	ETH_RGMII_CLK125	N16
AB4	ETH_RGMII_GTX_CLK	J15
Y5	ETH_RGMII_TX_CTL	K16
AA1	ETH_RGMII_TXD0	H15
AA2	ETH_RGMII_TXD1	G15
Y1	ETH_RGMII_TXD2	H16
Y2	ETH_RGMII_TXD3	G16
V4	ETH_RGMII_RX_CLK	R15
Y9	ETH_RGMII_RX_CTL	M15
AB6	ETH_RGMII_RXD0	K15
AA6	ETH_RGMII_RXD1	L15
V11	ETH_RGMII_RXD2	N15
W2	ETH_RGMII_RXD3	P15
W1	ETH_GMII_RX_ER	L16
AB7	ETH_GMII_CRS	E16
Y6	ETH_GMII_COL	F15
AB3	ETH_MDC	T16
AB2	ETH_MDIO	T15
W5	ETH_MDINT	M2
J4	ETH_PHYINT	R34

4.2.8 FDCAN

MPU Pin	Function	SiP Pads
D3	FDCAN1_TX	AC17
C2	FDCAN1_RX	AB17
V10	FDCAN2_TX	AC19
AA7	FDCAN2_RX	AB19

4.2.9 COM/FMC

MPU Pin	Function	SiP Pads
M3	PD14 (GPIO/FMC_AD0)	A15
L1	PD15 (GPIO/FMC_AD1)	A16
C10	PD0 (GPIO/FMC_AD2/I2C5_SDA)	A17
B10	PD1 (GPIO/FMC_AD3/I2C5_SCL)	A18
W10	PE7 (GPIO/FMC_AD4/QSPI_BK2_IO0)	A19
Y12	PE8 (GPIO/FMC_AD5/QSPI_BK2_IO1)	A20
W11	PE9 (GPIO/FMC_AD6/QSPI_BK2_IO2)	A21
W14	PE10 (GPIO/FMC_AD7/QSPI_BK2_IO3)	B15
AB9	PD11 (GPIO/FMC_CLE)	B16
W12	PD12 (GPIO/FMC_ALE)	B17
L3	PD6 (GPIO/FMC_NWAIT)	B18
A9	PD5 (GPIO/FMC_NWE)	B19
W15	PG9 (GPIO/FMC_NCE)	B20
N2	PC13 (RTC_OUT1)	C15

4.2.10 USB1 Interface (OTG)

MPU Pin	Function	SiP Pads
AA14	USB1_D_N	AB23
AB14	USB1_D_P	AC22
Y17	OTG_ID	AB22
V15	OTG_VBUS	AB20

4.2.11 USB2 Interface (Host)

MPU Pin	Function	SiP Pads
AB15	USB2_D_N	AB13
AA15	USB2_D_P	AC14

4.2.12 DISPLAY-RGB

MPU Pin	Function	SiP Pads
F3	LCD_R0	C17
J2	LCD_R1	AA29
L6	LCD_R2	Y7
K4	LCD_R3	AA6
J1	LCD_R4	Y6
K2	LCD_R5	AA5
K1	LCD_R6	Y5
L5	LCD_R7	Y4
L4	LCD_G0	C19
H6	LCD_G1	AA30
L2	LCD_G2	W4
J3	LCD_G3	V3
K6	LCD_G4	V4
D8	LCD_G5	U3
E7	LCD_G6	T3
E8	LCD_G7	T4
B8	LCD_B0	C21
A7	LCD_B1	AA31
B7	LCD_B2	R4
C7	LCD_B3	R3
B6	LCD_B4	P3
A6	LCD_B5	N3
C6	LCD_B6	N4
A5	LCD_B7	M3
D2	LCD_CLK	M4
H1	LCD_VSYNC	L3
H2	LCD_HSYNC	K3
T4	LCD_BL_CTRL	K4
B5	LCD_DE	J4

4.2.13 DISPLAY-DSI

MPU Pin	Function	SiP Pads
A15	DSI_DATA0_N	AB11
B15	DSI_DATA0_P	AB10
A17	DSI_DATA1_N	AC9
B17	DSI_DATA1_P	AC8
A16	DSI_CLK_N	AB8
B16	DSI_CLK_P	AB7
V14	PD13/DSI_TE	AA3

4.2.14 SDCARD

MPU Pin	Function	SiP Pads
E12	SDMMC1_CK	F21
D12	SDMMC1_CMD	E20
E14	SDMMC1_D0	G20
D14	SDMMC1_D1	G21
F14	SDMMC1_D2	H20
D15	SDMMC1_D3	H21
Y4	SD_CardDetect	J21
W13	PB6/SD_PWR_EN	D21
V9	PB10/SD_WP	D20

4.2.15 GPIO

MPU Pin	Function	SiP Pads
B13	PA8 (GPIO/TIM1_CH1)	E18
A11	PA9 (GPIO/TIM1_CH2)	F18
A4	PE13 (GPIO/TIM1_CH3)	G18
Y16	PA11 (GPIO/TIM1_CH4)	H18
B1	PH10 (GPIO/TIM5_CH1)	J18
B3	PH11 (GPIO/TIM5_CH2)	K18
W16	PA12 (GPIO/TIM1_ETR)	D17
W3	PA13 (GPIO/DBTRGI)	E17
R3	PA14 (GPIO/DBTRGO)	F17
F11	PB7 (GPIO/TIM4_CH2)	G17
AB8	PB8 (GPIO/TIM4_CH3)	H17
F12	PB9 (GPIO/TIM4_CH4)	J17
U10	PC0 (GPIO)	K17
U3	PC3 (GPIO)	L17
D13	PC7 (GPIO)	D19
M1	PD8 (GPIO)	E19
M2	PD9 (GPIO)	F19
E9	PE6 (GPIO/TIM1_BKIN2)	G19
F13	PF2 (GPIO)	H19
V3	PF3 (GPIO)	J19
V12	PF10 (GPIO/QSPI_CLK)	K19
W6	PF15 (GPIO)	L19
W4	PG2 (GPIO)	D3
U4	PG3 (GPIO/CAN_STBY)	D4
Y8	PG8 (GPIO/ETH_CLK)	E3
D10	PG15 (GPIO)	E4
A3	PH4 (GPIO)	F3
A2	PH5 (GPIO)	F4
D6	PH8 (GPIO)	G3
E6	PH9 (GPIO)	G4
F5	PH12 (GPIO/TIM5_CH3)	U32

continues on next page

Table 1 – continued from previous page

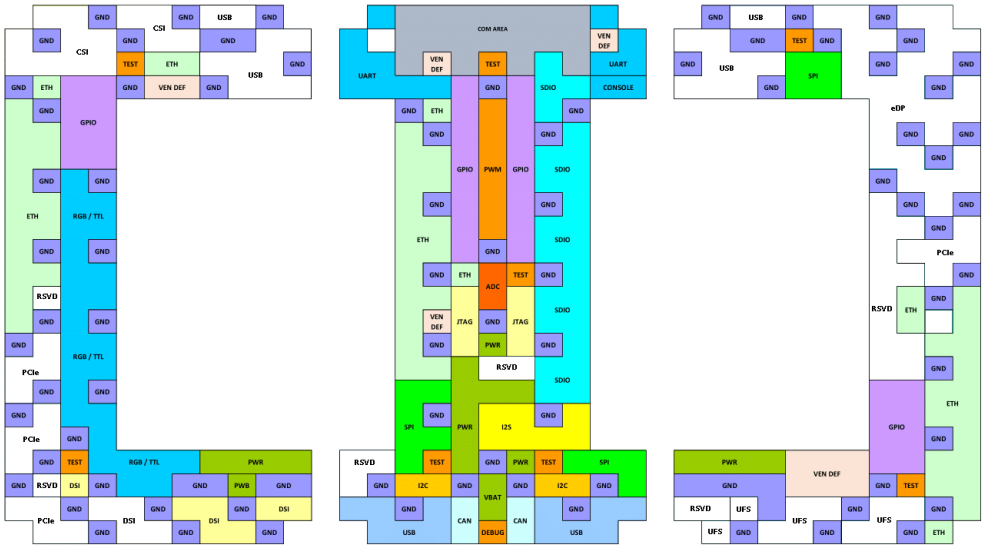
MPU Pin	Function	SiP Pads
C1	PH15 (GPIO/TIM8_CH3N)	U33
J6	PI4 (GPIO/TIM8_BKIN)	V32
F2	PI5 (GPIO/TIM8_CH1)	V33
G5	PI6 (GPIO/TIM8_CH2)	W32
F1	PI7 (GPIO/TIM8_CH3)	W33
J5	PI9 (GPIO)	Y32
T3	PI11 (GPIO)	H3
AA5	PB1 (GPIO/TIM1_CH3N)	Y33
Y11	PG7 (GPIO/UART8_RTS)	W15
AA9	PG10 (GPIO/UART8_CTS)	W16

4.2.16 ADC

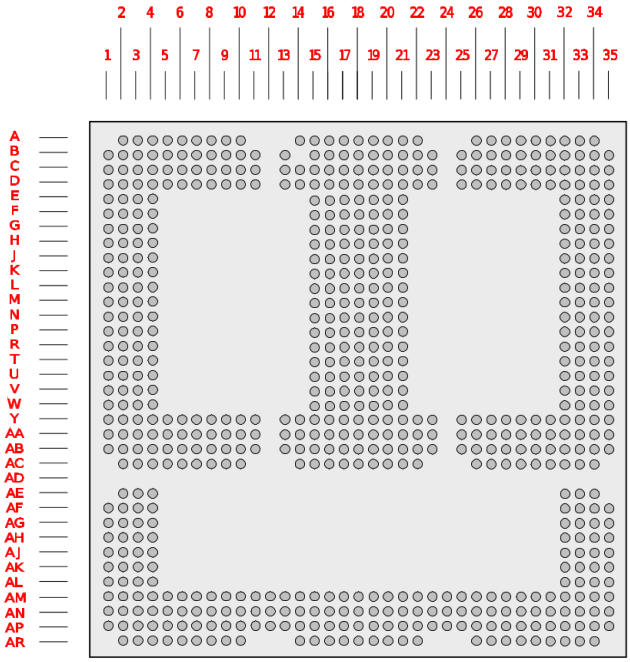
MPU Pin	Function	SiP Pads
R4	ANA0/ADC1_IN0	M18
W8	PF11/ADC1_IN2 (GPIO)	B22
V8	PF12/ADC1_IN6 (GPIO)	C16
AA3	PA0/ADC1_IN16 (GPIO)	P16
U5	PA5/ADC1_IN19 (GPIO)	C6
T5	ANA1/ADC2_IN1	N18
W7	PF13/ADC2_IN2 (GPIO)	C7
W9	PA6/ADC2_IN3 (GPIO)	D6
V7	PF14/ADC2_IN6 (GPIO)	D7
AB5	PB0/ADC2_IN9 (GPIO)	Y29

4.2.17 MSMP1 SiP Pads

4.2.17.1 Contact Groups



4.2.17.2 Contact Grid Numbering



4.2.17.3 Contact Table

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
ETHERNET						
AB4	ETH_RGMII_GTX_CLK	J15		AA1	ETH_RGMII_TXD0	H15
AA2	ETH_RGMII_TXD1	G15		Y1	ETH_RGMII_TXD2	H16
Y1	ETH_RGMII_TXD2	H16		Y2	ETH_RGMII_TXD3	G16
Y5	ETH_RGMII_TX_CTL	K16		V4	ETH_RGMII_RX_CLK	R15
AB6	ETH_RGMII_RXDO	K15		AA6	ETH_RGMII_RXD1	L15
V11	ETH_RGMII_RXD2	N15		W2	ETH_RGMII_RXD3	P15
W2	ETH_RGMII_RXD3	P15		W1	ETH_GMII_RX_ER	L16
Y9	ETH_RGMII_RX_CTL	M15		AB7	ETH_GMII_CRS	E16
Y6	ERH_GMII_COL	F15		U8	ETH_RGMII_CLK125	N16
AB3	ETH_MDC	T16		AB2	ETH_MDIO	T15
–	–	H1		–	–	G1
–	–	F1		–	–	G2
–	–	F2		–	–	J2
–	–	P1		–	–	J1
–	–	K1		–	–	M1
–	–	N1		–	–	K2
–	–	L1		–	–	D2
–	–	E1		W5	ETH_RSTN	M2
–	–	C6		–	–	C7
–	–	N35		–	–	Y35
–	–	AA35		–	–	Y34
–	–	AA34		–	–	V34
–	–	W35		–	–	V35
–	–	U35		–	–	R35
–	–	P35		–	–	U34
–	–	T35		–	–	AC34
–	–	AB35		J4	ETH_PHY_INTN	R34
CAN						
D3	FDCAN1_TX	AC17		C2	FDCAN1_RX	AB17
V10	FDCAN2_TX	AC19		AA7	FDCAN2_RX	AB19
USB						
AA15	USB2_D_P	AC14		AB15	USB2_D_N	AB13
–	–	AC16		Y17	OTG_ID	AB14
–	–	AC15		V15	OTG_VBUS	AB16
AB14	USB1_D_P	AC22		AA14	USB1_D_N	AB23
–	–	AC20		–	–	AB22
–	–	AC21		–	–	AB20
–	–	D10		–	–	D11
–	–	C10		–	–	D9
–	–	C8		–	–	C9
–	–	A9		–	–	A8
–	–	B11		–	–	B10
–	–	D25		–	–	D26
–	–	C26		–	–	D27
–	–	C28		–	–	C27
–	–	A28		–	–	A27

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	–	B26		–	–	B25
SDIO						
E12	SDMMC1_CK	F21		D12	SDMMC1_CMD	E20
Y4	SD_CardDetect	J21		–	–	D20
E14	SDMMC1_D0	G20		D14	SDMMC1_D1	G21
F14	SDMMC1_D2	H20		D15	SDMMC1_D3	H21
V9	PB10 (GPIO)	D21		–	–	C20
	–	K20		–	–	K21
–	–	T21		–	–	U20
–	–	L20		–	–	L21
–	–	M21		–	–	N20
–	–	N21		–	–	P20
–	–	P21		–	–	R21
–	–	U21		–	–	T20
UART						
V13	UART4_RX	D22		U11	UART4_TX	D23
AA11	UART7_RX (SPI5_NSS)	A14		AA10	UART7_TX (SPI5_SCK)	B13
AB10	UART7_RTS (SPI5_MISO)	C13		AB11	UART7_CTS (SPI5_MOSI)	C14
F9	USART2_RX (GPIO)	D14		D9	USART2_TX (GPIO)	D13
C9	USART2_RTS (FMC_NOE)	D15		C4	USART2_CTS (TIM1_BKIN)	D16
–	–	A22		–	–	B23
–	–	C22		–	–	C23
SPI/I2C/I2S						
B9	I2C2_SCL	AA15		E10	I2C2_SDA	AA16
G3	I2C6_SCL	AA20		H3	I2C6_SDA	AA21
E1	I2S2_SDI (TIM8_CH4)	V21		E3	I2S2_SDO (TIM8_ETR)	W21
–	–	V19		–	–	W19
D7	I2S2_MCK (GPIO/UART8_TX)	V18		D1	I2S2_WS (TIM5_CH4)	W18
E2	I2S2_CK (TIM8_BKIN2)	W20		A8	SPI3_MISO	U15
AA8	SPI3_MOSI	V15		AA9	PG10 (GPIO/UART8_CTS)	W16
Y11	PG7 (GPIO/UART8_RTS)	W15		V6	SPI3_NSS	Y15
C5	SPI3_SCK	U16		C12	SPI4_MISO	Y22
B4	SPI4_MOSI	Y23		D5	SPI4_NSS	AA23
E4	SPI4_SCK	Y21		H5	SPI1_MISO	C29
K5	SPI1_MOSI	D30		F4	SPI1_NSS	C30
G2	SPI1_SCK	D29		–	–	–
GPIO/ADC/PWM						
R4	ANA0/ADC1_IN0	M18		T5	ANA1/ADC2_IN1	N18
B13	PA8 (GPIO/TIM1_CH1)	E18		A11	PA9 (GPIO/TIM1_CH2)	F18
A4	PE13 (GPIO/TIM1_CH3)	G18		Y16	PA11 (GPIO/TIM1_CH4)	H18
B1	PH10 (GPIO/TIM5_CH1)	J18		B3	PH11 (GPIO/TIM5_CH2)	K18
W16	PA12 (GPIO/TIM1_ETR)	D17		W3	PA13 (GPIO/DBTRGI)	E17
R3	PA14 (GPIO/DBTRGO)	F17		F11	PB7 (GPIO/TIM4_CH2)	G17
AB8	PB8 (GPIO/TIM4_CH3)	H17		F12	PB9 (GPIO/TIM4_CH4)	J17

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
U10	PC0 (GPIO)	K17		U3	PC3 (GPIO)	L17
D13	PC7 (GPIO)	D19		F10	PD7 (GPIO/USART2_CK)	E19
M1	PD8 (GPIO)	F19		M2	PD9 (GPIO)	G19
E9	PE6 (GPIO/TIM1_BKIN2)	H19		F13	PF2 (GPIO)	J19
V3	PF3 (GPIO)	K19		W6	PF15 (GPIO)	L19
W4	PG2 (GPIO)	D3		U4	PG3 (GPIO/CAN_STBY)	D4
Y8	PG8 (GPIO/ETH_CLK)	E3		D10	PG15 (GPIO)	E4
A3	PH4 (GPIO)	F3		A2	PH5 (GPIO)	F4
D6	PH8 (GPIO)	G3		E6	PH9 (GPIO)	G4
F5	PH12 (GPIO/TIM5_CH3)	U32		C1	PH15 (GPIO/TIM8_CH3N)	U33
J6	PI4 (GPIO/TIM8_BKIN)	V32		F2	PI5 (GPIO/TIM8_CH1)	V33
G5	PI6 (GPIO/TIM8_CH2)	W32		F1	PI7 (GPIO/TIM8_CH3)	W33
J5	PI9 (GPIO)	Y32		AA5	PB1 (GPIO/TIM1_CH3N)	Y33
VENDOR DEFINED PINS						
W8	PF11/ADC1_IN2 (GPIO)	B22		V8	PF12/ADC1_IN6 (GPIO)	C16
AA3	PA0/ADC1_IN16 (GPIO)	P16		W9	PA6/ADC2_IN3 (GPIO)	D6
V7	PF14/ADC2_IN6 (GPIO)	D7		AB5	PB0/ADC2_IN9 (GPIO)	Y29
–	–	Y30		P4	BOOT2	Y31
J2	LCD_R1	AA29		H6	LCD_G1	AA30
A7	LCD_B1	AA31		–	–	–
COM/FMC						
M3	PD14 (GPIO/FMC_AD0)	A15		L1	PD15 (GPIO/FMC_AD1)	A16
C10	PD0 (GPIO/FMC_AD2/ I2C5_SDA)	A17		B10	PD1 (GPIO/FMC_AD3/ I2C5_SCL)	A18
W10	PE7 (GPIO/FMC_AD4/ QSPI_BK2_IOO)	A19		Y12	PE8 (GPIO/FMC_AD5/ QSPI_BK2_IO1)	A20
W11	PE9 (GPIO/FMC_AD6/ QSPI_BK2_IO2)	A21		W14	PE10 (GPIO/FMC_AD7/ QSPI_BK2_IO3)	B15
AB9	PD11 (GPIO/FMC_CLE)	B16		W12	PD12 (GPIO/FMC_ALE)	B17
L3	PD6 (GPIO/FMC_NWAIT)	B18		A9	PD5 (GPIO/FMC_NWE)	B19
W15	PG9 (GPIO/FMC_NCE)	B20		–	–	B21
N2	PC13 (RTC_OUT1)	C15		F3	LCD_R0	C17
L4	LCD_G0	C19		B8	LCD_B0	C21
CONFIG/JTAG						
D17	JTAG_TCK	N17		–	–	P19
E17	JTAG_TMS	N19		D16	JTAG_TDI	P17
E16	JTAG_TDO	R17		E15	JTAG_nTRST	R19
–	–	AC18		–	–	C18
RGB DISPLAY						
L6	LCD_R2	Y7		K4	LCD_R3	AA6
J1	LCD_R4	Y6		K2	LCD_R5	AA5
K1	LCD_R6	Y5		L5	LCD_R7	Y4
L2	LCD_G2	W4		J3	LCD_G3	V3
K6	LCD_G4	V4		D8	LCD_G5	U3
E7	LCD_G6	T3		E8	LCD_G7	T4

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
B7	LCD_B2	R4		C7	LCD_B3	R3
B6	LCD_B4	P3		A6	LCD_B5	N3
C6	LCD_B6	N4		A5	LCD_B7	M3
D2	LCD_CLK	M4		H1	LCD_VSYNC	L3
H2	LCD_HSYNC	K3		T4	LCD_BL_CTRL	K4
B5	LCD_DE	J4		R2	NRST	J3
T3	PI11 (GPIO)	H3		–	–	–
MIPI DSI						
A15	DSI_DATA0_N	AB11		B15	DSI_DATA0_P	AB10
A17	DSI_DATA1_N	AC9		B17	DSI_DATA1_P	AC8
–	–	AC6		–	–	AC5
–	–	AB5		–	–	AB4
A16	DSI_CLK_N	AB8		B16	DSI_CLK_P	AB7
V14	PD13/DSI_TE (GPIO)	AA3		–	–	–
MIPI CSI						
–	–	C1		–	–	B1
–	–	A2		–	–	A3
–	–	A5		–	–	A6
–	–	B6		–	–	B7
–	–	B3		–	–	B4
–	–	C2		–	–	C3
–	–	C4		–	–	–
PCIe						
–	–	AB1		–	–	AB2
–	–	AC2		–	–	AC3
–	–	W2		–	–	V2
–	–	W1		–	–	Y1
–	–	T2		–	–	U1
–	–	T1		–	–	R2
–	–	L34		–	–	M34
–	–	K35		–	–	L35
–	–	K33		–	–	L33
eDP/eDP++						
–	–	A30		–	–	A31
–	–	B31		–	–	B32
–	–	A33		–	–	A34
–	–	B34		–	–	B35
–	–	C33		–	–	C34
–	–	D32		–	–	D33
–	–	D31		–	–	C31
–	–	D35		–	–	E35
–	–	E34		–	–	F34
–	–	G35		–	–	H35
–	–	H34		–	–	J34
–	–	G33		–	–	H33
–	–	F32		–	–	G32
–	–	E32		–	–	E33
UFS						
–	–	AC29		–	–	AC28

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Table 2 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	–	AC32		–	–	AC31
–	–	AB30		–	–	AB29
–	–	AB33		–	–	AB32
–	–	AB27		–	–	AC26
PWR						
–	5V	Y17		–	–	Y19
–	VBAT	W17		–	–	U18
–	–	AA18		–	–	AB18
–	NRST	U17		T2	CAR_PWR_EN	V17
N3	BOOT0	U19		N4	BOOT1	R18
	–	T17		–	VBUS_OTG	M19
–	VBUS_SW	Y16		–	–	–
–	3.3V 1.8V	Y20		–	5V	Y8
–	5V	Y9		–	5V	Y10
–	5V	Y11		–	–	Y3
–	–	C5		–	PMIC/PONKEYn	AA9
–	5V	Y25		–	5V	Y26
–	5V	Y27		–	5V	Y28
–	–	AA33		–	–	B29
GND						
–	GND	D18		–	GND	E15
–	GND	E21		–	GND	F16
–	GND	F20		–	GND	J16
–	GND	J20		–	GND	L18
–	GND	M16		–	GND	M20
–	GND	P18		–	GND	A4
–	GND	A7		–	GND	A10
–	GND	B2		–	GND	B5
–	GND	B8		–	GND	B9
–	GND	C11		–	GND	D1
–	GND	D5		–	GND	D8
–	GND	E2		–	GND	H2
–	GND	H4		–	GND	L2
–	GND	L4		–	GND	P2
–	GND	P4		–	GND	A26
–	GND	A29		–	GND	A32
–	GND	B27		–	GND	B28
–	GND	B30		–	GND	B33
–	GND	C25		–	GND	C32
–	GND	C35		–	GND	A10
–	GND	D28		–	GND	D34
–	GND	F33		–	GND	F35
–	GND	G34		–	GND	H32
–	GND	J33		–	GND	R16
–	GND	R20		–	GND	V16
–	GND	V20		–	GND	Y18
–	GND	AA14		–	GND	AA17
–	GND	AA19		–	GND	AA22
–	GND	AB15		–	GND	AB21

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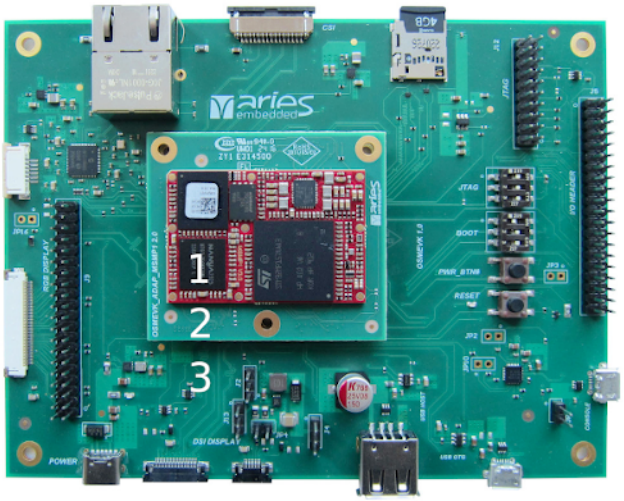
Table 2 – continued from previous page

MPU Pin	Function	SiP Pads		MPU Pin	Function	SiP Pads
–	GND	R1		–	GND	U2
–	GND	U4		–	GND	V1
–	GND	W3		–	GND	Y2
–	GND	AA1		–	GND	AA4
–	GND	AA7		–	GND	AA8
–	GND	AA10		–	GND	AA11
–	GND	AB3		–	GND	AB6
–	GND	AB9		–	GND	AC4
–	GND	AC7		–	GND	AC10
–	GND	J35		–	GND	K34
–	GND	M35		–	GND	N34
–	GND	T34		–	GND	W34
–	GND	AA25		–	GND	AA26
–	GND	AA27		–	GND	AA28
–	GND	AA32		–	GND	AB28
–	GND	AB31		–	GND	AB34
–	GND	AC27		–	GND	AC30
–	GND	AC33		–	–	–
RESERVED						
–	–	R18		–	–	T17
–	–	T18		–	–	T19
–	–	Y13		–	–	Y14
–	–	AA13		–	–	N2
–	–	AA2		–	–	J32
–	–	K32		–	–	L32
–	–	M32		–	–	M33
–	–	N32		–	–	N33
–	–	P32		–	–	P33
–	–	P34		–	–	R32
–	–	R33		–	–	T32
–	–	T33		–	–	AB25
–	–	AB26		–	–	–

4.3 Conversion of MSMP1 interfaces to OSMEVK baseboard

The adapter board OSMEVK_ADAP_MSMP1 (**2**) enables the conversion of interfaces and/or voltage levels from the MSMP1 module (**1**) to the appropriate value and direction, ensuring compatibility with the SoM functionality on the OSMEVK baseboard (**3**).



CPU Pin	OSM Pin	MSMP1 Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
ETHERNET				
AB4	J15	ETH_RGMII_GTX_CLK	ETH_A_TXCLK	P1-39
AA1	H15	ETH_RGMII_TXD0	ETH_A_TXD0	P1-47
AA2	G15	ETH_RGMII_TXD1	ETH_A_TXD1	P1-45
Y1	H16	ETH_RGMII_TXD2	ETH_A_TXD2	P1-43
Y2	G16	ETH_RGMII_TXD3	ETH_A_TXD3	P1-41
Y5	K16	ETH_RGMII_TX_CTL	ETH_A_TXCTL	P1-37
V4	R15	ETH_RGMII_RX_CLK	ETH_A_RXCLK	P1-21
AB6	K15	ETH_RGMII_RXD0	ETH_A_RXD0	P1-25
AA6	L15	ETH_RGMII_RXD1	ETH_A_RXD1	P1-27
V11	N15	ETH_RGMII_RXD2	ETH_A_RXD2	P1-29
W2	P15	ETH_RGMII_RXD3	ETH_A_RXD3	P1-31
W1	L16	ETH_MII_RX_ER	–	–
Y9	M15	ETH_RGMII_RX_CTL	ETH_A_RXCTL	P1-23
AB7	E16	ETH_MII_CRS	–	–
Y6	F15	ETH_MII_COL	–	–
U8	N16	ETH_RGMII_CLK125	ETH_PHY_CLK	P1-15
AB3	T16	ETH_MDC	ETH_A_MDC	P1-11
AB2	T15	ETH_MDIO	ETH_A_MDIO	P1-9
W5	M2	ETH_RSTN	–	–
J4	R34	ETH_PHY_INTN	–	–
CAN/USB				
D3	AC17	FDCAN1_TX	CAN_A_TX	P4-1
C2	AB17	FDCAN1_RX	CAN_A_RX	P4-2
V10	AC19	FDCAN2_TX	–	–

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Table 3 – continued from previous page

CPU Pin	OSM Pin	MSMP1 Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
AA7	AB19	FDCAN2_RX	–	–
AB14	AC14	USB2_D_P (Diff.)	USB_OTG_D_P	P4-20
AA14	AB13	USB2_D_N (Diff.)	USB_OTG_D_N	P4-22
U5	AC16	PA5 (GPIO)	USB_OTG_EN	P4-14
Y17	AB14	OTG_ID (GPIO)	USB_OTG_ID	P4-16
V15	AB16	OTG_VBUS	USB_OTG_VBUS	P4-4/6/8
AA15	AC22	USB1_D_P (Diff.)	USB_HOST_D_P	P4-32
AB15	AB23	USB1_D_N (Diff.)	USB_HOST_D_N	P4-34
W7	AC20	PF13 (GPIO)	USB_HOST_EN	P4-26
SDIO				
E12	F21	SDMMC1_CK	SDIO_CLK	P2-27
D12	E20	SDMMC1_CMD	SDIO_CMD	P2-25
Y4	J21	SD_CardDetect	SDIO_CD#	P2-37
E14	G20	SDMMC1_D0	SDIO_DAT0	P2-29
D14	G21	SDMMC1_D1	SDIO_DAT1	P2-31
F14	H20	SDMMC1_D2	SDIO_DAT2	P2-33
D15	H21	SDMMC1_D3	SDIO_DAT3	P2-35
V9	D21	PB10 (GPIO)	SDIO_PWR_EN_RES	–
UART				
V13	D22	UART4_RX	CONS_RX	P2-48
U11	D23	UART4_TX	CONS_TX	P2-46
F9	D14	USART2_RX (GPIO)	–	–
D9	D13	USART2_TX (GPIO)	–	–
C9	D15	USART2_RTS (FMC_NOE)	–	–
C4	D16	USART2_CTS (TIM1_BKIN)	–	–
SPI/I2C/I2S				
B9	AA15	I2C2_SCL	I2C_A_SCL	P4-35
E10	AA16	I2C2_SDA	I2C_A_SDA	P4-37
G3	AA20	I2C6_SCL	I2C_B_SCL	P4-38
H3	AA21	I2C6_SDA	I2C_B_SDA	P4-40
E1	V21	I2S2_SDI (TIM8_CH4)	I2S_DATA_A_IN	P4-41
E3	W21	I2S2_SDO (TIM8_ETR)	I2S_DATA_A_OUT	P4-45
D7	V18	I2S2_MCK (GPIO/UART8_TX)	–	–
D1	W18	I2S2_WS (TIM5_CH4)	I2S_LRCLK	P4-47
E2	W20	I2S2_CK (TIM8_BKIN2)	I2S_BITCLK	P4-43
A8	U15	SPI3_MISO (GPIO)	SPI_A_SDI	P4-17
AA8	V15	SPI3_MOSI (GPIO)	SPI_A_SDO	P4-15
AA9	W16	PG10 (GPIO/UART8_CTS)	–	–
Y11	W15	PG7 (GPIO/UART8_RTS)	–	–
V6	Y15	SPI3_NSS (GPIO/TIM5_ETR)	SPI_A_CS0#	P4-13
C5	U16	SPI3_SCK (GPIO/UART8_RX)	SPI_A_SCK	P4-11
C12	Y22	SPI4_MISO	–	–

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Table 3 – continued from previous page

CPU Pin	OSM Pin	MSMP1 Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
B4	Y23	SPI4_MOSI	–	–
D5	AA23	SPI4_NSS	–	–
E4	Y21	SPI4_SCK	–	–
H5	C29	SPI1_MISO	–	–
K5	D30	SPI1_MOSI	–	–
F4	C30	SPI1_NSS	–	–
G2	D29	SPI1_SCK	–	–
GPIO/ADC/PWM				
R4	M18	ANA0/ADC1_IN0	ADC_0	P2-43
T5	N18	ANA1/ADC2_IN1	ADC_1	P2-45
B13	E18	PA8 (GPIO/TIM1_CH1)	PWM_1	P2-24
A11	F18	PA9 (GPIO/TIM1_CH2)	PWM_2	P2-26
A4	G18	PE13 (GPIO/TIM1_CH3)	–	–
Y16	H18	PA11 (GPIO/TIM1_CH4)	–	–
B1	J18	PH10 (GPIO/TIM5_CH1)	–	–
B3	K18	PH11 (GPIO/TIM5_CH2)	–	–
W16	D17	PA12 (GPIO/TIM1_ETR)	GPIO_A0	P2-5
W3	E17	PA13 (GPIO/DBTRGI)	GPIO_A1	P2-7
R3	F17	PA14 (GPIO/DBTRGO)	GPIO_A2	P2-9
F11	G17	PB7 (GPIO/TIM4_CH2)	GPIO_A3	P2-11
AB8	H17	PB8 (GPIO/TIM4_CH3)	GPIO_A4	P2-13
F12	J17	PB9 (GPIO/TIM4_CH4)	GPIO_A5	P2-15
U10	K17	PC0 (GPIO)	GPIO_A6	P2-17
U3	L17	PC3 (GPIO)	GPIO_A7	P2-19
D13	D19	PC7 (GPIO)	–	–
F10	E19	PD7 (GPIO/USART2_CK)	–	–
M1	F19	PD8 (GPIO)	–	–
M2	G19	PD9 (GPIO)	–	–
E9	H19	PE6 (GPIO/TIM1_BKIN2)	–	–
F13	J19	PF2 (GPIO)	–	–
V3	K19	PF3 (GPIO)	–	–
W6	L19	PF15 (GPIO)	–	–
W4	D3	PG2 (GPIO)	–	–
U4	D4	PG3 (GPIO/CAN_STBY)	–	–
Y8	E3	PG8 (GPIO/ETH_CLK)	–	–
D10	E4	PG15 (GPIO)	–	–
A3	F3	PH4 (GPIO)	–	–
A2	F4	PH5 (GPIO)	–	–
D6	G3	PH8 (GPIO)	–	–
E6	G4	PH9 (GPIO)	–	–
F5	U32	PH12 (GPIO/TIM5_CH3)	–	–
C1	U33	PH15 (GPIO/TIM8_CH3N))	–	–
J6	V32	PI4 (GPIO/TIM8_BKIN)	–	–
F2	V33	PI5 (GPIO/TIM8_CH1)	–	–
G5	W32	PI6 (GPIO/TIM8_CH2)	GPIO_D4	–
F1	W33	PI7 (GPIO/TIM8_CH3)	–	–

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Table 3 – continued from previous page

CPU Pin	OSM Pin	MSMP1 Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
J5	Y32	PI9 (GPIO)	–	–
AA5	Y33	PB1 (GPIO/TIM1_CH3N)	GPIO_D7	–
VENDOR-DEFINED				
W8	B22	PF11/ADC1_IN2 (GPIO)	–	–
V8	C16	PF12/ADC1_IN6 (GPIO)	–	–
AA3	P16	PA0/ADC1_IN16 (GPIO)	–	–
W9	D6	PA6/ADC2_IN3 (GPIO)	–	–
V7	D7	PF14/ADC2_IN6 (GPIO)	–	–
AB5	Y29	PB0/ADC2_IN9 (GPIO)	–	–
N4	Y30	BOOT1	–	–
P4	Y31	BOOT2	VD-Y31/BOOT2	P4-50
J2	AA29	LCD_R1	–	–
H6	AA30	LCD_G1	–	–
A7	AA31	LCD_B1	–	–
CONFIG/JTAG				
D17	N17	JTAG_TCK	JTAG_TCK	P2-18
E17	N19	JTAG_TMS	JTAG_TMS	P2-16
D16	P17	JTAG_TDI	JTAG_TDI	P2-14
E16	R17	JTAG_TDO	JTAG_TDO	P2-12
E15	R19	JTAG_nTRST	JTAG_TRST#	P2-10
RGB-DISPLAY				
L6	Y7	LCD_R2	RGB_R2	P3-50
K4	AA7	LCD_R3	RGB_R3	P3-48
J1	Y6	LCD_R4	RGB_R4	P3-46
K2	AA5	LCD_R5	RGB_R5	P3-44
K1	Y5	LCD_R6	RGB_R6	P3-42
L5	Y4	LCD_R7	RGB_R7	P3-40
L2	W4	LCD_G2	RGB_G2	P3-36
J3	V3	LCD_G3	RGB_G3	P3-34
K6	V4	LCD_G4	RGB_G4	P3-32
D8	U3	LCD_G5	RGB_G5	P3-30
E7	T3	LCD_G6	RGB_G6	P3-28
E8	T4	LCD_G7	RGB_G7	P3-26
B7	R4	LCD_B2	RGB_B2	P3-22
C7	R3	LCD_B3	RGB_B3	P3-20
B6	P3	LCD_B4	RGB_B4	P3-18
A6	N3	LCD_B5	RGB_B5	P3-16
C6	N4	LCD_B6	RGB_B6	P3-14
A5	M3	LCD_B7	RGB_B7	P3-12
D2	M4	LCD_CLK	RGB_CLK	P3-8
H1	L3	LCD_VSYNC	RGB_VSYNC	P3-6
H2	K3	LCD_HSYNC	RGB_HSYNC	P3-4
T4	K4	LCD_BL_CTRL	–	–
B5	J4	LCD_DE	RGB_DE	P3-2
R2	J3	NRST	–	–
T3	H3	PI11 (GPIO)	–	–
MIPI-DSI				

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Table 3 – continued from previous page

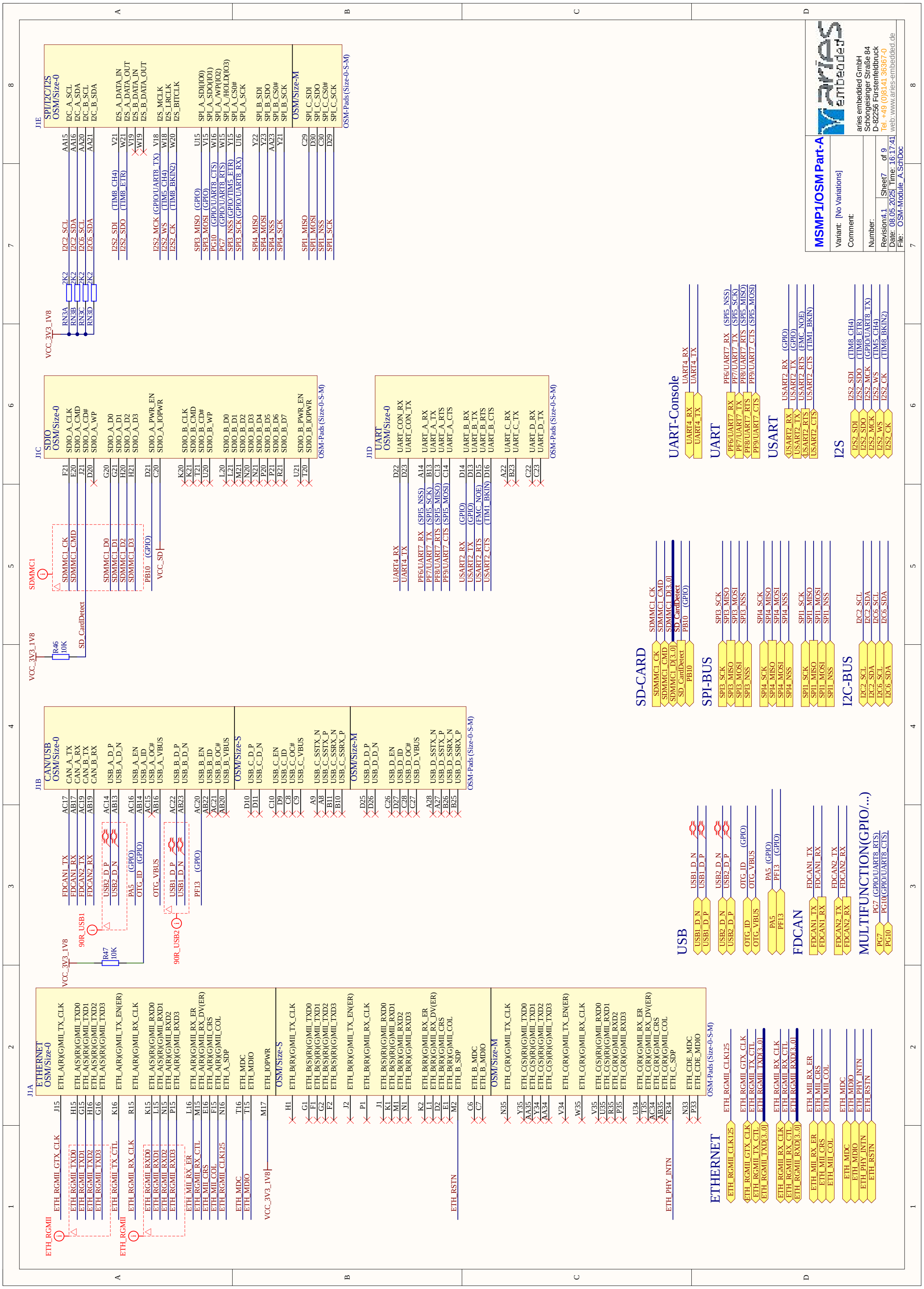
CPU Pin	OSM Pin	MSMP1 Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
A15	AB11	DSI_DATA0_N (Diff.)	DSI_DATA0_N	P3-49
B15	AB10	DSI_DATA0_P (Diff.)	DSI_DATA0_P	P3-47
A17	AC9	DSI_DATA1_N (Diff.)	DSI_DATA1_N	P3-43
B17	AC8	DSI_DATA1_P (Diff.)	DSI_DATA1_P	P3-41
A16	AB8	DSI_CLK_N (Diff.)	DSI_CLK_N	P3-37
B16	AB7	DSI_CLK_P (Diff.)	DSI_CLK_P	P3-35
V14	AA3	PD13/DSI_TE (GPIO)	DSI.TE	P3-31
PWR				
R2	U17	NRST	SYS_RST#	P4-29
V1	V17	CAR_PWR_EN	CARRIER_PWR_EN	P4-31
N3	U19	BOOT0	BOOT_SEL0#	P4-46
N4	R18	BOOT1	BOOT_SEL1#	P4-48

CPU Pin	OSM Pin	MSMP1 Function	OSMEVK_ADAP Function	OSMEVK Connector Pin
COM				
M3	A15	PD14 (GPIO/FMC_AD0)	–	–
L1	A16	PD15 (GPIO/FMC_AD1)	–	–
C10	A17	PD0 (GPIO/FMC_AD2/I2C5_SDA)	–	–
B10	A18	PD1 (GPIO/FMC_AD3/I2C5_SCL)	–	–
W10	A19	PE7 (GPIO/FMC_AD4/QSPI_BK2_IO0)	–	–
Y12	A20	PE8 (GPIO/FMC_AD5/QSPI_BK2_IO1)	–	–
W11	A21	PE9 (GPIO/FMC_AD6/QSPI_BK2_IO2)	–	–
W14	B15	PE10 (GPIO/FMC_AD7/QSPI_BK2_IO3)	–	–
AB9	B16	PD11 (GPIO/FMC_CLE)	–	–
W12	B17	PD12 (GPIO/FMC_ALE/TIM4_CH1)	–	–
L3	B18	PD6 (GPIO/FMC_NWAIT)	–	–
A9	B19	PD5 (GPIO/FMC_NWE)	–	–
W15	B20	PG9 (GPIO/FMC_NCE)	–	–
N2	C15	PC13 (RTC_OUT1)	–	–
F3	C17	LCD_R0	–	–
L4	C19	LCD_G0	–	–
B8	C21	LCD_B0	–	–

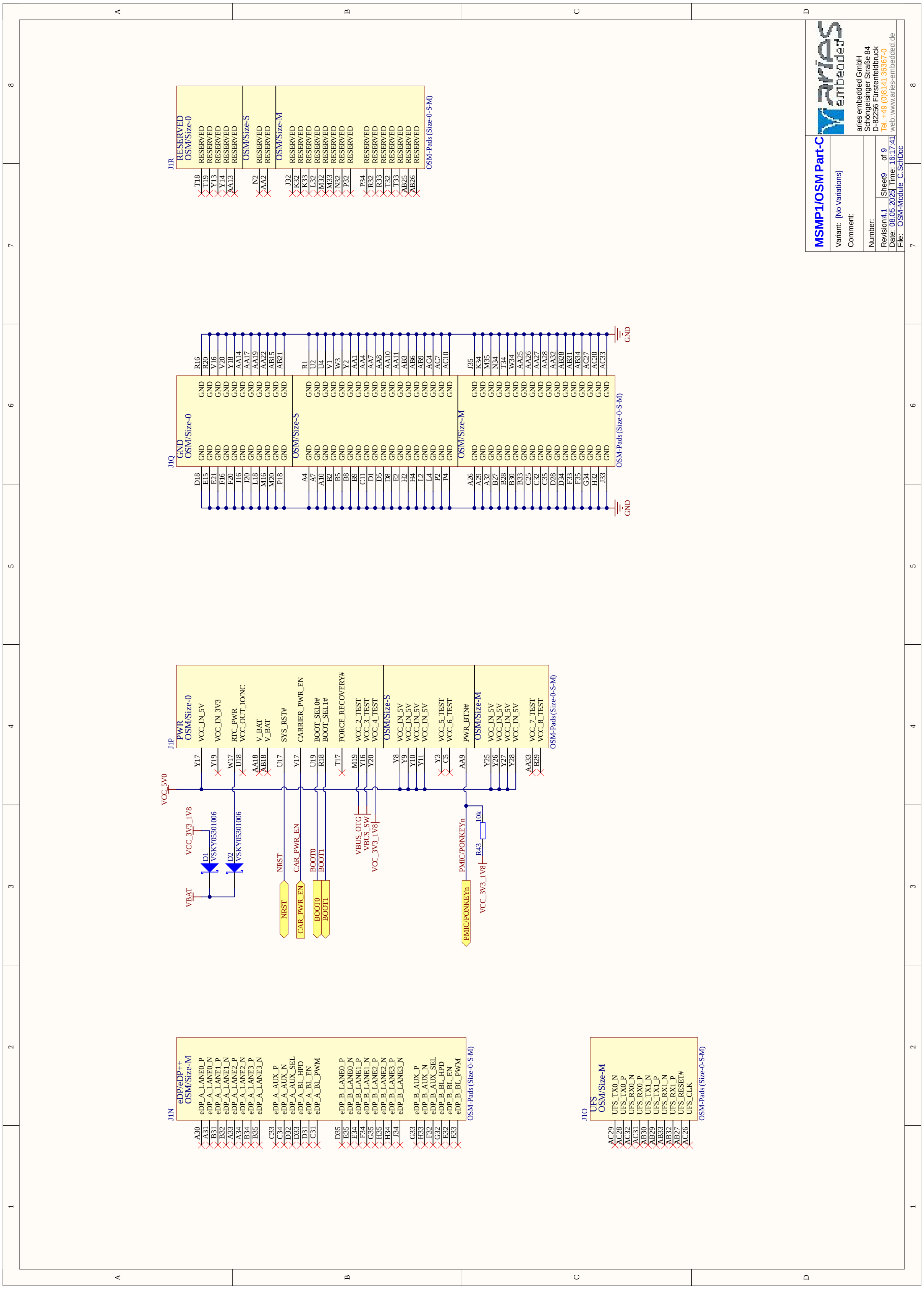
4.4 Schematics

Schematics for the MSMP1 SiP may be obtained on request. Please contact sales@aries-embedded.de.

Below the OSM schematics footprint is shown:


MSMP1/OSM Part-A
ETHERNET
USB
FDCAN
MULTIFUNCTION(GPIO/...)
SD-CARD
SPI-BUS
I2C-BUS
UART-Console
UART
USART
I2S


MULTIFUNCTION(GPIO/...)
COM/FMC
JTAG
DISPLAY(MIPI)
DISPLAY(RGB)
ADC
MSMP1/OSM Part-B
aries embedded GmbH
Schöngeisinger Straße 84
D-82256 Fürstenfeldbruck
web: www.aries-embedded.de


MSMP1/OSM Part-C
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File: OSM-Module_C.SchDoc