MCXL Hardware Manual

Release 1.0

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

1.6 Change Log

Revision	Date	Revised	Comment
1.0	05.05.2021	dk	Initial creation
1.1	19.01.2022	dk	PMod connectors are designed upside-down New diagram for MCXL-H055BBB-I The header is micro JTAG
1.2	16.02.2024	aw	Added measurements for mounting holes

CHAPTER

TWO

OVERVIEW

2.1 MCXL System on Module

The MCXL SoM leverages the functionality of the Cyclone 10 LP family on a compact embedded module. Intel Cyclone 10 LP FPGAs are ideal for cost-sensitive applications that require increasing lower static power as the need for scalable processing acceleration increases system interface requirements. MCXL SoM is the FPGA SoM featuring Hyperbus Technology.

2.2 Feature Set

- Microchip PolarFire FPGA
  - MCXL-H055BBB-I- 2x128MBit HyperRAM and 2x512MBit HyperFlash
  - MCXL-S055BC-I - 512Mbit SDRAM and 256Mbit QSPI Flash
- 10CL055YU484I7G Cyclone 10 FPGA, 55KLE
- Configuration device 256 Mbit
- Gigabit Ethernet Phy & connector
- 221 FPGA Pins
- **Cyclone 10LP**
  - 10CL016YU484C7N
  - 10CL040YU484C7N
  - 10CL055YU484C7N
- 4 User LEDs
- micro JTAG pin header
- Clock generation
- on board 2.5V and 1.2V power supply
- size 37mmx90mm

2.3 Order Codes

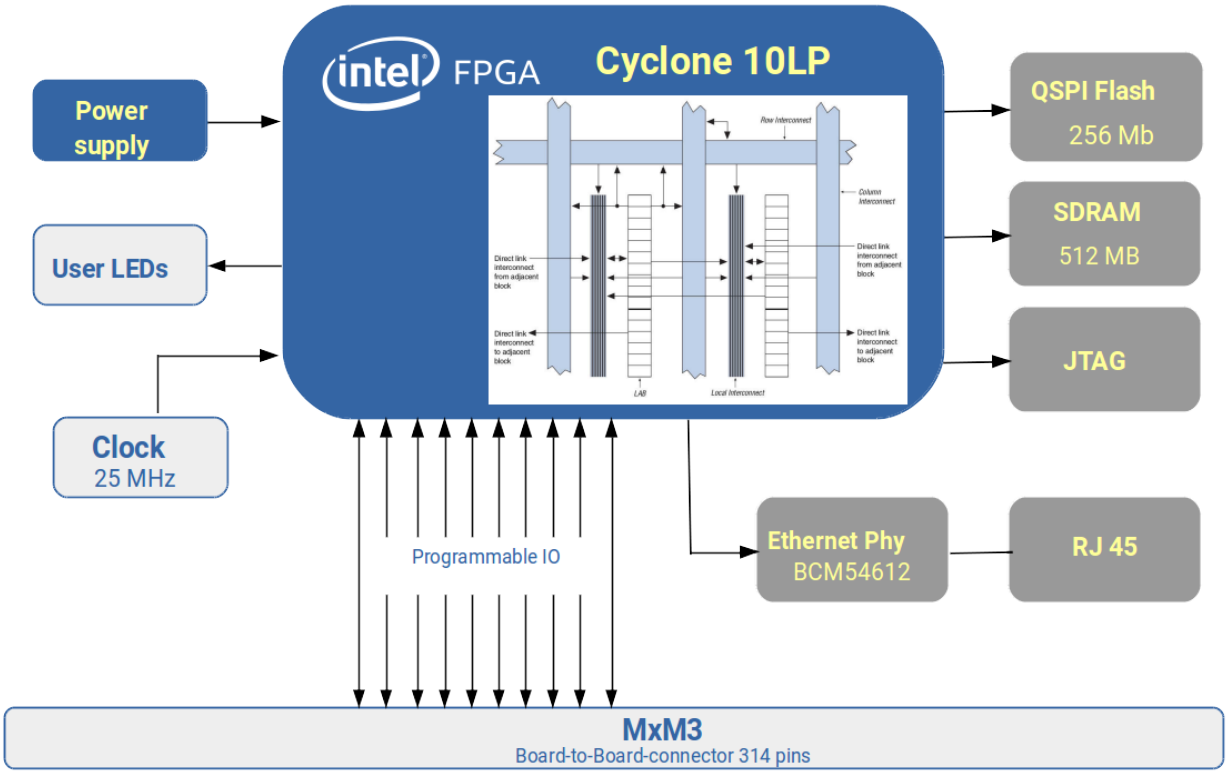
The MCXL SoM is available in the following standard configurations:

- **MCXL-H055BBB-I**
  - 10CL055YU484I7G Cyclone 10 FPGA
  - Configuration device 256 Mbit
  - Gigabit Ethernet Phy & connector
  - 221 FPGA Pins
  - size 37mm x 90mm
  - 0°C…+70°C
- **MCXL-S055BC-I**
  - 10CL055YU484I7G Cyclone 10 FPGA
  - 512Mbit SDRAM
  - Gigabit Ethernet Phy & connector
  - 221 FPGA Pins
  - size 37mm x 90mm
  - 0°C…+70°C

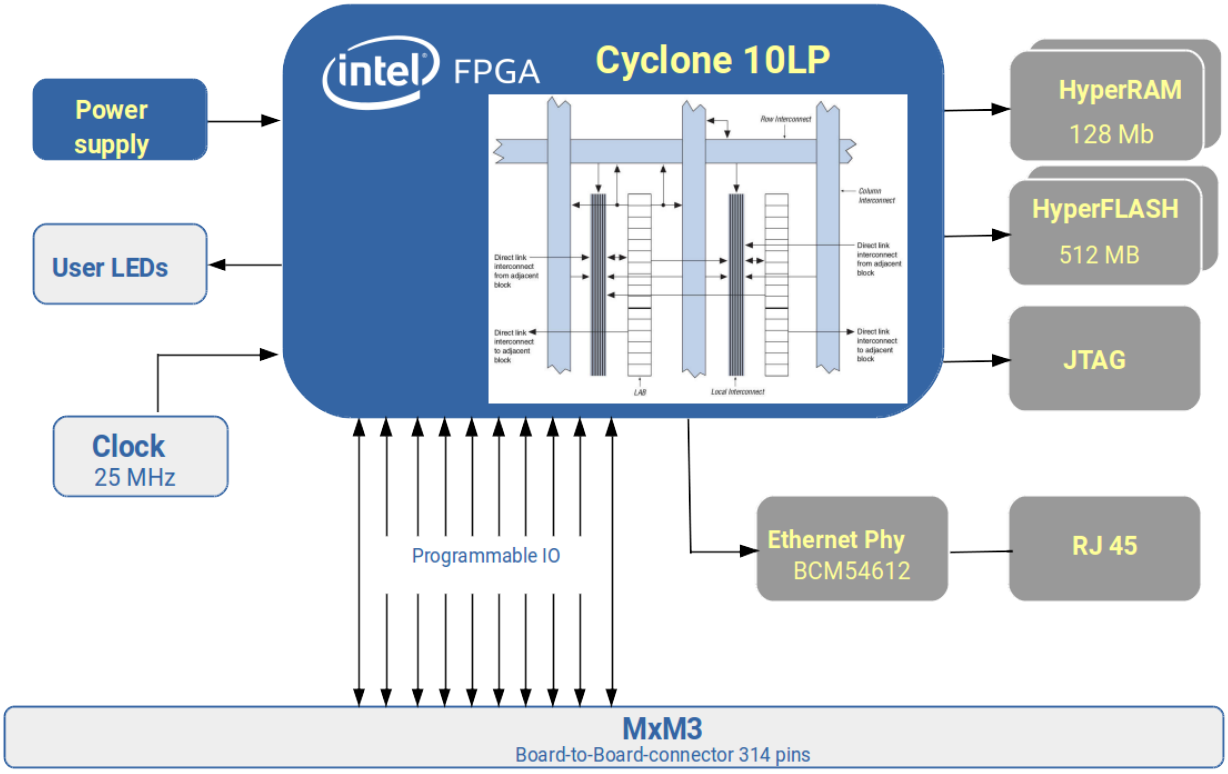
Please contact ARIES Embedded for more information about the availability of other standard products of MCXL or custom configurations.

2.4 Block Diagram

MCXL-S055BC-I

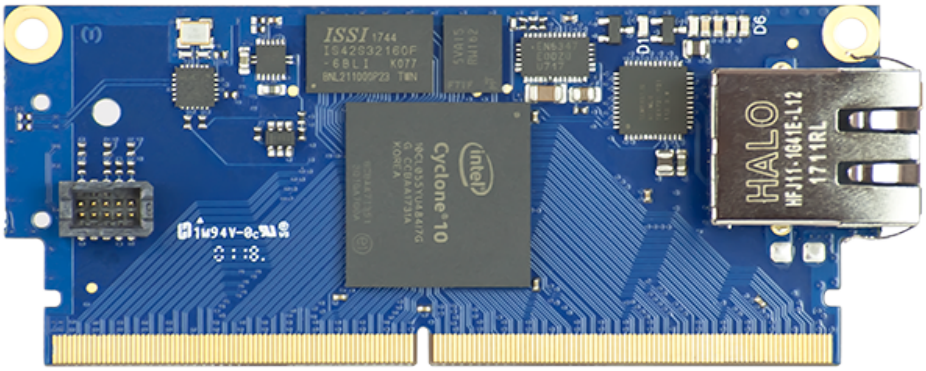


MCXL-H055BBB-I

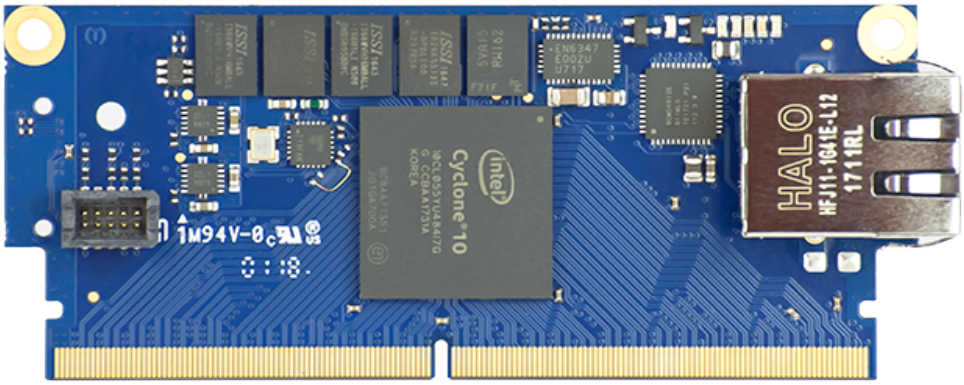


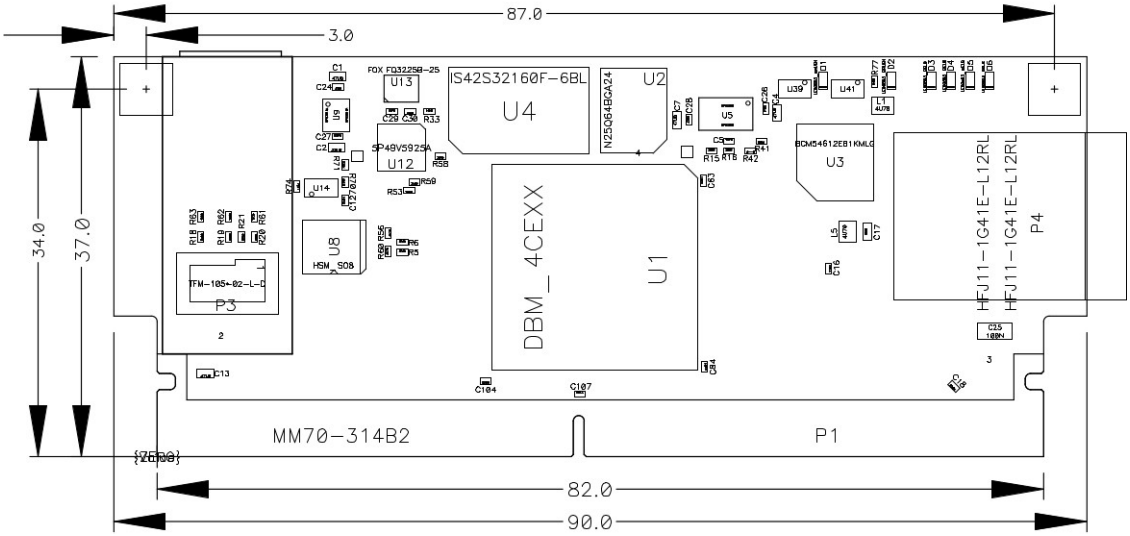
2.5 Dimensions

MCXL-S055BC-I



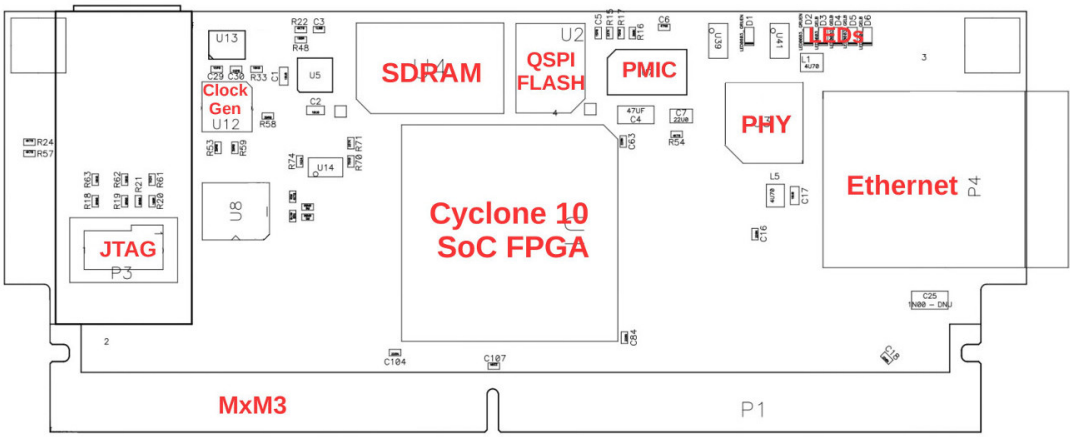
MCXL-H055BBB-I



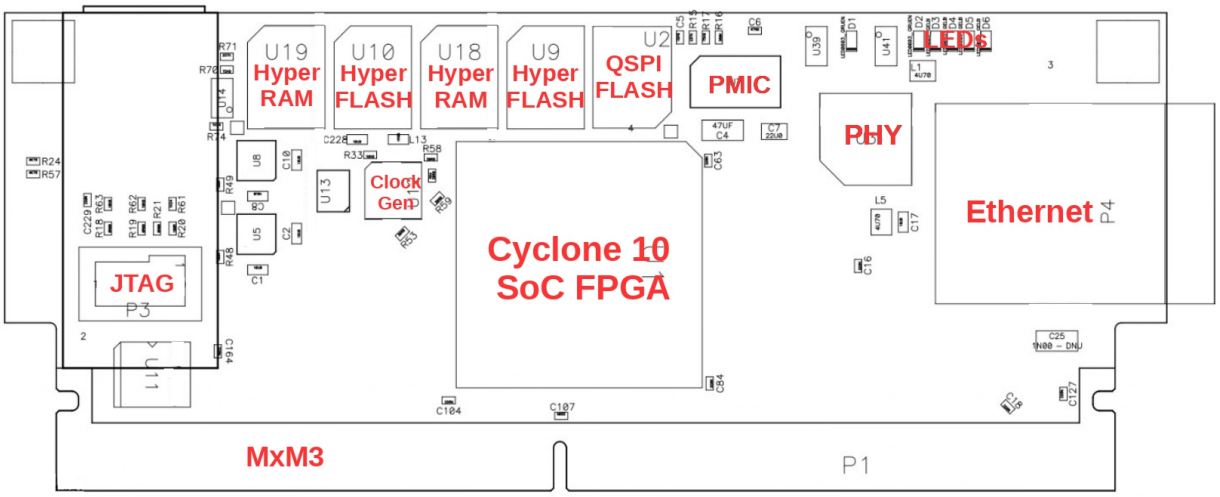


2.6 Part Overview

MCXL-S055BC-I



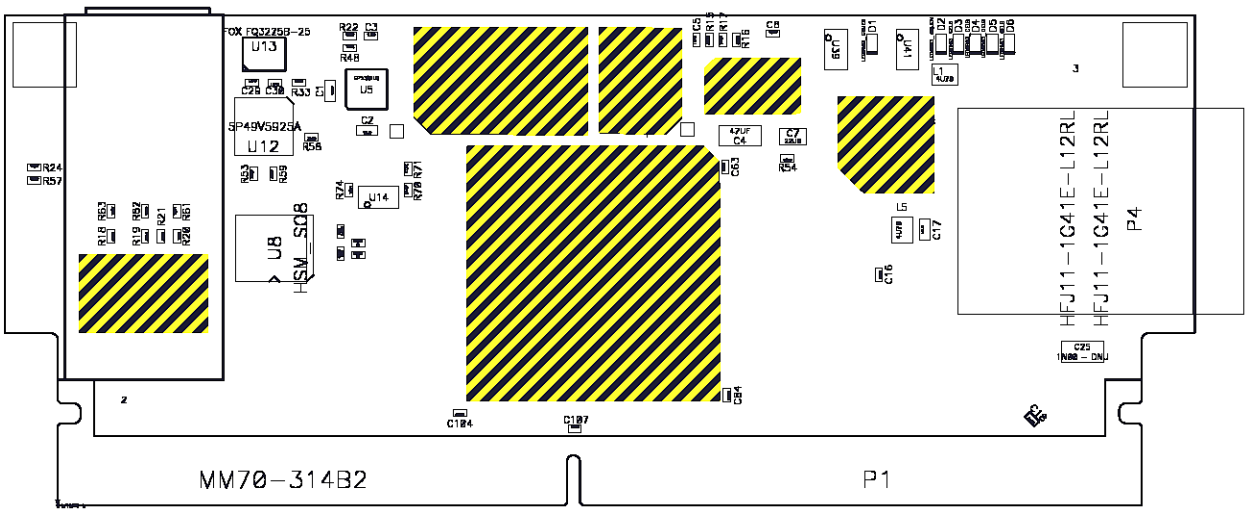
MCXL-H055BBB-I



2.7 Handling Recommendations

To avoid mechanical damage to the components populated on MCXL it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:

MCXL-S055BC-I



MCXL-H055BBB-I

CHAPTER

THREE

RESOURCES

3.1 Components

3.1.1 FPGA

The Intel Cyclone 10 LP FPGA on the MCXL comes in the FCG484 (23x23, 1.0 mm) package and provides up to 20 GCLK networks that drive throughout the device.

Devices	10CL016	10CL040	10CL055
Logic Elemets	15,408	39,600	55,856
Math Blocks (18x18 MACC)	56	126	156
Maximum LVDS	137	124	132
Maximum User I/O	340	325	321
SRAM M9K Kbits	504 Kbits	1,134 Kbits	2,340 Kbits
SRAM M9K Blocks	56	126	260
User PLL's	4	4	4

For more information about the Intel Cyclone 10 LP FPGA please refer to the documentation which is available from Intel.

3.1.2 Memory Types

The MCXL SoM supports

- 2x128MBit HyperRAM and 2x512MBit HyperFlash in MCXL-H055BBB-I

  or

- 512Mbit SDRAM in MCXL-S055BC-I

3.1.3 SDRAM in MCXL-S055BC-I

The MCXL-S is equipped with 1 block of ISSI, Integrated Silicon Solution Inc IS42S32160F-6BL resulting in up to 512 MB of 32bit SDRAM memory. The memory interface is clocked at 166MHz using the 3.3V SDRAM standard interface. The Clock is generated out of the FPGA. A respective free of charge IP-Core is available from Intel.

FPGA Signals for SDRAM

Function	SDRAM Pin	FPGA Pin		Function	FPGA Pin	SDRAM Pin
SD_CLK	J1	W2		SD_D0	R8	M2
SD_CKE	J2	W1		SD_D1	N7	N2
SD_CS	J8	N6		SD_D2	R9	M1
SD_RAS	J9	L6		SD_D3	N8	N1
SD_CAS	K7	R5		SD_D4	P9	M4
SD_WE	K8	M6		SD_D5	M8	M3
SD_DQM0	K9	P4		SD_D6	M7	M5
SD_DQM1	K1	V2		SD_D7	L8	P3
SD_DGM2	F8	R6		SD_D8	L2	V1
SD_DQM3	F2	AA3		SD_D9	M3	N5
SD_A0	G8	P6		SD_D10	M2	U2
SD_A1	G9	N7		SD_D11	P1	R1
SD_A2	F7	P7		SD_D12	N2	U1
SD_A3	F3	V5		SD_D13	R1	P2
SD_A4	G1	AB3		SD_D14	N3	R2
SD_A5	G2	Y3		SD_D15	R2	P1
SD_A6	G3	Y4		SD_D16	E8	V6
SD_A7	H1	Y2		SD_D17	D7	Y6
SD_A8	H2	Y1		SD_D18	D8	W6
SD_A9	J3	T5		SD_D19	B9	V7
SD_A10	G7	V4		SD_D20	C8	Y7
SD_A11	H9	V3		SD_D21	A9	U7
SD_A12	H3	T4		SD_D22	C7	U8
SD_BA0	J7	T3		SD_D23	A8	V8
SD_BA1	H8	P5		SD_D24	A2	W8
SD_D25	C3	AA5		SD_D26	A1	U9
SD_D27	C2	AB5		SD_D28	B1	Y8
SD_D29	D2	AA4		SD_D30	D3	W7
SD_D31	E2	AB4		–	–	–

3.1.4 HyperRam and HyperFlash in MCXL-H055BBB-I

The MCXL-H is equipped with two IS66WVH8M8-ALL-166B1L1 128MBit HyperRAM and two S26KS512S 512MBit HyperFlash.

The IS66WVH8M8-ALL-166B1L1 manufactured by ISSI, Integrated Silicon Solution Incare two integrated memory devices resulting in up to 256MB of 64Mbit Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 8M words by 8bits.

The S26KS512S manufactured by Cypress Semiconductor are two high-speed CMOS MirrorBit NOR flash devices resulting in up to 1024 MB of 64bit HyperFlash memory.

The memory interface is clocked at 166MHz using the 1.8V standard interface. The Clock is generated out of the FPGA. A respective free of charge IP-Core is available from Intel

FPGA Signals from HyperFlash

Function	HyperFlash Pin	FPGA Pin		Function	HyperFlash Pin	FPGA Pin
HyperFlash U9				**HyperFlash U10**		
RSTN	A4	–		RSTN	A4	–
HB1CS0	C2	P1		HB2CS0	C2	Y2
HB1CK0	B2	U2		HB2CK0	B2	T4
HB1CK0	B1	U1		HB2CK0	B1	T5
HB1RST	A2	M6		HB2RST	A2	T3
HB1INT	A5	M5		HB2INT	A5	R5
HB1RWDS	C3	M4,T2		HB2RWDS	B1	P3,T1
HB1DQ0	D3	N1		HB2DQ0	D3	W2
HB1DQ1	D2	R1		HB2DQ1	D2	P6
HB1DQ2	C4	M2		HB2DQ2	C4	V1
HB1DQ3	D4	N2		HB2DQ3	D4	W1
HB1DQ4	D5	M1		HB2DQ4	D5	V2
HB1DQ5	E3	M3		HB2DQ5	E3	Y1
HB1DQ6	E2	P2		HB2DQ6	E2	P7
HB1DQ7	E1	R2		HB2DQ7	E1	R6

FPGA Signals from HyperRAM

Function	HyperRAM Pin	FPGA Pin		Function	HyperRAM Pin	FPGA Pin
HyperRAM U18				**HyperRAM U19**		
RSTN	A4	–		RSTN	A4	–
HB1CS1	A3	L6		HB2CS1	A3	P4
HB1CK1	B2	N6		HB2CK1	B2	V3
HB1CK1	B1	N5		HB2CK1	B1	V4
HB1RWDS	C3	M4,T2		HB2RWDS	B1	P3,T1
HB1DQ0	D3	N1		HB2DQ0	D3	W2
HB1DQ1	D2	R1		HB2DQ1	D2	P6
HB1DQ2	C4	M2		HB2DQ2	C4	V1
HB1DQ3	D4	N2		HB2DQ3	D4	W1
HB1DQ4	D5	M1		HB2DQ4	D5	V2
HB1DQ5	E3	M3		HB2DQ5	E3	Y1
HB1DQ6	E2	P2		HB2DQ6	E2	P7
HB1DQ7	E1	R2		HB2DQ7	E1	R6

3.1.5 QSPI Flash

The MCXL is equipped with 1 block of 256Mbit QSPI Flash Memory. A Micron N25Q256, 256Mbit NOR flash device can be used for FPGA configuration and as external storage for data or NIOS Code. For FPGA configuration the device has to be set into SPI Mode. After the configuration the device can be used in quad mode. Respective IP Cores are available from Intel and devboards (DB_EPCQ). On MCXL is the N25Q256BGA24 device available.

FPGA Pin	Function	QSPI Pin
K2	DCLK	B2
K1	DATA0	D2
D1	DATA1	D3
J1	DATA2	C4
J2	DATA3	D4
E2	DCS	C2
T1	RST	A4
–	GND	B3
–	3.3V	B4

3.1.6 PMIC

Power on the MCXL is controlled by a EN6347QI Intel Enpirion Power System on a Chip (PowerSoC) DC-DC converter. It integrates the inductor, MOSFET switches, small-signal circuits and compensation in an advanced 4mm x 7mm x 1.85mm 38-pin QFN package.

3.1.7 User LEDs

The four signals, that can be used to read the Ident value of the board, are connected via a Buffer to four LEDs. To read the ident value, enable the internal Pull-Ups and to set the ident value four 1K resistors can be equipped to set a "zero" to the respective signal. If no resistor is equipped a "one" is red.

Function	Signal	Connector	Pulldown
LED1	B1IO0	H6	R1
LED2	B1IO1	J6	R2
LED3	B1IO2	J7	R3
LED4	B1IO3	K7	R4

3.2 Clocking

The clocking scheme on the MCXL is generated by an IDT programmable Clock Generator 5P49V5925. Its base is sourced from a 25 MHz oscillator to generate the required clocks for the board's components. The device provides one 25MHz clock to the Gigabit Ethernet Phy and two clocks to the FPGA (in MCXL-H055BBB-I configuartion one more clock to the Hyperbus). The FPGA clocks can be programmed on customer request. The I2C interface signals for reprogramming of the device are available on the pin header P2 (service header).

Function	Pin FPGA	Pin PHY	Oscillator
CLK25A	T2	–	25MHz, 3.3V
CLK25B	G1	–	25MHz, 3.3V
CLK25PHY	–	8	25MHz, 3.3V

The MCXL-H055BBB-I has one more clock :

Function	Pin FPGA	Pin PHY	Oscillator
CLK-HB	P5	–	25MHz, 1.8V

3.3 I2C

The The Intel Cyclone 10 LP FPGA on the MCXL is connected to I2C bus as master.

Address	Device	Description
0xD0 0xD4	5P49V5925 Clock Generator	Allows reconfiguration of the clocks present on MCXL
Master	MCXL FPGA	Connected to FPGA Pins W10 (SCL) and Y10 (SDA)

Function	Connector	FPGA Pin	Function
SPI_SEL:I2C_SDA	P1-5	Y10	B3IO0
SPI_SS_I2C_SCL	P1-6	W10	B3IO1
IDT_SDA	P2-10	–	–
IDT_SCL	P2-9	–	–

3.4 micro JTAG

The MCXL Baseboard provides a micro JTAG TFM-105-02-L-D header.

Function	FPGA Pin	Connector
TCK	L2	P3-1
TMS	L1	P3-5
TDI	L5	P3-9
TDO	L4	P3-3
TRSTB	–	–
VIO	–	–

3.5 Pin Out

3.5.1 PHY Ethernet

The MCXL module is equipped with a Broadcom Gigabit Ethernet Phy BCM54612EB1KMLG which is connected via RGMII to the FPGA.

Function	FPGA Pin		Function	FPGA Pin		Function	FPGA Pin
EMC_RSTN	J3		EMC_MDIO	B1		EMC_TXD0	E3
EMC_RX_CLK	J4		EMC_MDC	B2		EMC_TX_CTL	F1
EMC_RX_CTL	G3		EMC_TXD3	F2		EMC_TX_CLK	E4
EMC_RXD0	E1		EMC_TXD2	G4		EMC_RXD3	H1
EMC_RXD1	H2		EMC_TXD1	O2		EMC_RXD2	J5

Function	Connector
EMC_TRD0+	P4-2
EMC_TRD0-	P4-3
EMC_TRD1+	P4-4
EMC_TRD1-	P4-5
EMC_TRD2+	P4-6
EMC_TRD2-	P4-7
EMC_TRD3+	P4-8
EMC_TRD3-	P4-9

3.5.2 Connectors

Connector P1 in MCXL-S055BC-I

The MM70-314B2 is designed as card edge connector in SMARC 314 format. For the MXCL Baseboard is used the JAE MM70 MxM3 Connector.

Below are tables with the pins of the connector and their corresponding function.

Pin	Function	FPGA		Pin	Function	FPGA
Connector P1:A						
1	3.3V	–		2	3.3V	–
3	3.3V	–		4	GND	–
5	B3IO0	Y10		6	B3IO1	W10
7	B3IO2	V10		8	B3IO3	U10
9	GND	–		10	B3IO4	V11
11	B3IO5	U11		12	B3IO6	T11
13	B3IO7	T10		14	GND	–
15	B3IO8	AB7		16	B3IO9	AA7
17	B3IO10	AB8		18	B3IO11	AA8
19	GND	–		20	B3IO12	AB9
21	B3IO13	AA9		22	B3IO14	AB10
23	B3IO15	AA10		24	GND	–
25	B3IN0	AB11		26	B3IN1	AA11
27	B4IO0	V12		28	B4IO1	U12

continues on next page

Table 1 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
29	GND	–		30	B4IO2	T15
31	B4IO3	T14		32	B4IO4	U17
33	B4IO5	U16		34	GND	–
35	B4IN0	AB12		36	B4IN1	AA12
37	B4IO6	AB13		38	B4IO7	AA13
39	GND	–		40	B4IO8	AB14
41	B4IO9	AA14		42	B4IO10	AB15
43	B1IO11	AA15		44	GND	–
45	B4IO12	AB16		46	B4IO13	AA16
47	B4IO14	AB18		48	B4IO15	AA18
49	GND	–		50	B4IO16	AB19
51	B4IO17	AA19		52	B4IO18	AB20
53	B4IO19	AA20		54	GND	–
55	B5IO0	W19		56	B5IO1	AA21
57	B5IO2	Y22		58	B5IO3	Y21
59	GND	–		60	B5IO4	W22
61	B5IO5	W21		62	B5IO6	V22
63	B5IO7	V21		64	GND	–
65	B5IO8	U22		66	B5IO9	U21
67	B5IN0	T22		68	B5IO1	T21
69	GND	–		70	B5IO10	R22
71	B5IO11	R21		72	B5IO12	P22
73	B5IO13	P21		74	GND	–
Connector P1:B						
75	B5IO14	N22		76	B5IO15	N21
77	B5IO16	M22		78	B5IO17	M21
79	GND	–		80	B6IO0	L22
81	B6IO1	L21		82	B6IO2	K22
83	B6IO3	K21		84	GND	–
85	B6IO4	J22		86	B6IO5	J21
87	B6IO6	H22		88	B6IO7	H21
89	GND	–		90	B6IN0	G22
91	B6IN1	G21		92	B6IO8	F22
93	B6IO9	F21		94	GND	–
95	B6IO10	E22		96	B6IO11	E21
97	B6IO12	D22		98	B6IO13	D21
99	GND	–		100	B6IO14	C22
101	B6IO15	C21		102	B6IO16	B22
103	B6IO17	B21		104	GND	–
105	B7IO0	A20		106	B7IO1	B20
107	B7IO2	A19		108	B7IO3	B19
109	GND	–		110	B7IO4	A18
111	B7IO5	B18		112	B7IO6	A17
113	B7IO7	B17		114	GND	–
115	B7IO8	A16		116	B7IO9	B16
117	B7IO10	A15		118	B7IO11	B15
119	GND	–		120	B7IO12	A14
121	B7IO13	B14		122	B7IO14	A13
123	B7IO15	B13		124	GND	–

continues on next page

Table 1 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
125	B7IO38	G14		126	B7IN0	A12
127	B7IN1	B12		128	B8I038	D6
129	GND	–		130	B8IN0	A11
131	B8IN1	B11		132	B8IO20	A10
133	B8IO21	B10		134	GND	–
135	B8IO22	A9		136	B8IO23	B9
137	B8IO24	A8		138	B8IO25	B8
139	GND	–		140	B8IO26	A7
141	B8IO27	B7		142	B8IO28	A6
143	B8IO29	B6		144	GND	–
145	B8IO30	A5		146	B8IO31	B5
147	B8IO32	A4		148	B8IO33	B4
149	GND	–		150	B8IO34	A3
151	B8IO35	B3		152	B8IO36	F7
153	B8IO37	G7		154	GND	–
155	HW_RST	–		156	GND	–
Connector P1:A						
157	3.3V	–		158	3.3V	–
159	3.3V	–		160	3.3V	–
161	GND	–		162	–	–
163	–	–		164	–	–
165	–	–		166	3.3V	–
167	–	–		168	–	–
169	–	–		170	–	–
171	3.3V	–		172	–	–
173	–	–		174	–	–
175	–	–		176	3.3V	–
177	–	–		178	–	–
179	–	–		180	–	–
181	3.3V	–		182	–	–
183	–	–		184	–	–
185	–	–		186	3.3V	–
187	B4IO20	R15		188	B4IO21	R14
189	B4IO22	V13		190	B4IO23	U13
191	VCCIO4	–		192	B4IO24	U14
193	B4IO25	V14		194	B4IO26	Y13
195	B4IO27	W13		196	VCCIO4	–
197	B4IO28	V15		198	B4IO29	U15
199	B4IO30	Y17		200	B4IO31	W17
201	VCCIO4	–		202	B4IO32	R16
203	B4IO33	T16		204	B4IO334	W14
205	B4IO35	W15		206	VCCIO4	–
207	B4IO36	V16		208	RST	–
209	B5IO18	U20		210	B5IO19	U19
211	GND	–		212	B5IO20	R17
213	B5IO21	W20		214	B5IO22	T17
215	B5IO23	T18		216	VCCIO5	–
217	B5IO24	R18		218	B5IO25	R19
219	B5IO26	R20		220	B5IO27	P20

continues on next page

Table 1 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
221	VCCIO5	–		222	B5IO28	P17
223	B5IO29	N16		224	B5IO30	N17
225	B5IO31	N18		226	VCCIO5	–
227	B5IO32	N20		228	B5IO33	N19
229	B5IO34	M20		230	B5IO35	M19
231	VCCIO5	–		232	B5IO36	M16
Connector P1:B						
233	B6IO34	K19		234	B6IO18	K17
235	B6IO19	K18		236	VCCIO6	–
237	B6IO20	J18		238	B6IO21	H18
239	B6IO22	G18		240	B6IO23	H17
241	VCCIO6	–		242	B6IO24	J17
243	B6IO25	H16		244	B6IO26	H20
245	B6IO27	H19		246	VCCIO6	–
247	B6IO28	F20		248	B6IO29	F19
249	B6IO30	D20		250	B6IO31	C20
251	VCCIO6	–		252	B6IO32	F17
253	B6IO33	G17		254	B7IO16	–
255	B7IO17	D17		256	GND	–
257	B7IO18	C15		258	B7IO19	D15
259	B7IO20	C19		260	B7IO21	D19
261	VCCIO7	–		262	B7IO22	F15
263	B7IO23	G16		264	B7IO24	F16
265	B7IO25	E16		266	VCCIO7	–
267	B7IO26	C13		268	B7IO27	D13
269	B7IO28	G13		270	B7IO29	F13
271	VCCIO7	–		272	B7IO30	E15
273	B7IO31	E14		274	B7IO32	E13
275	B7IO33	E12		276	VCCIO7	–
277	B7IO34	E11		278	B7IO35	F11
279	B7IO36	G15		280	B7IO37	F14
281	GND	–		282	B8IO0	G10
283	B8IO1	F10		284	B8IO2	D10
285	B8IO3	E10		286	VCCIO8	–
287	B8IO4	G11		288	B8IO5	C10
289	B8IO6	G9		290	B8IO7	F9
291	VCCIO8	–		292	B8IO8	C8
293	B8IO9	C7		294	B8IO10	E9
295	B8IO11	E7		296	VCCIO8	–
297	B8IO12	C6		298	B8IO13	D7
299	B8IO14	F8		300	B8IO15	G8
301	VCCIO8	–		302	B8IO16	E5
303	B8IO17	E5		304	B8IO18	C3
305	B8IO19	C4		306	VCCIO8	–
307	B1IO0	H6		308	B1IO1	J6
309	B1IO2	J7		310	B1IO3	K7
311	GND	–		312	B1IO4	H5
313	B1IO5	H7		314	GND	–

Connector P1 in MCXL-H055BBB-I

Connector P1 is designed as card edge connector in SMARC 314 format. For the MXCL Baseboard is used the JAE MM70 Connector.

Below are tables with the pins of the connector and their corresponding function.

Pin	Function	FPGA		Pin	Function	FPGA
Connector P1:A						
1	3.3V	–		2	3.3V	–
3	3.3V	–		4	GND	–
5	B3IO0	V5		6	B3IO1	V6
7	B3IO2	AB5		8	B3IO3	AA5
9	GND	–		10	B3IO4	V11
11	B3IO5	U11		12	B3IO6	T11
13	B3IO7	T10		14	GND	–
15	B3IO8	AB7		16	B3IO9	AA7
17	B3IO10	AB8		18	B3IO11	AA8
19	GND	–		20	B3IO12	AB9
21	B3IO13	AA9		22	B3IO14	AB10
23	B3IO15	AA10		24	GND	–
25	B3IN0	AB11		26	B3IN1	AA11
27	B4IO0	V12		28	B4IO1	U12
29	GND	–		30	B4IO2	T15
31	B4IO3	T14		32	B4IO4	U17
33	B4IO5	U16		34	GND	–
35	B4IN0	AB12		36	B4IN1	AA12
37	B4IO6	AB13		38	B4IO7	AA13
39	GND	–		40	B4IO8	AB14
41	B4IO9	AA14		42	B4IO10	AB15
43	B1IO11	AA15		44	GND	–
45	B4IO12	AB16		46	B4IO13	AA16
47	B4IO14	AB18		48	B4IO15	AA18
49	GND	–		50	B4IO16	AB19
51	B4IO17	AA19		52	B4IO18	AB20
53	B4IO19	AA20		54	GND	–
55	B5IO0	W19		56	B5IO1	AA21
57	B5IO2	Y22		58	B5IO3	Y21
59	GND	–		60	B5IO4	W22
61	B5IO5	W21		62	B5IO6	V22
63	B5IO7	V21		64	GND	–
65	B5IO8	U22		66	B5IO9	U21
67	B5IN0	T22		68	B5IO1	T21
69	GND	–		70	B5IO10	R22
71	B5IO11	R21		72	B5IO12	P22
73	B5IO13	P21		74	GND	–
Connector P1:B						
75	B5IO14	N22		76	B5IO15	N21
77	B5IO16	M22		78	B5IO17	M21
79	GND	–		80	B6IO0	L22
81	B6IO1	L21		82	B6IO2	K22
83	B6IO3	K21		84	GND	–

continues on next page

Table 2 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
85	B6IO4	J22		86	B6IO5	J21
87	B6IO6	H22		88	B6IO7	H21
89	GND	–		90	B6IN0	G22
91	B6IN1	G21		92	B6IO8	F22
93	B6IO9	F21		94	GND	–
95	B6IO10	E22		96	B6IO11	E21
97	B6IO12	D22		98	B6IO13	D21
99	GND	–		100	B6IO14	C22
101	B6IO15	C21		102	B6IO16	B22
103	B6IO17	B21		104	GND	–
105	B7IO0	A20		106	B7IO1	B20
107	B7IO2	A19		108	B7IO3	B19
109	GND	–		110	B7IO4	A18
111	B7IO5	B18		112	B7IO6	A17
113	B7IO7	B17		114	GND	–
115	B7IO8	A16		116	B7IO9	B16
117	B7IO10	A15		118	B7IO11	B15
119	GND	–		120	B7IO12	A14
121	B7IO13	B14		122	B7IO14	A13
123	B7IO15	B13		124	GND	–
125	B7IO38	G14		126	B7IN0	A12
127	B7IN1	B12		128	B8I038	D6
129	GND	–		130	B8IN0	A11
131	B8IN1	B11		132	B8IO20	A10
133	B8IO21	B10		134	GND	–
135	B8IO22	A9		136	B8IO23	B9
137	B8IO24	A8		138	B8IO25	B8
139	GND	–		140	B8IO26	A7
141	B8IO27	B7		142	B8IO28	A6
143	B8IO29	B6		144	GND	–
145	B8IO30	A5		146	B8IO31	B5
147	B8IO32	A4		148	B8IO33	B4
149	GND	–		150	B8IO34	A3
151	B8IO35	B3		152	B8IO36	F7
153	B8IO37	G7		154	GND	–
155	HW_RST	–		156	GND	–
Connector P1:A						
157	3.3V	–		158	3.3V	–
159	3.3V	–		160	3.3V	–
161	GND	–		162	B3IO16	AB3
163	B3IO17	AA3		164	B3IO18	Y6
165	B3IO19	Y3		166	3.3V	–
167	B3IO20	AB4		168	B3IO21	AA4
169	B3IO22	V7		170	B3IO23	W6
171	3.3V	–		172	B3IO24	Y10
173	B3IO25	W10		174	B3IO26	Y7
175	B3IO27	W7		176	3.3V	–
177	B3IO28	Y8		178	B3IO29	W9
179	B3IO30	V8		180	B3IO31	U9

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Table 2 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
181	3.3V	–		182	B3IO32	V10
183	B3IO33	U10		184	B3IO34	U8
185	B3IO35	U7		186	3.3V	–
187	B4IO20	R15		188	B4IO21	R14
189	B4IO22	V13		190	B4IO23	U13
191	VCCIO4	–		192	B4IO24	U14
193	B4IO25	V14		194	B4IO26	Y13
195	B4IO27	W13		196	VCCIO4	–
197	B4IO28	V15		198	B4IO29	U15
199	B4IO30	Y17		200	B4IO31	W17
201	VCCIO4	–		202	B4IO32	R16
203	B4IO33	T16		204	B4IO334	W14
205	B4IO35	W15		206	VCCIO4	–
207	B4IO36	V16		208	RST	–
209	B5IO18	U20		210	B5IO19	U19
211	GND	–		212	B5IO20	R17
213	B5IO21	W20		214	B5IO22	T17
215	B5IO23	T18		216	VCCIO5	–
217	B5IO24	R18		218	B5IO25	R19
219	B5IO26	R20		220	B5IO27	P20
221	VCCIO5	–		222	B5IO28	P17
223	B5IO29	N16		224	B5IO30	N17
225	B5IO31	N18		226	VCCIO5	–
227	B5IO32	N20		228	B5IO33	N19
229	B5IO34	M20		230	B5IO35	M19
231	VCCIO5	–		232	B5IO36	M16
Connector P1:B						
233	B6IO34	K19		234	B6IO18	K17
235	B6IO19	K18		236	VCCIO6	–
237	B6IO20	J18		238	B6IO21	H18
239	B6IO22	G18		240	B6IO23	H17
241	VCCIO6	–		242	B6IO24	J17
243	B6IO25	H16		244	B6IO26	H20
245	B6IO27	H19		246	VCCIO6	–
247	B6IO28	F20		248	B6IO29	F19
249	B6IO30	D20		250	B6IO31	C20
251	VCCIO6	–		252	B6IO32	F17
253	B6IO33	G17		254	B7IO16	–
255	B7IO17	D17		256	GND	–
257	B7IO18	C15		258	B7IO19	D15
259	B7IO20	C19		260	B7IO21	D19
261	VCCIO7	–		262	B7IO22	F15
263	B7IO23	G16		264	B7IO24	F16
265	B7IO25	E16		266	VCCIO7	–
267	B7IO26	C13		268	B7IO27	D13
269	B7IO28	G13		270	B7IO29	F13
271	VCCIO7	–		272	B7IO30	E15
273	B7IO31	E14		274	B7IO32	E13
275	B7IO33	E12		276	VCCIO7	–

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Table 2 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
277	B7IO34	E11		278	B7IO35	F11
279	B7IO36	G15		280	B7IO37	F14
281	GND	–		282	B8IO0	G10
283	B8IO1	F10		284	B8IO2	D10
285	B8IO3	E10		286	VCCIO8	–
287	B8IO4	G11		288	B8IO5	C10
289	B8IO6	G9		290	B8IO7	F9
291	VCCIO8	–		292	B8IO8	C8
293	B8IO9	C7		294	B8IO10	E9
295	B8IO11	E7		296	VCCIO8	–
297	B8IO12	C6		298	B8IO13	D7
299	B8IO14	F8		300	B8IO15	G8
301	VCCIO8	–		302	B8IO16	E5
303	B8IO17	E5		304	B8IO18	C3
305	B8IO19	C4		306	VCCIO8	–
307	B1IO0	H5		308	B1IO1	J6
309	B1IO2	J7		310	B1IO3	K7
311	GND	–		312	B1IO4	H6
313	B1IO5	H7		314	GND	–

3.6 Schematics

Schematics for the MCXL SoM may be obtained on request.