MAXEVK Hardwaremanual

Release 1

ARIES Embedded GmbH

May 28, 2020

CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

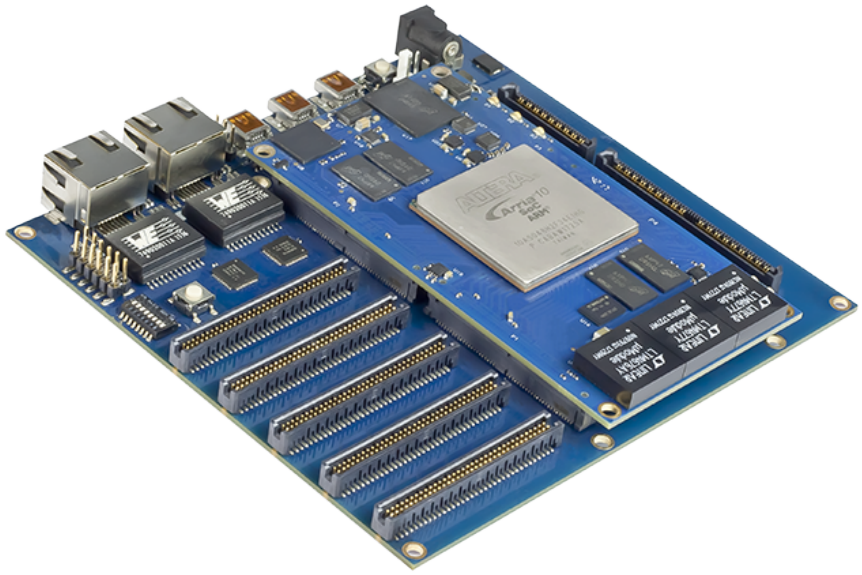
1.6 Change Log

Revision	Date	Revised	Comment
1.0	28.05.2020	js, aw	Initial creation

CHAPTER

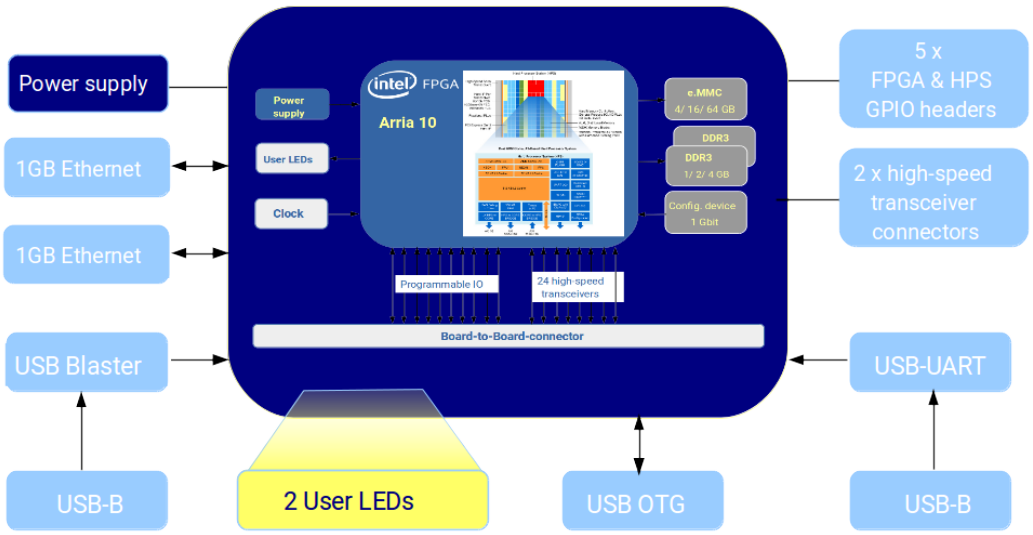
TWO

OVERVIEW



The MAXEVK was developed to serve the MAX System on Modul, based on Arria 10 SoC-FPGA devices. It offers most interfaces of the HPS Subsystem and all FPGA I/O pins on to a 1,27mm pin header. 24 transceive channels are available at two Samtec high-speed connectors. The HPS supports two Gigabit Ethernet interfaces, one USB OTG interface as well as a UART/USB converter. For in-system-programming a USB-Blaster II is implemented.

2.1 Block Diagram



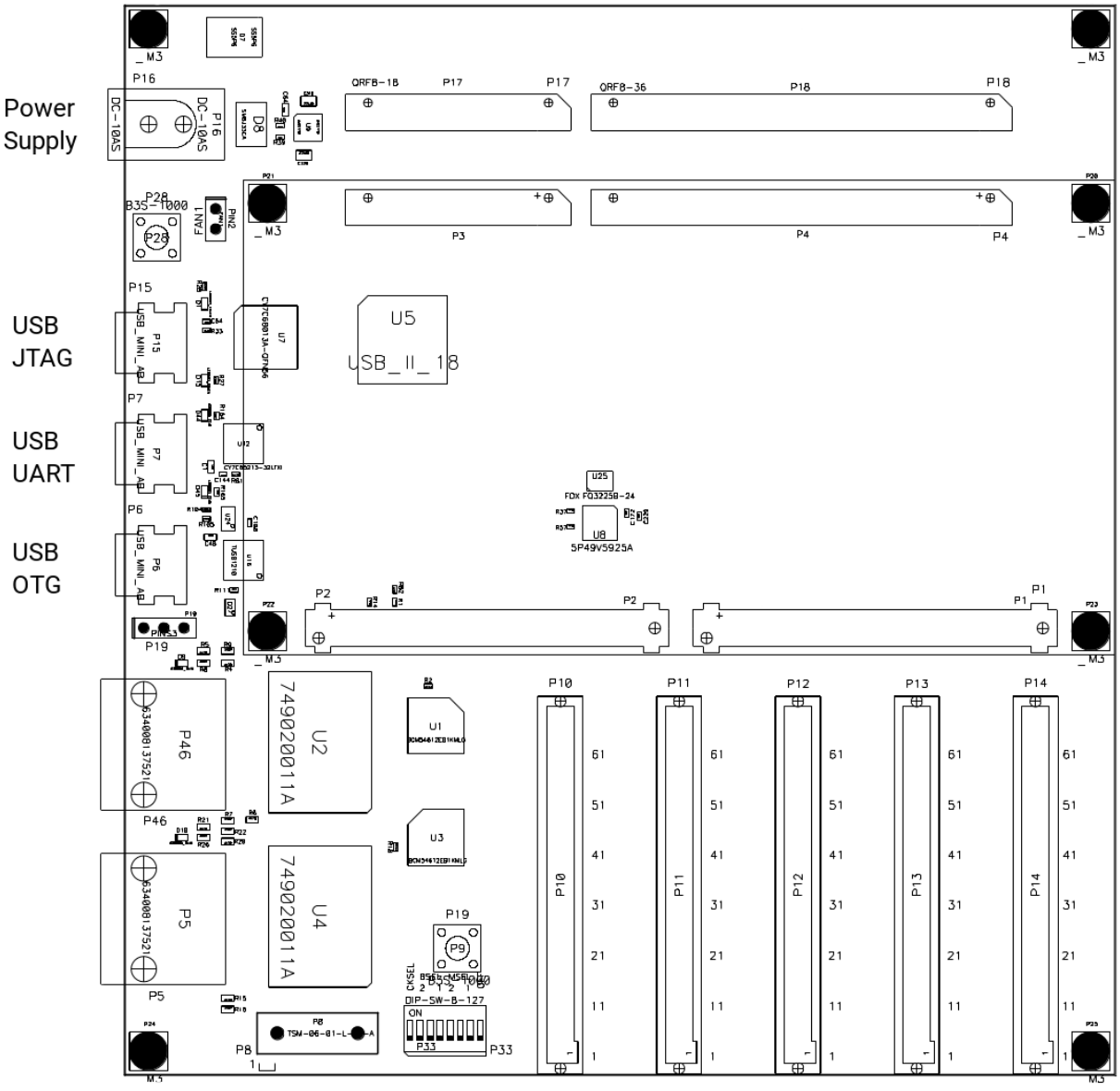
2.2 Feature Set

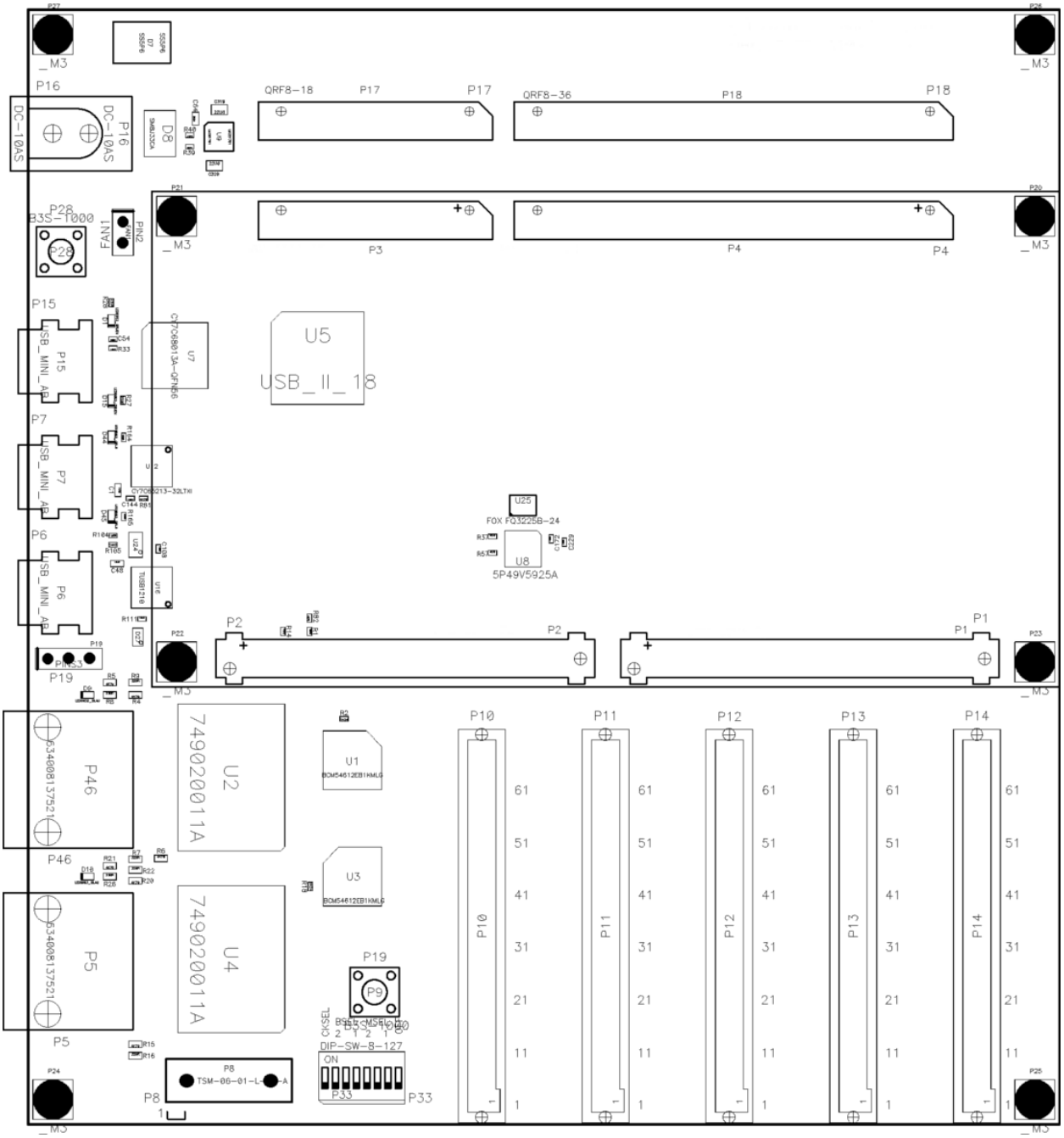
The MAXEVK provides the following features

- 2 x Gigabit Ethernet
- USB-OTG
- UART / USB converter
- embedded USB-Blaster II
- 5 x pinheader for FPGA / HPS signals
- 2 x high-speed conectors for 24 transceiver
- 12V power supply
- clock generation for Ethernet / USB
- wall plug power supply
- size: 180 x 180mm

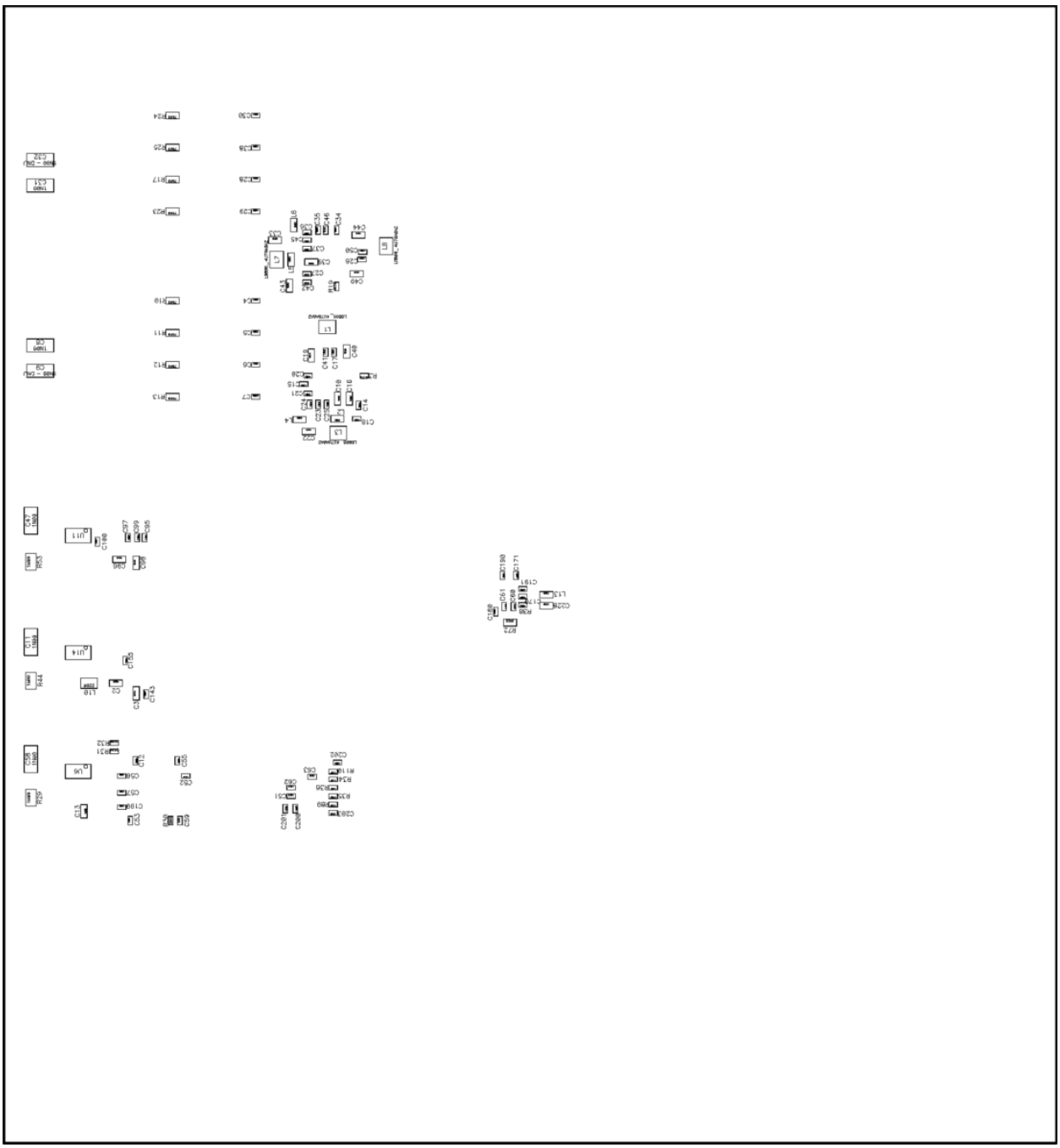
2.3 Parts Location

2.3.1 Components Top Side



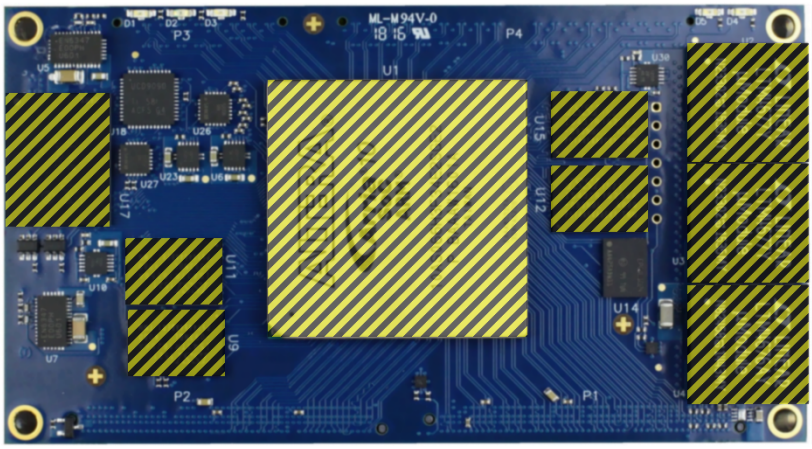

P16
DC-10AS
QRF8-18
P17
QRF8-36
P18
P28
B3S-1000
P15
USB_MINI_AB
U5
USB_II_18
P7
P6
U25
FOX FQ3225B-24
U8
5P49V5925A
P2
P1
P19
P46
P5
U2
74902011A
U4
74902011A
U1
U3
P10
P11
P12
P13
P14
P8
TSM-06-01-L-A
P33
DIP-SW-8-127
P9
P3
P4
P20
P21
P22
P23
P24
P25
P26
P27
_M3

2.3.2 Components Bottom Side



2.4 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on MAX it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:

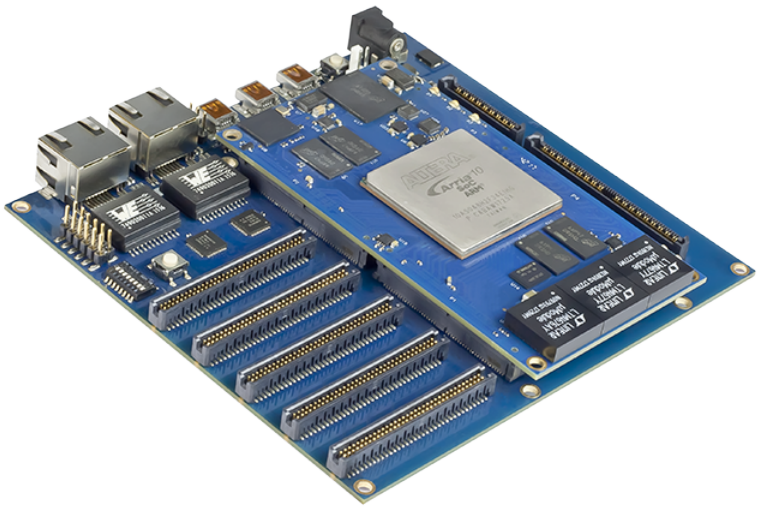


CHAPTER

THREE

MAXEVK

The MAXEVK was designed for board bring-up and board testing of the MAX Arria 10 SoM. It provides several interfaces for all the on-module functions.



HPS:

- Dual Gigabit Ethernet
- USB OTG
- UART / USB Interface

FPGA:

- Pinheader for all I/O Pins
- Transceiver

Miscellaneous:

- Fan header
- Embedded USB Blaster
- JTAG connection to MAX10
- Power Supply

3.1 DIP-Switch (P33)

The DIP Switch is used to configure the modules. It contains the *MSEL*, *BSEL* Signals and the *IDT Clock Select* signal. The last switch can be used to switch the board on and off. The default setting is *OFF*.

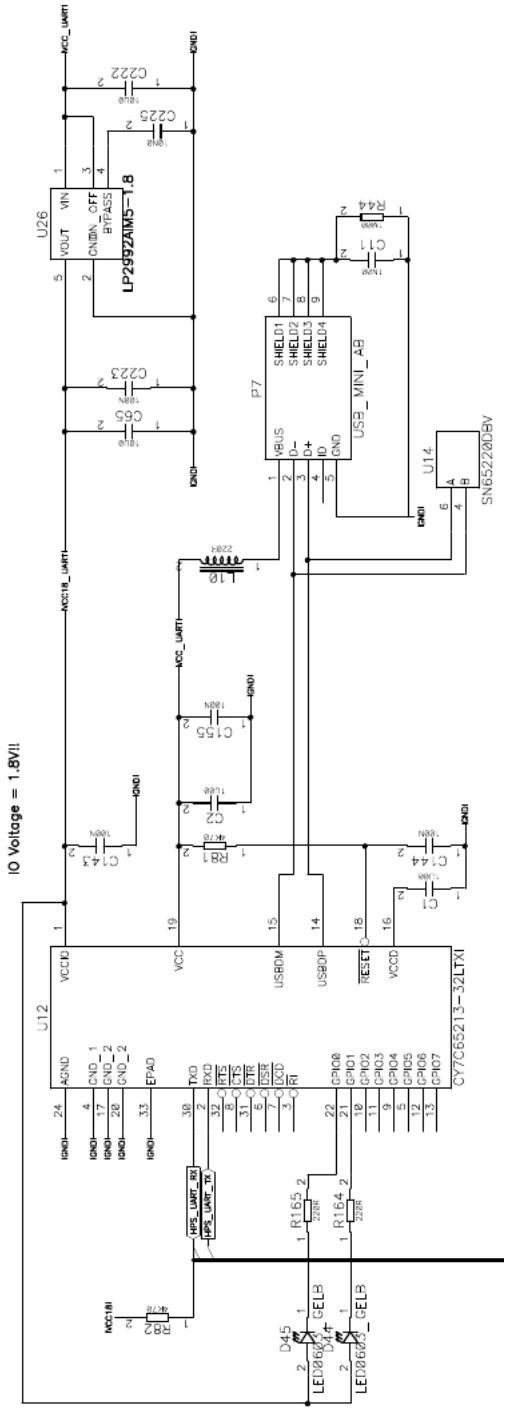
MSEL Pins default setting: **AS standard**

BSEL Pins default setting: **eMMC boot**

Nr.	Function
1	IDT Clock Select for Transceiver Clocks ON: external Clock from P3 OFF: internal Crystal (25 MHz)
2	BSEL2 ON: 0 OFF: 1
3	BSEL1 ON: 1 OFF: 0
4	BSEL0 ON: 0 OFF: 1
5	MSEL2 ON: 1 OFF: 0
6	MSEL1 ON: 0 OFF: 1
7	MSEL0 ON: 0 OFF: 1
8	EXT_OFF ON: Switch Module OFF OFF: Power up Module

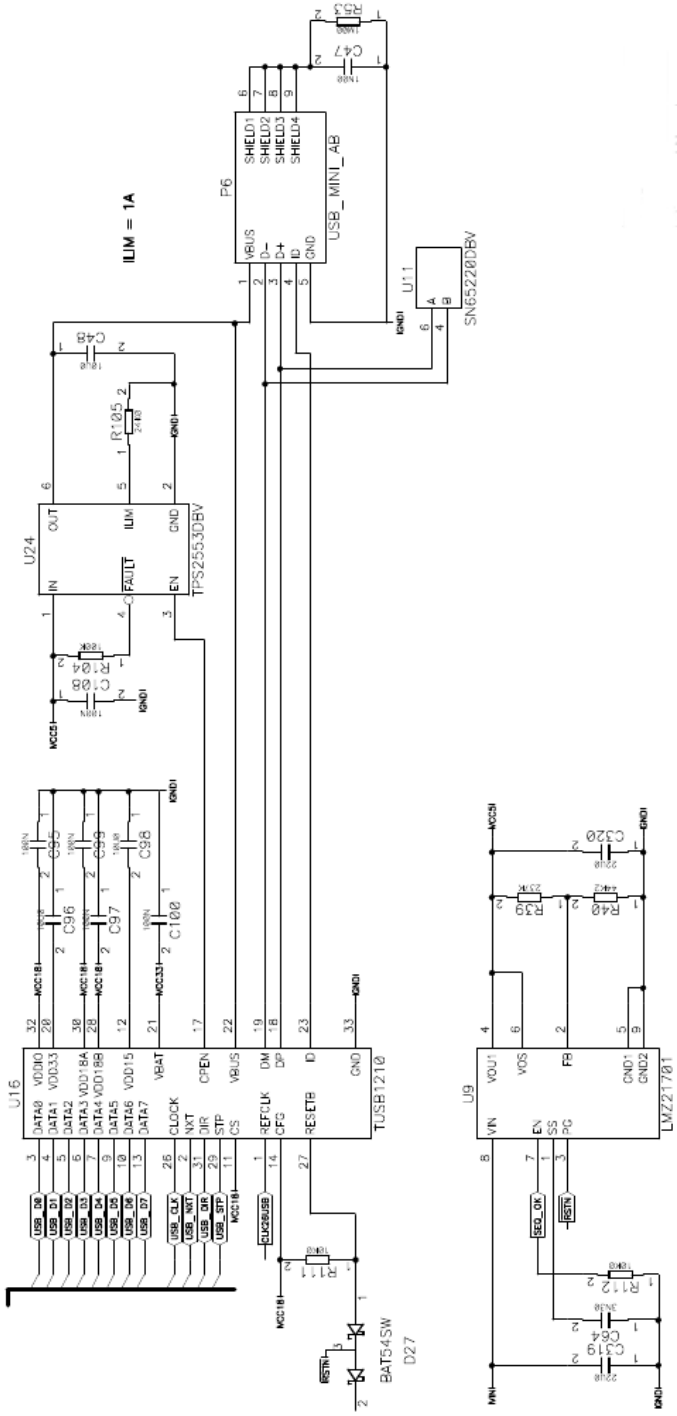
3.2 UART / USB

The UART / USB converter is based on the Cypress CY7C65213-32 device and provides a serial connection between the HPS and the development PC. For Linux this connection is the default terminal interface.



3.3 USB - OTG

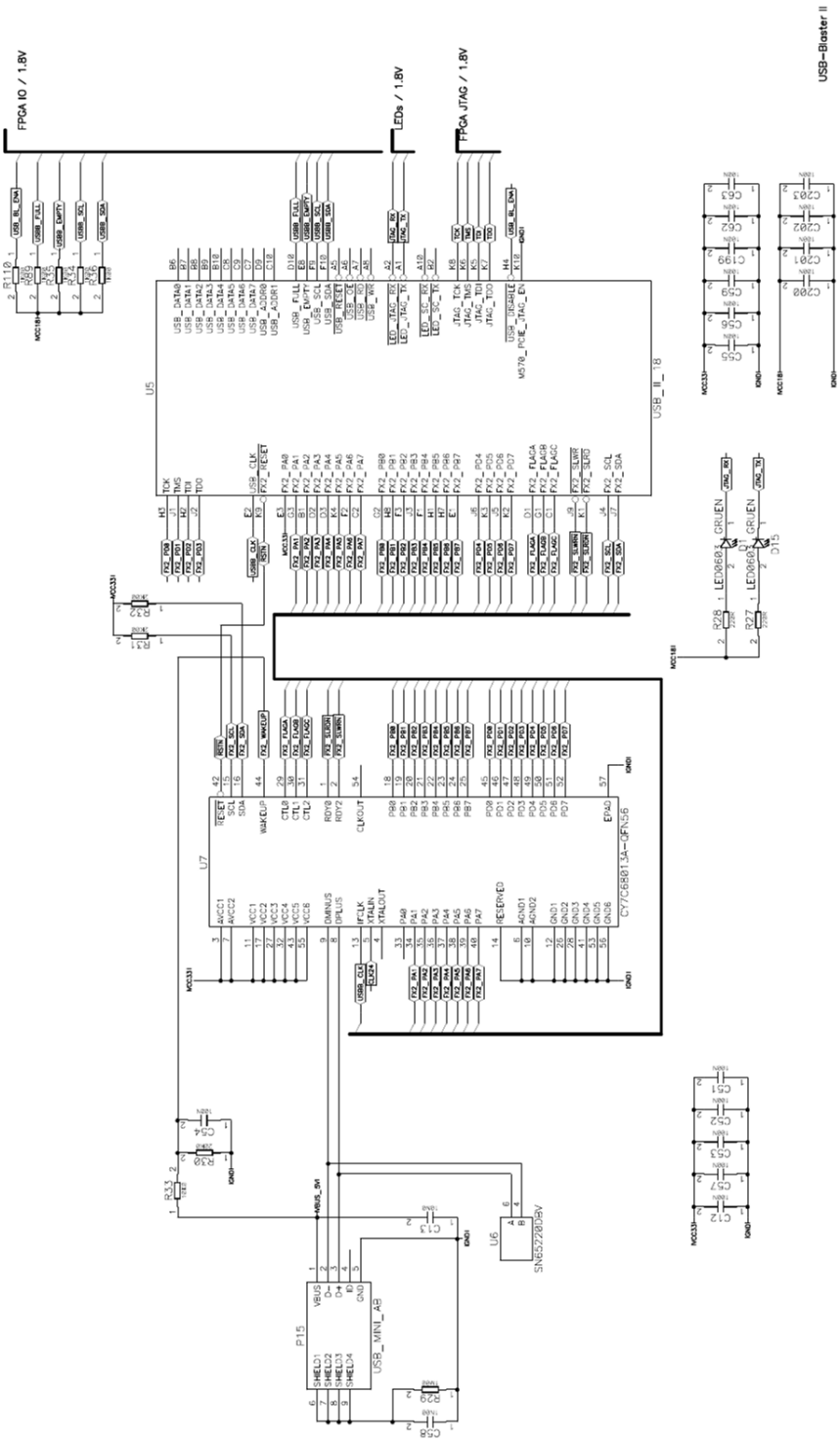
A TUSB1210 USB OTG Phy is implemented on the board, together with a 5V power switch and the mini USB connector P6.



3.4 USB-Blaster II

The MAXEVK base board is equipped with an on-board USB-Blaster-II, which can be used as programming and debugging interface for the MAX module.

The module provides one JTAG port, where the FPGA and the HPS are chained together.

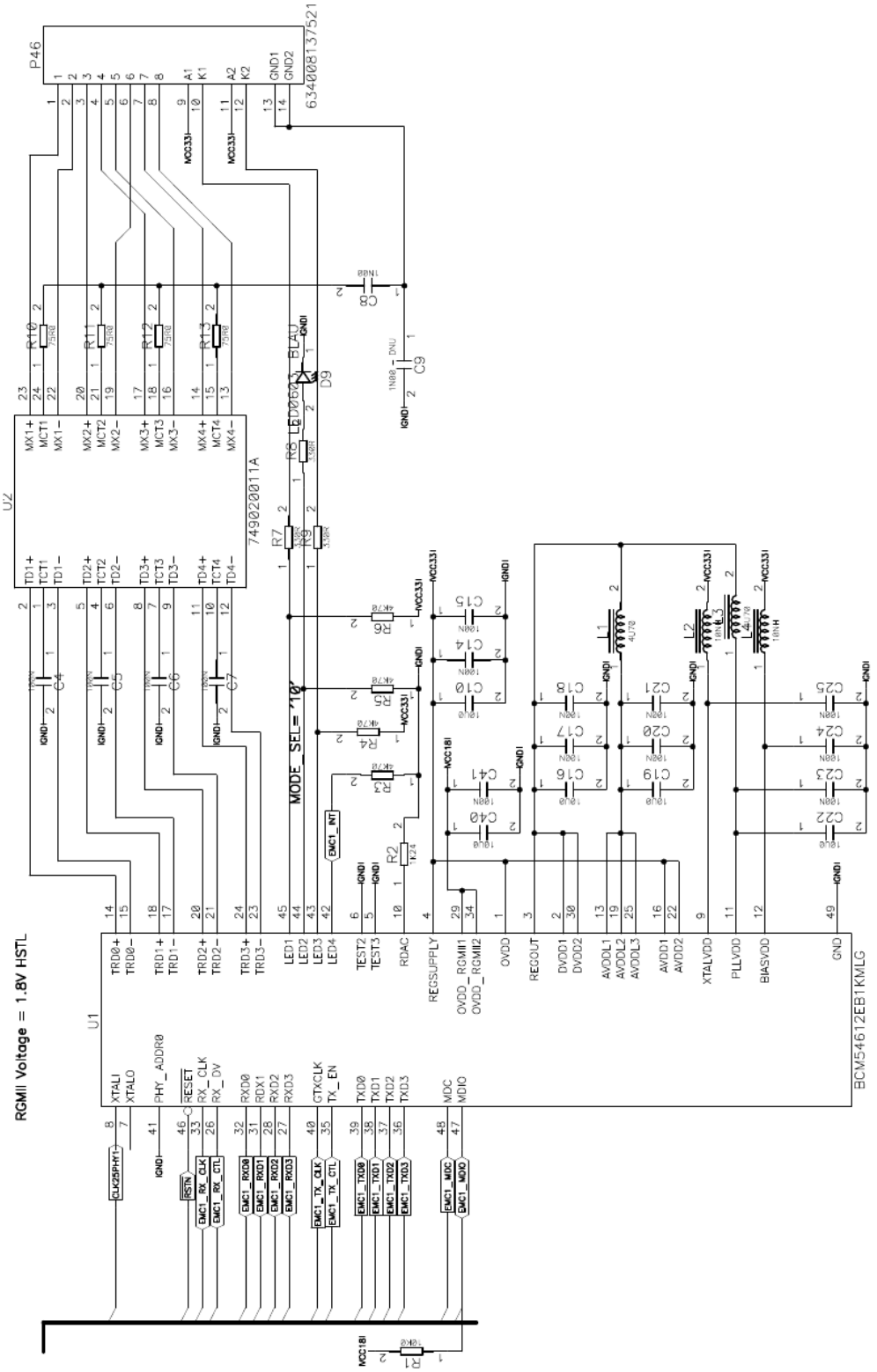


3.5 Gigabit Ethernet

The base board provides two Broadcom BCM54612 Gigabit Ethernet Phys, the Gigabit Ethernet transformer and the RJ45 connector. The two PHY LEDs are also connected to the RJ45 LEDs. A third LED on the board shows the Gigabit Link status.

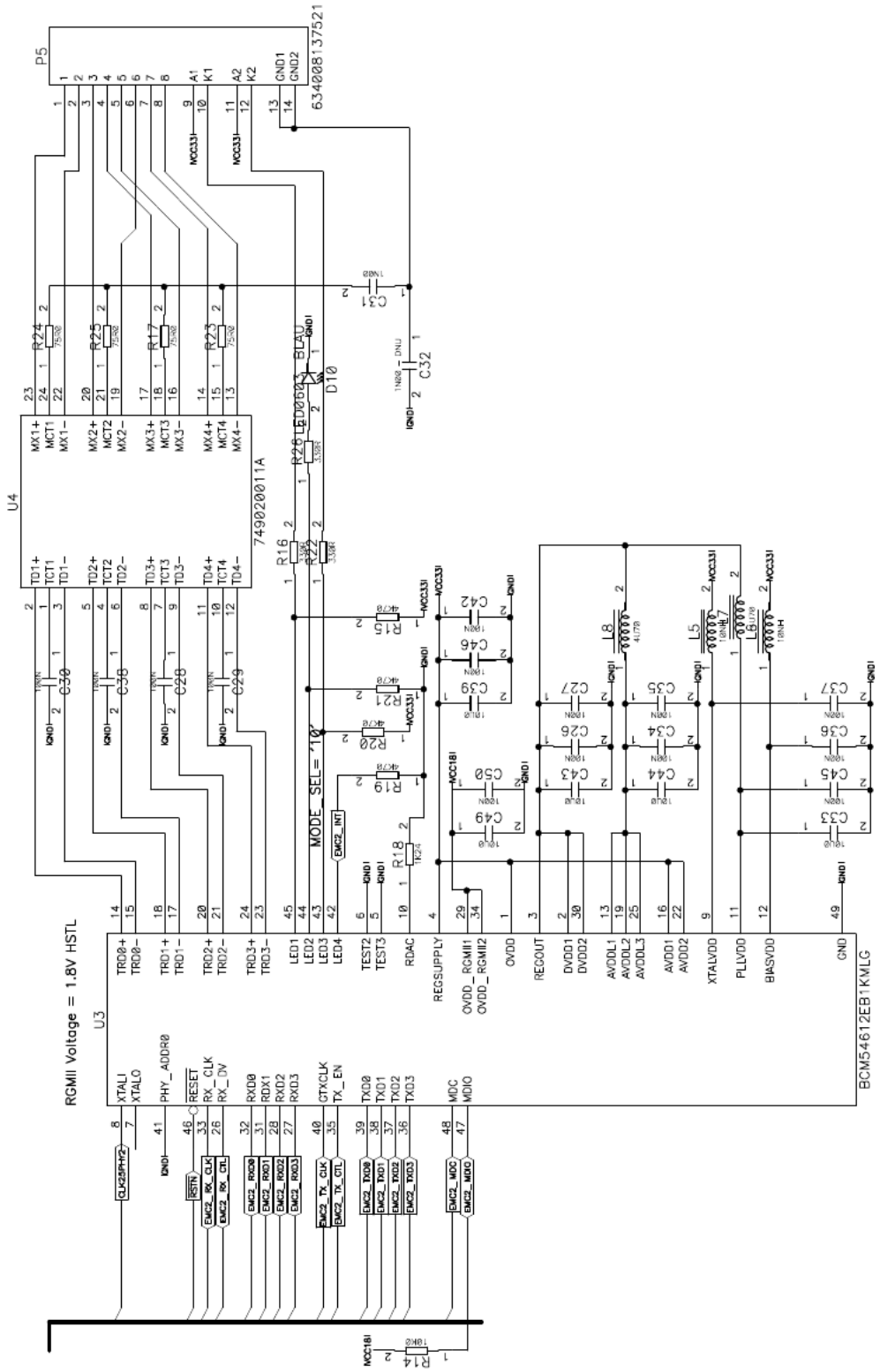
3.6 Gigabit Ethernet 1

Phy Address: 00000 Connector: P46 Connector type: TJ45



3.7 Gigabit Ethernet 2

Phy Address: 00000 Connector: P5 Connector type: TJ45



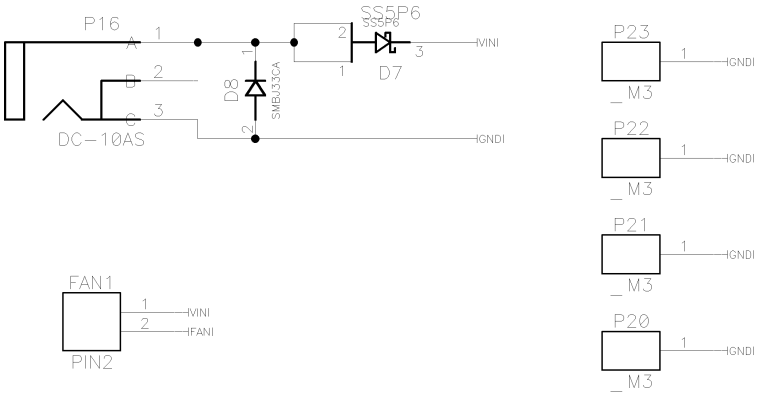
3.8 Power Supply

The power stage is build for an input voltage of 12V. The 12V is provided to the MAX-SoC module and is used for a 5V rail on the baseboard - mainly for the USB-OTG supply. The power plug is a DC10 connector.

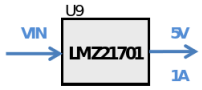
Out: GND

IN: 12V

Power Supply:



5V Rail:



3.9 Reset Buttons

The button P9 activates the HPS_RSTN signal, which is connected to the HPS warm reset input.

P28 is the power good reset button.

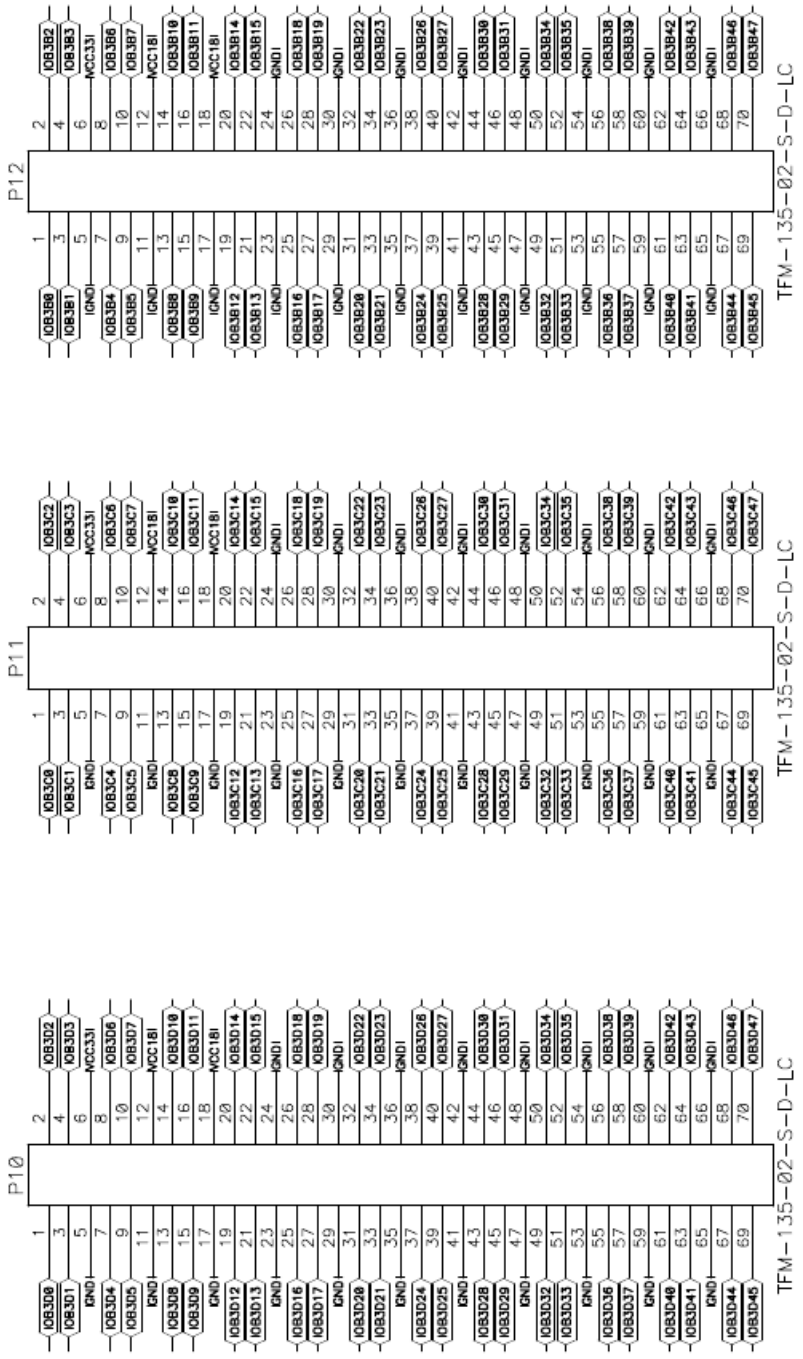
3.10 FAN header

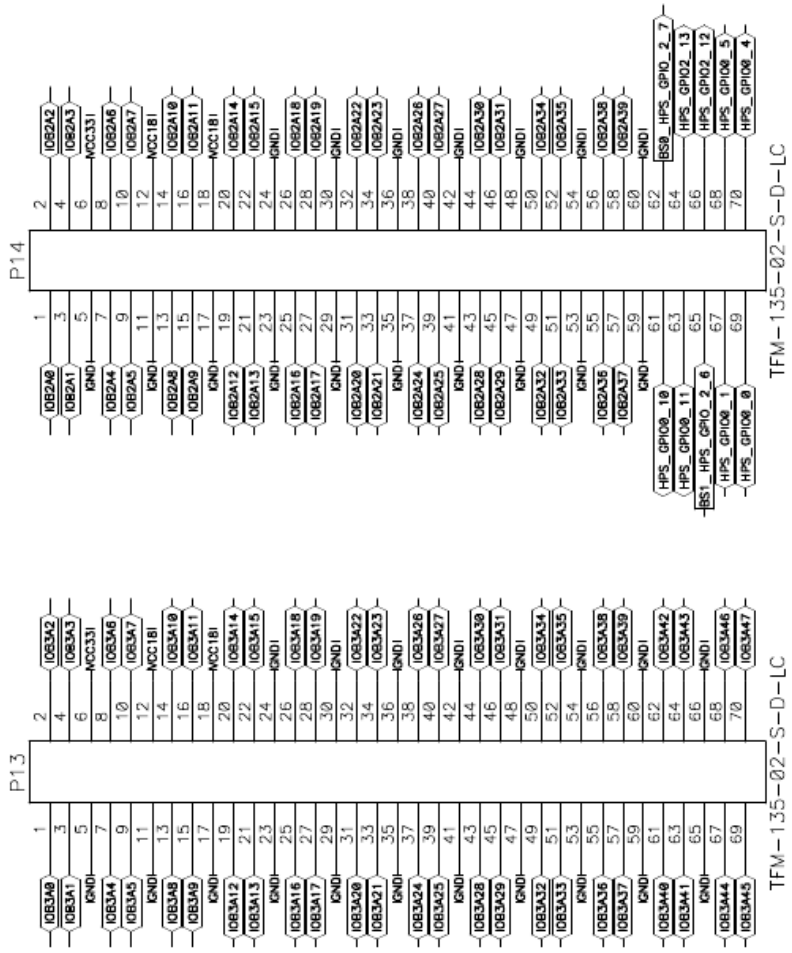
The FAN1 header provides the connection to the FAN of the module.

Pin	Function
1	VIN
2	FAN signal from module

3.11 IO Header

The following section describes the availability of IO signals on different pin headers.




P14
TFM-135-02-S-D-LC
P13
TFM-135-02-S-D-LC

3.12 IOBANK 2A - P14

Function	FPGA	#	#	FPGA	Function
IOB2A0	AK14	1	2	AK13	IOB2A2
IOB2A1	AL14	3	4	AL13	IOB2A3
GND		5	6		VCC33
IOB2A4	AL15	7	8	AP12	IOB2A6
IOB2A5	AM15	9	10	AN12	IOB2A7
GND		11	12		VCC18
IOB2A8	AH15	13	14	AH14	IOB2A10
IOB2A9	AJ15	15	16	AJ14	IOB2A11
GND		17	18		VCC18
IOB2A12	AM16	19	20	AM13	IOB2A14
IOB2A13	AL16	21	22	AN13	IOB2A15
GND		23	24		GND
IOB2A16	AK17	25	26	AF16	IOB2A18
IOB2A17	AJ17	27	28	AG16	IOB2A19
GND		29	30		GND
IOB2A20	AG18	31	32	AP14	IOB2A22
IOB2A21	AF18	33	34	AN14	IOB2A23
GND		35	36		GND
IOB2A24	AP17	37	38	AN17	IOB2A26
IOB2A25	AP16	39	40	AM17	IOB2A27
GND		41	42		GND
IOB2A28	AN18	43	44	AP15	IOB2A30
IOB2A29	AM18	45	46	AN15	IOB2A31
GND		47	48		GND
IOB2A32	AH17	49	50	AL18	IOB2A34
IOB2A33	AG17	51	52	AK18	IOB2A35
GND		53	54		GND
IOB2A36	AE19	55	56	AE17	IOB2A38
IOB2A37	AF19	57	58	AE16	IOB2A39
GND		59	60		GND
HPS_GPIO0_10	L20	61	62	E16	BSEL0_HPS_GPIO2_7
HPS_GPIO0_11	M20	63	64	H15	HPS_GPIO2_13
BSEL1_HPS_GPIO2_6	G15	65	66	F15	HPS_GPIO2_12
HPS_GPIO0_1	M18	67	68	L21	HPS_GPIO0_5
HPS_GPIO0_0	M17	69	70	M21	HPS_GPIO0_4

3.13 IOBANK 3A - P13

Function	FPGA	#	#	FPGA	Function
IOB3A0	AJ6	1	2	AG7	IOB3A2
IOB3A1	AJ7	3	4	AH7	IOB3A3
GND		5	6		VCC33
IOB3A4	AL4	7	8	AM2	IOB3A6
IOB3A5	AL5	9	10	AM1	IOB3A7
GND		11	12		VCC18
IOB3A8	AE8	13	14	AH5	IOB3A10
IOB3A9	AF8	15	16	AJ5	IOB3A11
GND		17	18		VCC18
IOB3A12	AM5	19	20	AL3	IOB3A14
IOB3A13	AM6	21	22	AM3	IOB3A15
GND		23	24		GND
IOB3A16	AG8	25	26	AK8	IOB3A18
IOB3A17	AH8	27	28	AK7	IOB3A19
GND		29	30		GND
IOB3A20	AK6	31	32	AN4	IOB3A22
IOB3A21	AL6	33	34	AP4	IOB3A23
GND		35	36		GND
IOB3A24	AE9	37	38	AK9	IOB3A26
IOB3A25	AF9	39	40	AJ9	IOB3A27
GND		41	42		GND
IOB3A28	AM7	43	44	AN5	IOB3A30
IOB3A29	AN7	45	46	AP5	IOB3A31
GND		47	48		GND
IOB3A32	AF10	49	50	AG9	IOB3A34
IOB3A33	AG10	51	52	AH10	IOB3A35
GND		53	54		GND
IOB3A36	AG11	55	56	AP6	IOB3A38
IOB3A37	AF11	57	58	AP7	IOB3A39
GND		59	60		GND
IOB3A40	AE11	61	62	AL8	IOB3A42
IOB3A41	AE12	63	64	AL9	IOB3A43
GND		65	66		GND
IOB3A44	AN9	67	68	AM8	IOB3A46
IOB3A45	AP9	69	70	AN8	IOB3A47

3.14 IOBANK 3B – P12

Function	FPGA	#	#	FPGA	Function
IOB3B0	AB7	1	2	AC5	IOB3B2
IOB3B1	AB8	3	4	AC4	IOB3B3
GND		5	6		VCC33
IOB3B4	AE3	7	8	AD1	IOB3B6
IOB3B5	AE2	9	10	AD2	IOB3B7
GND		11	12		VCC18
IOB3B8	AB11	13	14	AD4	IOB3B10
IOB3B9	AB10	15	16	AE4	IOB3B11
GND		17	18		VCC18
IOB3B12	AF4	19	20	AB5	IOB3B14
IOB3B13	AF3	21	22	AB6	IOB3B15
GND		23	24		GND
IOB3B16	AE7	25	26	AC7	IOB3B18
IOB3B17	AE6	27	28	AD7	IOB3B19
GND		29	30		GND
IOB3B20	AG3	31	32	AE1	IOB3B22
IOB3B21	AH3	33	34	AF1	IOB3B23
GND		35	36		GND
IOB3B24	AC10	37	38	AD6	IOB3B26
IOB3B25	AC9	39	40	AD5	IOB3B27
GND		41	42		GND
IOB3B28	AH4	43	44	AG2	IOB3B30
IOB3B29	AJ4	45	46	AG1	IOB3B31
GND		47	48		GND
IOB3B32	AD9	49	50	AF6	IOB3B34
IOB3B33	AC8	51	52	AG6	IOB3B35
GND		53	54		GND
IOB3B36	AJ2	55	56	AH2	IOB3B38
IOB3B37	AK2	57	58	AJ1	IOB3B39
GND		59	60		GND
IOB3B40	AD11	61	62	AF5	IOB3B42
IOB3B41	AD10	63	64	AG5	IOB3B43
GND		65	66		GND
IOB3B44	AK3	67	68	AK1	IOB3B46
IOB3B45	AK4	69	70	AL1	IOB3B47

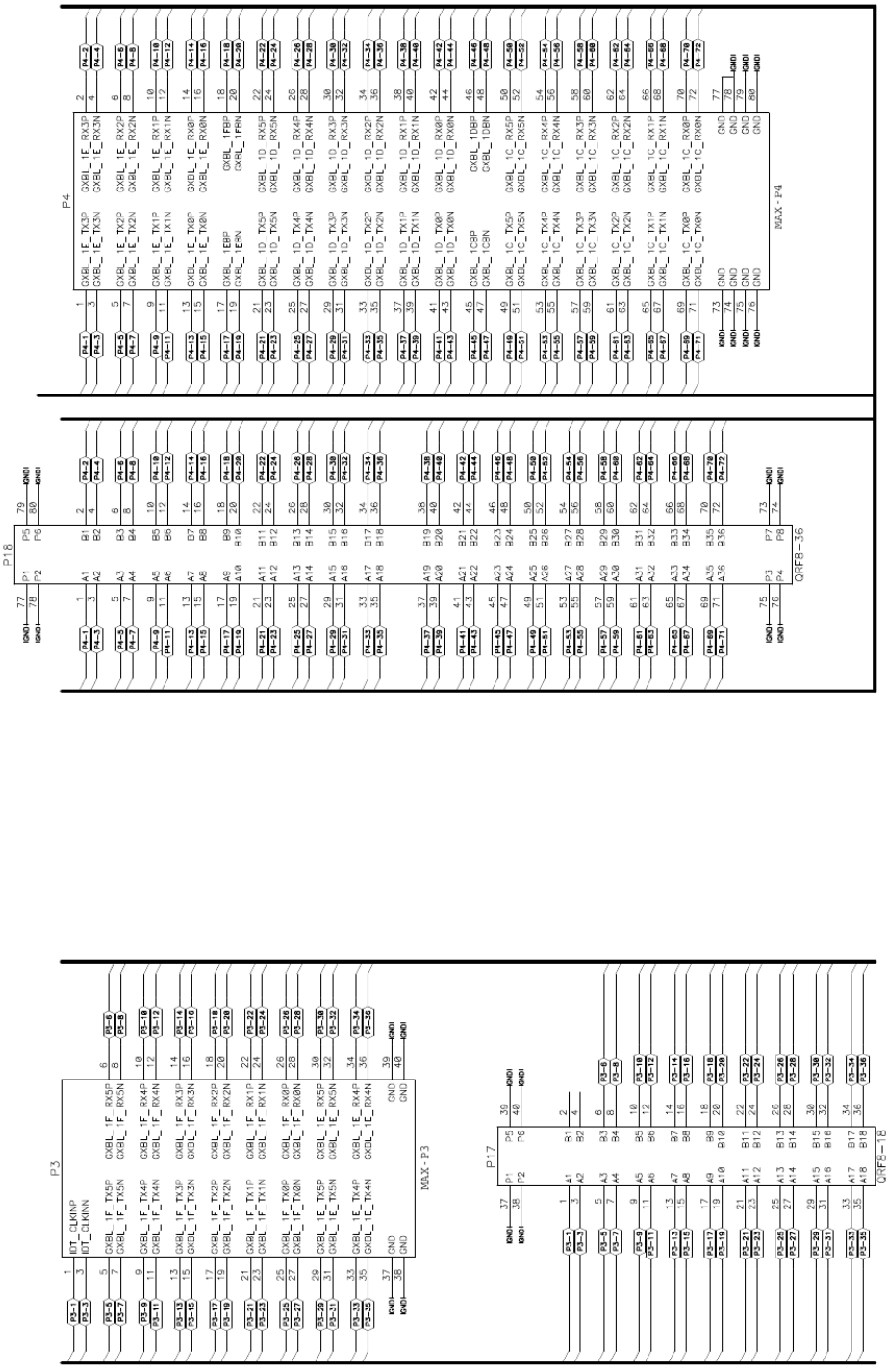
3.15 IOBANK 3C – P11

Function	FPGA	#	#	FPGA	Function
IOB3C0	R4	1	2	P5	IOB3C2
IOB3C1	T4	3	4	P4	IOB3C3
GND		5	6		VCC33
IOB3C4	R3	7	8	R2	IOB3C6
IOB3C5	T3	9	10	P2	IOB3C7
GND		11	12		VCC18
IOB3C8	Y9	13	14	T6	IOB3C10
IOB3C9	Y8	15	16	T5	IOB3C11
GND		17	18		VCC18
IOB3C12	V4	19	20	P1	IOB3C14
IOB3C13	V5	21	22	R1	IOB3C15
GND		23	24		GND
IOB3C16	AA9	25	26	U5	IOB3C18
IOB3C17	AA8	27	28	U6	IOB3C19
GND		29	30		GND
IOB3C20	V3	31	32	T1	IOB3C22
IOB3C21	U3	33	34	U1	IOB3C23
GND		35	36		GND
IOB3C24	W7	37	38	W5	IOB3C26
IOB3C25	W6	39	40	W4	IOB3C27
GND		41	42		GND
IOB3C28	Y7	43	44	U2	IOB3C30
IOB3C29	Y6	45	46	V2	IOB3C31
GND		47	48		GND
IOB3C32	AA6	49	50	Y4	IOB3C34
IOB3C33	AA5	51	52	Y3	IOB3C35
GND		53	54		GND
IOB3C36	Y2	55	56	W2	IOB3C38
IOB3C37	Y1	57	58	W1	IOB3C39
GND		59	60		GND
IOB3C40	AB3	61	62	AA4	IOB3C42
IOB3C41	AB2	63	64	AA3	IOB3C43
GND		65	66		GND
IOB3C44	AA1	67	68	AC2	IOB3C46
IOB3C45	AB1	69	70	AC3	IOB3C47

3.16 IOBANK 3D - P10

Function	FPGA	#	#	FPGA	Function
IOB3D0	T10	1	2	P9	IOB3D2
IOB3D1	U10	3	4	N9	IOB3D3
GND		5	6		VCC33
IOB3D4	R7	7	8	L8	IOB3D6
IOB3D5	R8	9	10	K7	IOB3D7
GND		11	12		VCC18
IOB3D8	M8	13	14	R9	IOB3D10
IOB3D9	N8	15	16	T9	IOB3D11
GND		17	18		VCC18
IOB3D12	J5	19	20	L6	IOB3D14
IOB3D13	J4	21	22	K6	IOB3D15
GND		23	24		GND
IOB3D16	P7	25	26	L5	IOB3D18
IOB3D17	N7	27	28	M4	IOB3D19
GND		29	30		GND
IOB3D20	K4	31	32	J2	IOB3D22
IOB3D21	L4	33	34	J1	IOB3D23
GND		35	36		GND
IOB3D24	T8	37	38	M7	IOB3D26
IOB3D25	U8	39	40	M6	IOB3D27
GND		41	42		GND
IOB3D28	K3	43	44	K2	IOB3D30
IOB3D29	L3	45	46	K1	IOB3D31
GND		47	48		GND
IOB3D32	V8	49	50	P6	IOB3D34
IOB3D33	V9	51	52	R6	IOB3D35
GND		53	54		GND
IOB3D36	M3	55	56	L1	IOB3D38
IOB3D37	M2	57	58	M1	IOB3D39
GND		59	60		GND
IOB3D40	U7	61	62	W9	IOB3D42
IOB3D41	V7	63	64	W10	IOB3D43
GND		65	66		GND
IOB3D44	N5	67	68	N3	IOB3D46
IOB3D45	N4	69	70	N2	IOB3D47

3.17 Transceiver P7 / P18



The Transceiver pinout is identically to the module.

P3 – P7 QRF8-018-05.0-L-D-DP-A
P4 – P18 QRF8-036-05.0-L-D-DP-A

3.18 Clocking